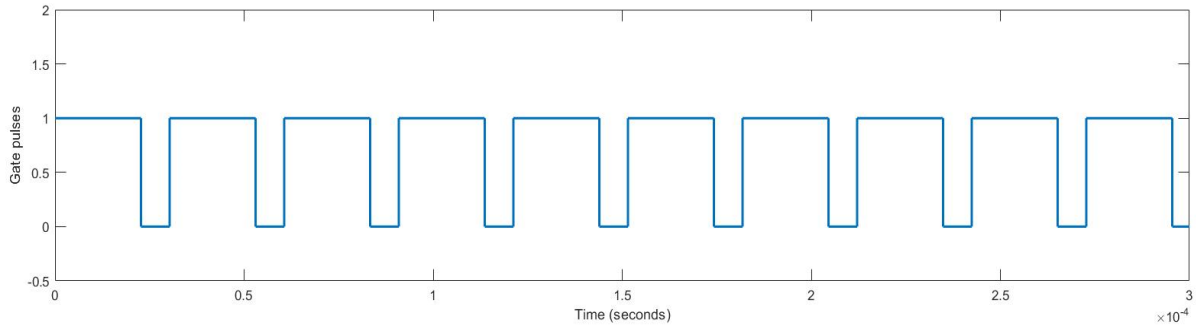

Fig 1. Gate pulses

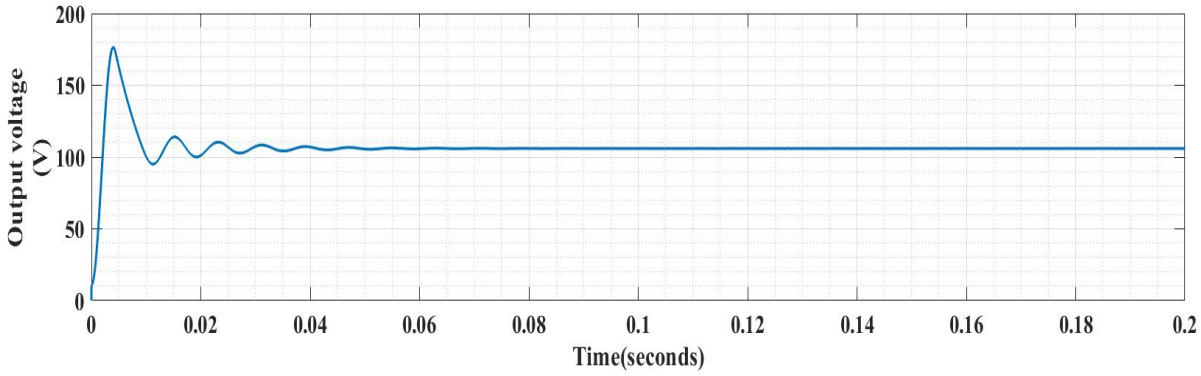

Fig 2. Open-loop output voltage at D=75%

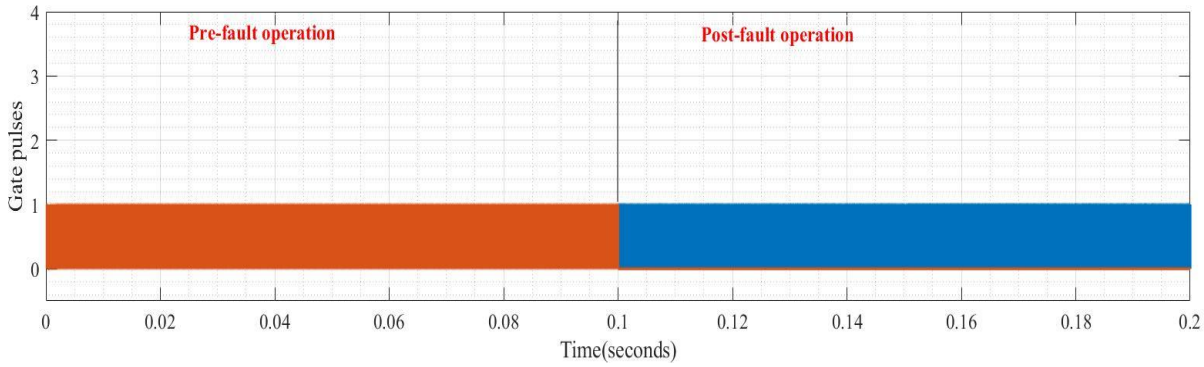

Fig 3. Gate pulses with switch-2 fault at t=0.1sec

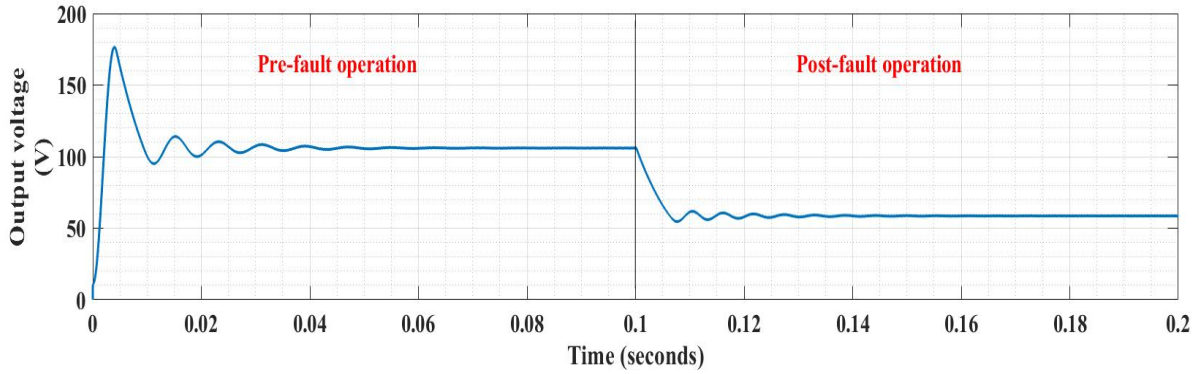

Fig 4. Open-loop output voltage at D=75% with switch-2 fault at t=0.1sec