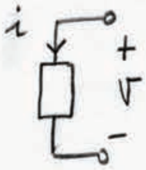
LECTURE 1 — INTRODUCTION AND LUMPED CIRCUIT ABSTRACTION

V-I Relationship



v-i relationship for resistor

$v = i \cdot R$

Lumped Matter Discipline

$$\frac{\partial \phi_B}{\partial t} = 0 \qquad \frac{\partial q}{\partial t} = 0 \quad \text{(} q \text{ — charge)} \qquad \text{speed} < c \text{ (speed of light)}$$

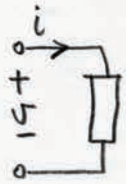
KVL Kirchhoff Voltage Law $\Sigma_j v_j = 0$

KCL Kirchhoff Current Law $\Sigma_j i_j = 0$

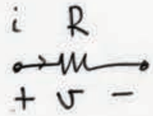
} power consumed: $v \cdot i$

LECTURE 2 — BASIC CIRCUIT ANALYSIS METHODS

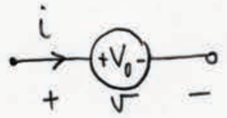
Associated Variables Discipline



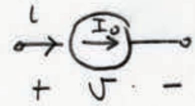
current entering by the positive terminal
↓
power consumed $v \cdot i > 0$



$v = i \cdot R$



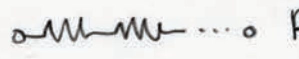
$v = V_0$



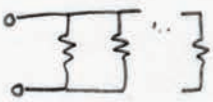
$i = I_0$

Method 1: KVL, KCL, element relationship v-i

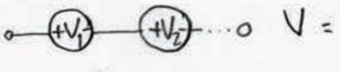
Method 2: Element combination rules



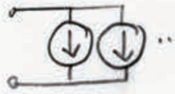
$R = \Sigma_j R_j$



$G = \frac{1}{R} = \Sigma_j G_j$



$V = \Sigma_j V_j$

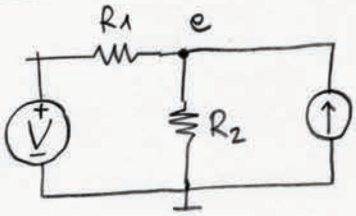


$I = \Sigma_j I_j$

Method 3: Node Analysis

1. Select reference node = ground
2. Label remaining nodes
3. Write KCL for all but ground node
4. Solve for node voltages
5. Solve for branch currents

LECTURE 3 — SUPERPOSITION, THÉVENIN & NORTON



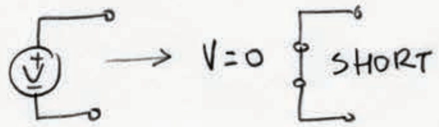
$$\frac{e-V}{R_1} + \frac{e}{R_2} - I = 0 \qquad \left(\frac{1}{R_1}+\frac{1}{R_2}\right)e = \frac{1}{R_1}V + I$$

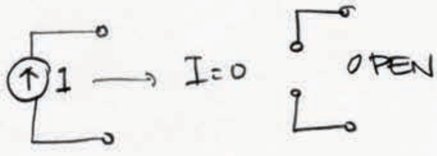
$$e = \frac{R_2}{R_1+R_2}\cdot V + \frac{R_1R_2}{R_1+R_2}\cdot I$$

lineal

Method 4: SUPERPOSITION

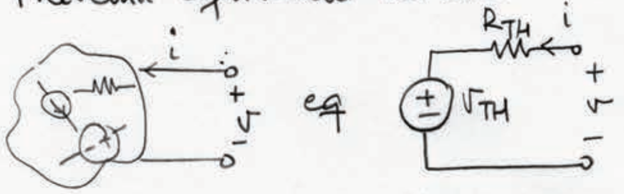
1. Find responses to each source alone
2. Sum individual responses



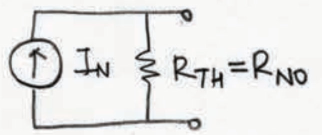


Method 5:

Thévenin equivalent network



Norton equivalent network



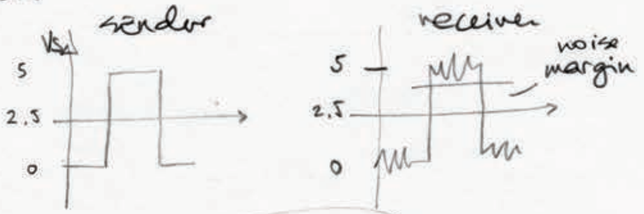
$$I_N = \frac{V_{TH}}{R_{TH}}$$

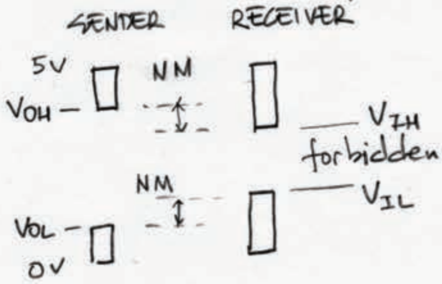
Superposition, Thévenin, Norton ONLY for linear networks

LECTURE 4 — THE DIGITAL ABSTRACTION

Value discretization

HIGH	LOW
5V	0V
TRUE	FALSE
1	0





"1" noise margin $V_{OH}-V_{IH}$

"0" noise margin $V_{IL}-V_{OL}$

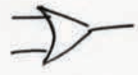
$V_{OH}, V_{OL}, V_{IH}, V_{IL}$

STATIC DISCIPLINE

Boolean logic

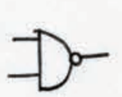
X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	NOT X
0	1
1	0

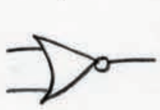


X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

BUFFER

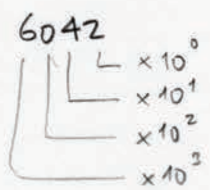


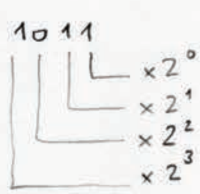
NAND



NOR

Number representation

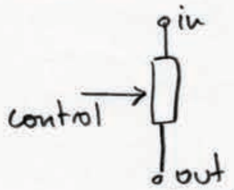


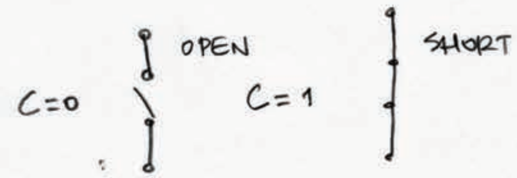


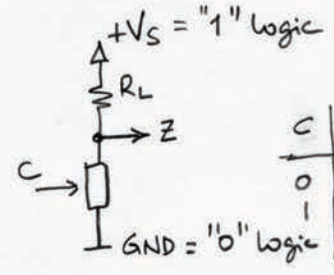
LECTURE 5

INSIDE THE DIGITAL GATE

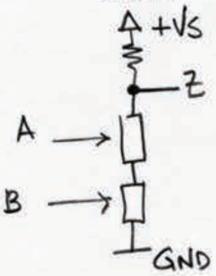
Abstract 'switch' device





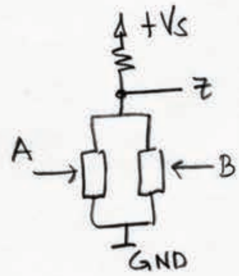


C	Z
0	1
1	0



A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

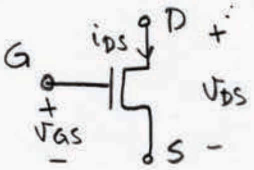
→ NAND



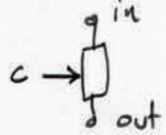
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

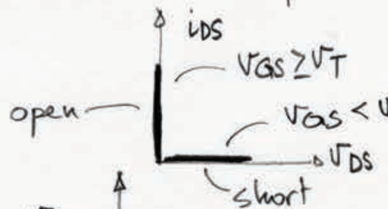
→ NOR

THE MOSFET DEVICE

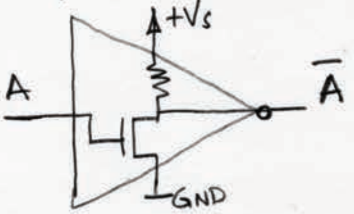


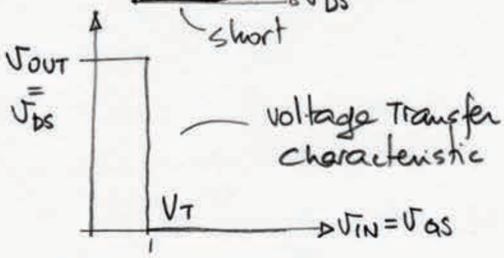
switch model (S model) of the MOSFET →

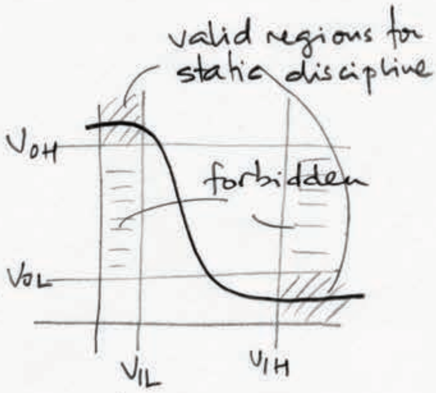




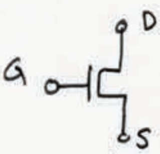
Mosfet inverter



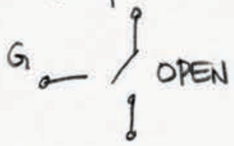




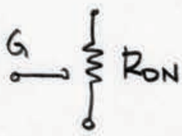
Switch Resistor (SR model) of the MOSFET

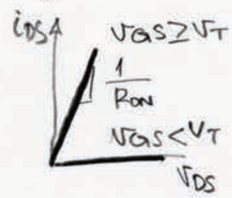


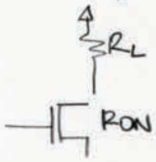
OFF state

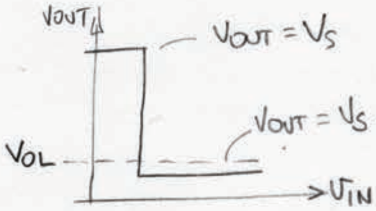


ON state







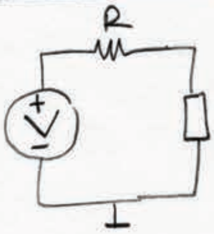


$V_{OUT} = V_S \cdot \frac{R_{ON}}{R_L + R_{ON}} < V_{OL}$ for static discipline

SR model 'ON' state is Linear!

LECTURE 6

NONLINEAR CIRCUITS



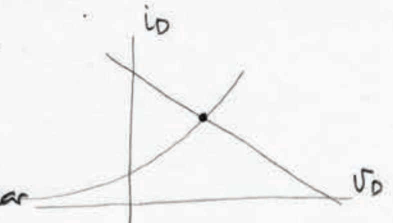
- non linear

eg. $i = ae^{bv}$

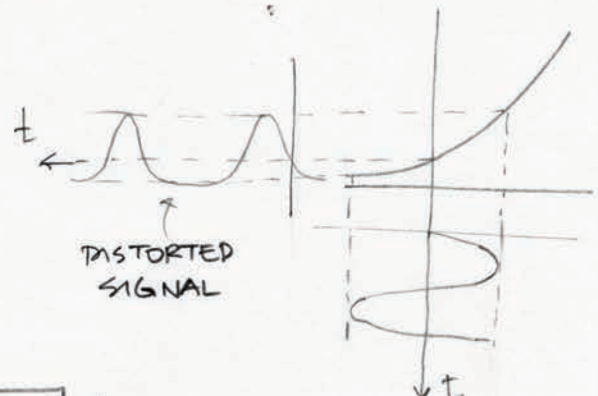
Method 1: Analytical

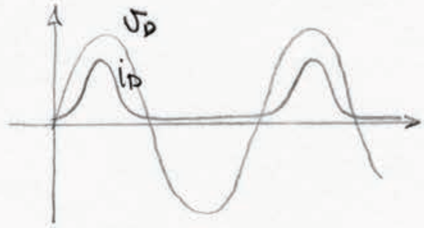
Method 2, Graphical

Method 3: Piecewise linear



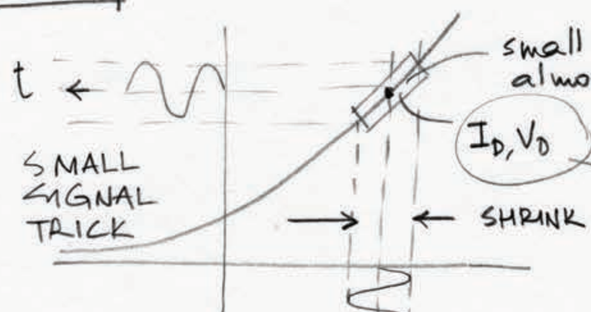
Incremental Analysis: Small Signal Method

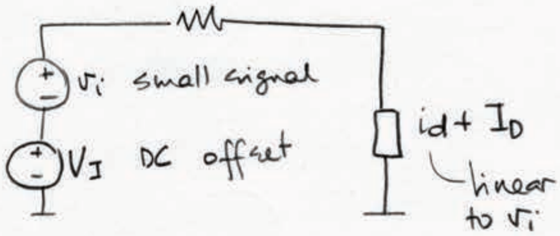




LECTURE 7

INCREMENTAL ANALYSIS

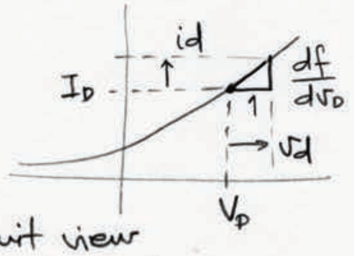




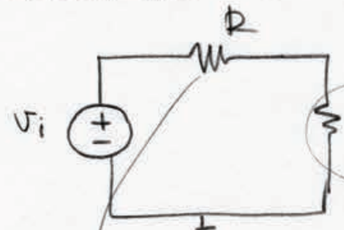
$$i_D = f(V_D) + \underbrace{\left.\frac{df(V_D)}{dv_D}\right|_{v_D = V_D}}_{\text{constant w.r.t. } \Delta v_D} \cdot \Delta v_D + \ldots \text{neglect}$$

$$\underset{I_D}{\overset{\|}{}} \quad + \quad G \cdot v_i$$

SLOPE at I_D, V_D



Circuit view

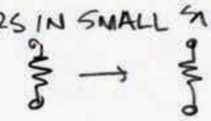


small signal circuit

$$R = \frac{1}{df/dv_D|_{v_D = V_D}}$$

resistor like behaviour

RESISTORS IN SMALL SIGNAL CIRCUIT

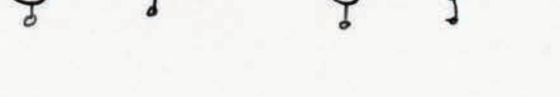


still the same

SMALL CIRCUIT METHOD

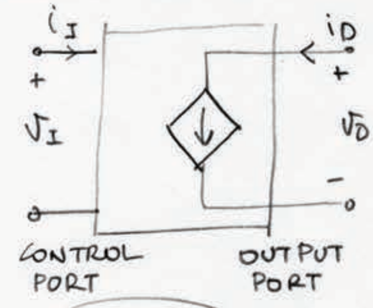
1. Find BIAS point (large signal anal)
2. Develop linearized model for each element at BIAS
3. Solve linear circuit

SOURCES IN SMALL SIGNAL CIRCUIT



TOPOLOGY OF THE CIRCUIT REMAINS THE SAME !!!
JUST REPLACE THE ELEMENTS

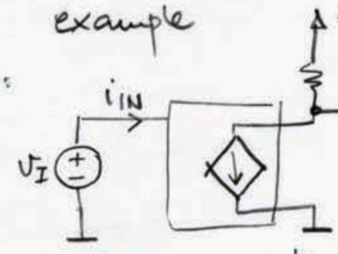
LECTURE 8 — DEPENDENT SOURCES & AMPLIFIERS



VCCS Voltage Controlled Current Source $i_D = f(v_I)$

CCCS $i_D = f(i_I)$ CCVS, VCVS so on so forth

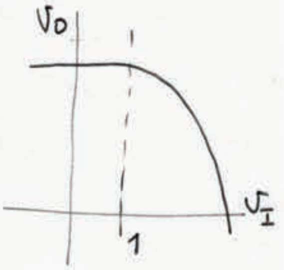
example



$$i_D = \frac{k}{2}(v_{IN}-1)^2 \quad v_{IN} \geq 1$$
$$i_D = 0 \quad v_{IN} < 1$$

vi naught

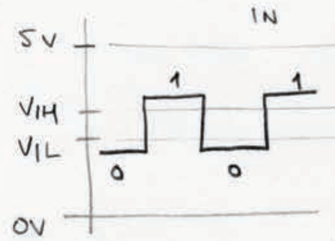
$$v_O = V_S - i_D \cdot R_L = \begin{cases} V_S - \frac{k}{2}(v_{IN}-1)^2 \cdot R_L & v_{IN} \geq 1 \\ V_S & v_{IN} < 1 \end{cases}$$

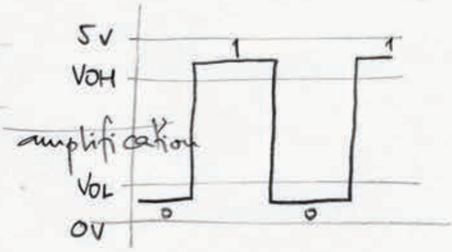


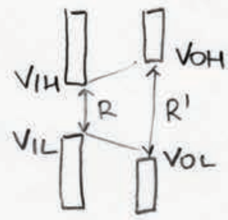
SUPERPOSITION WITH DEPENDENT SOURCES

- Leave all dependent sources
- Solve for one independent source at time

AMPLIFIERS : key to noise immunity

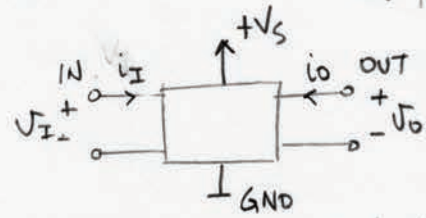


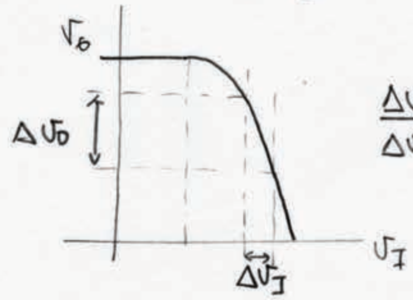




Minimum amplific. required

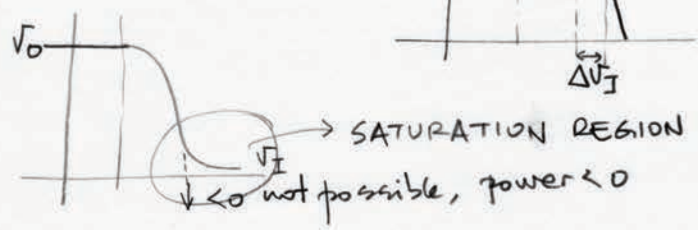
$$\frac{R'}{R} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$





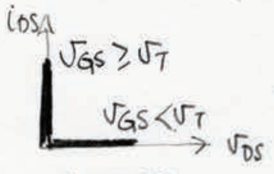
$$\frac{\Delta v_O}{\Delta v_I} \geq 1 \text{ amplification}$$

VCCS real behaviour

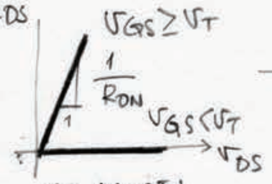


LECTURE 9 — MOSFET SCS MODEL & AMPLIFIER

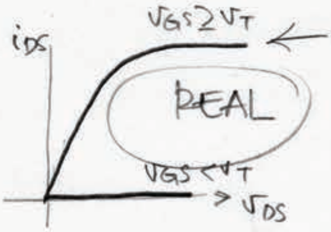
Real MOSFET behaviour



S MODEL



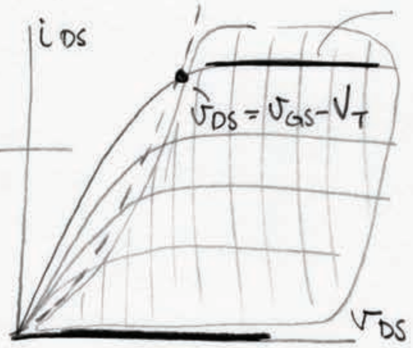
SR MODEL



$v_{DS} = v_{GS} - v_T$

SWITCH CURRENT SOURCE

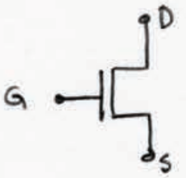
SCS Model



SATURATION REGION

$v_{GS1} > v_{GS2} > v_{GS3} \ldots$

DEPENDEND CURRENT SOURCE LIKE

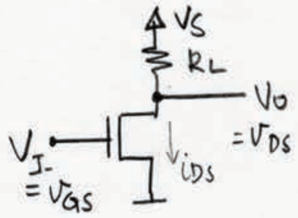


$v_{GS} < V_T$ OFF STATE

$v_{GS} \geq v_T$, $v_{DS} \geq v_{GS} - v_T$: $\quad i_{DS} = \frac{k}{2}(v_{GS} - V_T)^2$ VCCS !

SR Model → Digital designs CUTOFF = 0 TRIODE = 1

SCS Model → Analog designs



$i_D = \frac{k}{2}(v_I - V_T)^2 \qquad v_0 = V_S - i_D R_L$

only in saturation region

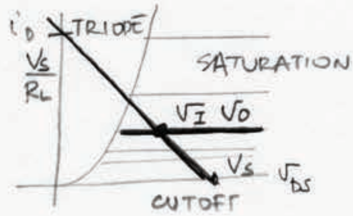
SATURATION REGION DISCIPLINE: $\quad v_{GS} = v_I \geq v_T$

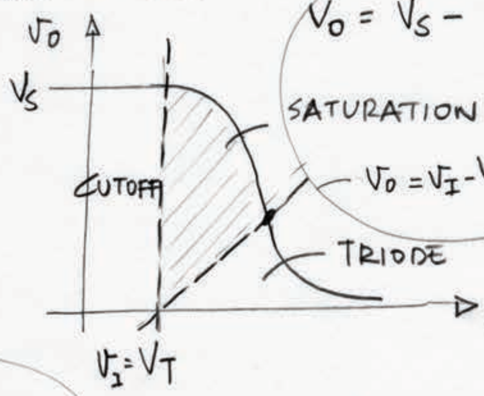
$v_{DS} = v_0 \geq v_{GS} - V_T = v_I - V_T$

SMALL SIGNAL ANALYSIS

(1) LARGE SIGNAL: DC BIAS

$$V_O = V_S - \frac{k}{2}(V_I - V_T)^2 \cdot R_L$$

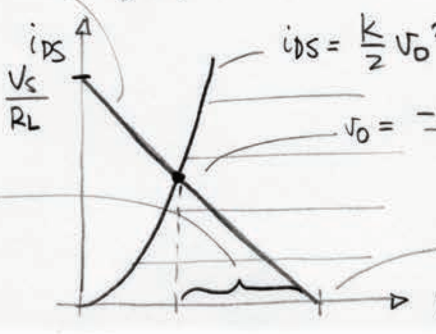




SOLVE FOR V_O

load line

$i_{DS} = \frac{V_S}{R_L} - \frac{V_O}{R_L}$



$i_{DS} = \frac{k}{2} V_O^2$

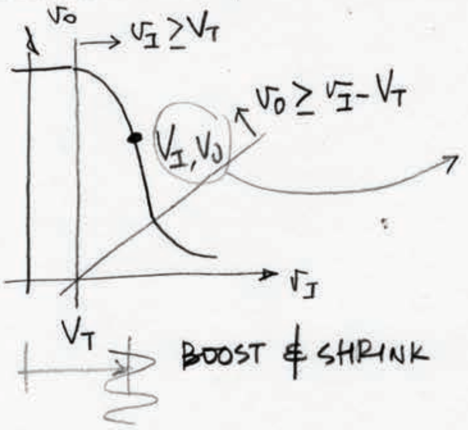
$$V_O = \frac{-1 + \sqrt{1 + 2kR_L V_S}}{kR_L}$$

$V_O = V_S$

valid region for saturation discipline

LECTURE 10

AMPLIFIERS . REVISITING SMALL SIGNAL TRICK



$$v_O = V_S - \frac{k}{2}(v_I - V_T)^2 \cdot R_L$$

① Find BIAS operating point

② Linearize $\quad v_I = V_I + v_i$

$$v_O = V_S - \frac{k}{2}(V_I + v_i - V_T)^2 \cdot R_L =$$

$$= \underbrace{V_S - \frac{k}{2}(V_I - V_T)^2 R_L}_{V_O} - k(V_I - V_T) R_L \cdot v_i - \cancel{\frac{k}{2} v_i^2 R_L}$$

NEGLECT

$$v_{OUT} = -\underbrace{k(V_I - V_T)}_{g_m} \cdot R_L \cdot v_i$$

g_m — transconductance

OTHER WAY :

$$\left.\frac{dv_O}{dv_I}\right|_{v_I = V_I}$$

$$A = g_m \cdot R_L \qquad v_O = -A v_i$$

LECTURE 11

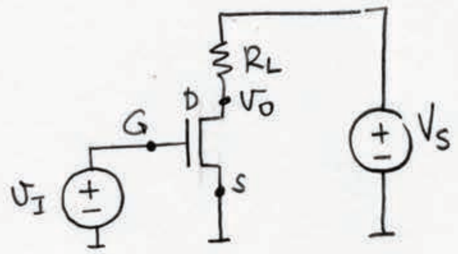
SMALL SIGNAL CIRCUITS

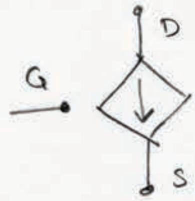
from lecture 7

① Find BIAS point

② Linearize elements, topology remains

③ Solve linear circuit



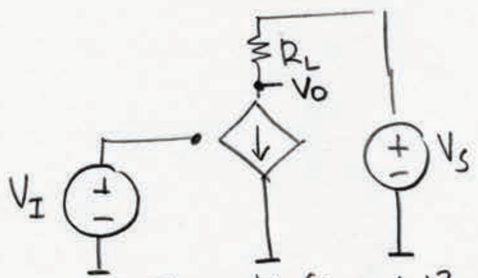


$$i_{DS} = \frac{k}{2}(v_{GS} - V_T)^2 = f(v_{GS})$$

$$i_{ds} = \left.\frac{\partial f}{\partial v_{GS}}\right|_{v_{GS} = V_{GS}} \cdot v_{gs} = k(V_{GS} - V_T) \cdot v_{gs}$$

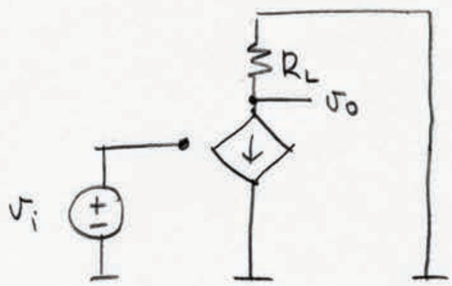
$k(V_{GS} - V_T) = g_m$ transconductance

LARGE SIGNAL



$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2$$

SMALL SIGNAL



$$i_{ds} = g_m \cdot v_{gs}$$

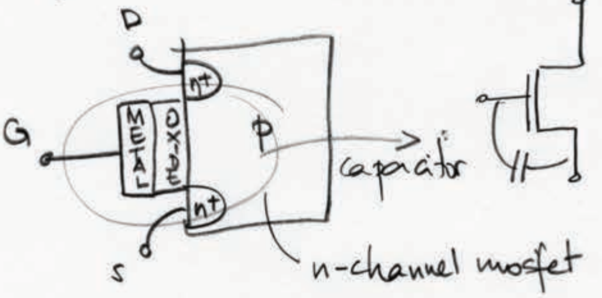
$$v_o = -i_{ds} \cdot R_L = -g_m \cdot R_L \cdot v_{gs}$$

$v_{gs} = v_i \to$ only for this case

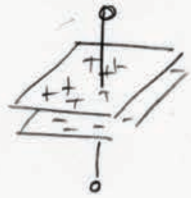
$$= -A \cdot v_i$$

LECTURE 12 — CAPACITORS & FIRST ORDER CIRCUITS

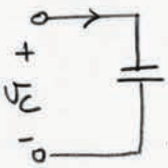
Physical Structure of a MOSFET



Linear Capacitor



$$C = \frac{\epsilon A}{d}$$



$$q = C \cdot v$$

$$i = C \cdot \frac{dv}{dt}$$

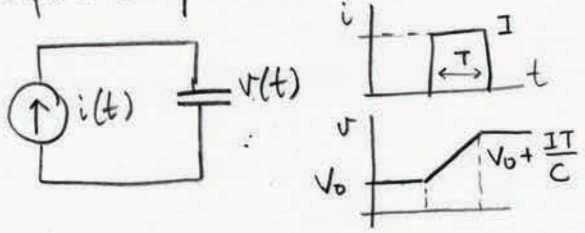
$$v = \frac{1}{C}\int_{-\infty}^{t} i\, dt$$

Energy / Memory

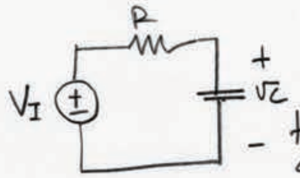
$$P = v \cdot i = C \cdot v \cdot \frac{dv}{dt} = \frac{d}{dt}\left(\frac{1}{2} C v^2\right)$$

energy

Capacitor & Current Source



RC Circuit



$$\frac{v_C - V_I}{R} + C \cdot \frac{dv_C}{dt} = 0$$

$$RC \frac{dv_C}{dt} + v_C = V_I$$

time constant

$$v_C = (V_0 - V_I)\, e^{-t/RC} + V_I = V(0)\, e^{-t/RC} + V(+\infty)\left(1 - e^{-t/RC}\right)$$