between the input and the output parts of the circuit, in the sense that the output resistor R_L can be changed by many orders of magnitude, with a corresponding orders-of-magnitude change in output current, but the output voltage and the input current will be virtually unchanged. This isolation is referred to as *buffering*.

15.3.5 AN ADDITIONAL CONSTRAINT: $v^+ - v^- \simeq 0$

In all preceding Op Amp calculations, we have made an approximation that because the so-called loop gain in the denominator is much bigger than one, the "one" term can be neglected. This approximation is almost always valid in Op Amp calculations. It is the factor 1+ (loop gain) that determines how insensitive the circuit is to changes in the Op Amp gain constant A (see Equation 15.17, for example), hence large loop gain is clearly a desirable design goal. If the loop gain is almost always going to be large, it seems a bit clumsy (although clearly correct) to make the circuit calculations without taking this fact into account until the last line. One would hope that with some hindsight, it might be possible to make the "large loop gain" assumption at the start of the circuit calculation, thereby simplifying the math. Let us re-examine the circuit of Figure 15.8b with this in mind.

We know that for most Op Amps, A will be 100,000 or larger, and the maximum allowed v_o will be about 12 V (see Figure 15.3c). Hence the largest value of $(v^+ - v^-)$ for linear operation will be around 120 mV, a voltage orders-of-magnitude smaller than either the input or the output voltage. On this basis it is reasonable to assume, as before, $i^+ \simeq 0$, and $i^- \simeq 0$, but *include an additional constraint*:

$$v^+ - v^- \simeq 0. \tag{15.19}$$

Not equal to zero, just small compared to other circuit voltages. When these three constraints are applied to the circuit in Fig 15.8b, we find

$$v^+ = 0$$

$$v^- \simeq 0.$$

Hence KCL at the v^- node yields

$$\frac{v_i}{R_a} + \frac{v_o}{R_b} \simeq 0 \tag{15.20}$$

(compare with Equation 15.10). Solving for v_o, we find

$$v_o \simeq -\frac{R_b}{R_a} v_i \tag{15.21}$$

as before, except this time the calculation is much simpler, because the combined constraints of approximately zero voltage and approximately zero current are quite powerful. For the non-inverting circuit of Figure 15.7, for example, we can write, using the voltage-divider relation,

$$v_i = v^+ \simeq v^- = \frac{R_2}{R_1 + R_2} v_o. \tag{15.22}$$

Hence

$$v_o \simeq \frac{R_1 + R_2}{R_2} v_i \tag{15.23}$$

as before. The voltage constraint of Equation 15.19 is also called the *virtual ground constraint*,[2] and can be interpreted in physical terms by noting that the output of a circuit with negative feedback must adjust itself to *force* $(v^+ - v^-)$ to be nearly zero, because that nearly-zero voltage is in turn multiplied by 100,000 to become the output voltage.

The $v^+ - v^- \simeq 0$ constraint can be applied only if the Op Amp is not saturated and the feedback is negative; that is, the net feedback signal comes from the output back to the negative input terminal.

15.4 INPUT AND OUTPUT RESISTANCES

15.4.1 OUTPUT RESISTANCE, INVERTING OP AMP

Negative feedback has a profound effect on the Thévenin-equivalent input and output resistances of circuits. To illustrate, we calculate first the Thévenin output resistance of the simple inverting Op Amp assumed to be operating in the active (non-saturated) region, that is, the circuit in Figure 15.8b. Obviously if we model the Op Amp by the ideal Op Amp model, the Thévenin output resistance is by definition zero, with or without feedback. So to show any effect, we must use a more accurate device model that includes some finite resistance in series with the dependent source, as in Figure 15.11. One way of calculating the Thévenin output resistance is to apply a test current i_t, at the output terminals, as shown in Figure 15.11, and calculate the resulting voltage v_t, when all other *independent sources*, in this case v_i, are set to zero.

2. Or more accurately, the *virtual short constraint*, or the *virtual node constraint*, since the inverting and non-inverting inputs need not always be at ground potential.

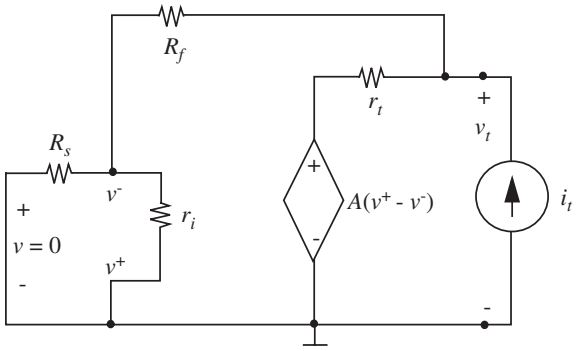


FIGURE 15.11 Calculation of output resistance.

In calculating the Thévenin resistance do *not* casually set dependent sources to zero, as their value is dictated by some other variable in the circuit which may or may not be zero.

The calculation of v_t is straightforward. We use the node method with conductances in place of resistances for convenience. In other words, we use $g_i = 1/r_i$, $G_s = 1/R_s$, $G_f = 1/R_f$, and $g_t = 1/r_t$. Applying KCL at the nodes with unknown node voltages, we get the following three independent equations:

$$v^+ = 0 \tag{15.24}$$

$$v^- = \frac{G_f}{G_f + G_s + g_i} v_t \tag{15.25}$$

$$i_t + \left[A\left(v^+ - v^-\right) - v_t\right] g_t + \left(v^- - v_t\right) G_f = 0. \tag{15.26}$$

$$\tag{15.27}$$

To simplify the mathematics, we now assume for this calculation that r_i is infinite ($g_i = 0$), because it is always much larger than R_s or R_f. Now, eliminating v^+ and v^- from Equation 15.26,

$$\frac{i_t}{v_t} = G_o = \frac{AG_f g_t}{G_f + G_s} + g_t + \frac{G_f G_s}{G_f + G_s}. \tag{15.28}$$

Thus the output conductance is the sum of three conductances. The first term is the effect of the feedback, the second term is the output conductance of the Op Amp alone, and the third term in resistance notation is $R_f + R_s$, hence is the effect of the feedback resistors in the absence of the Op Amp. For large A, this last term is not important, so the Thévenin output conductance with

feedback is

$$\frac{i_t}{v_t} = G_o \simeq g_t \left[1 + \frac{AG_f}{G_f + G_s} \right] \tag{15.29}$$

or, in more familiar terms

$$G_o \simeq g_t \left[1 + A \frac{R_s}{R_s + R_f} \right]. \tag{15.30}$$

Hence the Thévenin output resistance of the circuit is

$$R_o \simeq \frac{r_t}{1 + A\frac{R_s}{R_s+R_f}}. \tag{15.31}$$

For large loop gain

$$R_o \simeq \frac{r_t}{A\frac{R_s}{R_s+R_f}}. \tag{15.32}$$

The Thévenin output resistance r_t for the Op Amp alone, without feedback is typically of the order of 1000 ohms, so for large A and reasonable R_s and R_f, the overall Thévenin output resistance R_o for this topology circuit is a fraction of an ohm.

Equation 15.31 is in fact a general result. For any linear circuit in which the feedback resistor is sampling the output *node voltage* (rather than the output current), the Thévenin equivalent output resistance with feedback is equal to the output resistance without feedback, divided by a factor 1+ (loop gain), the same factor involved in gain calculations and calculation of sensitivity to changes in the gain constant A.

15.4.2 INPUT RESISTANCE, INVERTING CONNECTION

To calculate the Thévenin-equivalent input resistance of the inverting Op Amp circuit, we apply a test source at the input, and measure the resulting response. (There are no internal independent sources to be set to zero.) In Figure 15.12 we have chosen to drive with a test voltage v_t, and calculate the resulting current i_t. As before, it is equally valid to apply a test current source, and calculate the resulting voltage. The calculations are greatly simplified if the circuit topology is taken into account. The input consists of two elements in series: the resistor R_s, and a complicated circuit that will reduce to the Thévenin-equivalent input resistance of the rest of the Op Amp circuit. Recognizing this, we can first calculate the resistance *to the right of* the R_s (just set R_s to zero in Figure 15.12)

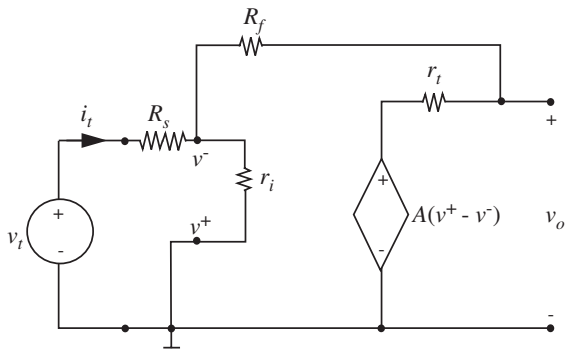


FIGURE 15.12 Input resistance calculation.

and then add R_s to this calculated value to get the complete answer. We will denote the resistance of the Op Amp circuit to the right of R_s as R_i, and the complete input resistance, including resistor R_s, as R_i'.

Because we chose a test voltage, and R_s is zero for now, the control variable is directly constrained:

$$v^+ = 0 \tag{15.33}$$

$$v^- = v_t. \tag{15.34}$$

Now apply KCL at the input node:

$$i_t = \frac{v_t}{r_i} + \frac{v_t - A(v^+ - v^-)}{R_f + r_t}. \tag{15.35}$$

hence

$$\frac{i_t}{v_t} = G_i = \frac{1}{r_i} + \frac{1}{R_f + r_t} + \frac{A}{R_f + r_t}. \tag{15.36}$$

Again we have the sum of three conductances. So the corresponding resistance expression, the Thévenin input resistance for the circuit, is the parallel combination of three terms:

$$R_i = r_i \parallel (R_f + r_t) \parallel \left(\frac{R_f + r_t}{A}\right) \tag{15.37}$$

the Op Amp input resistance, the feedback resistor plus Op Amp output resistor, and an effective resistance generated by the feedback. For large A,

$$R_i \simeq \frac{R_f + r_t}{A} \tag{15.38}$$

that is, we expect the input resistance to be *very low*. For example, for a typical case of $R_f = 10$ kΩ, $r_t = 1000$ Ω, $A = 10^5$, the input resistance measured at the v^- terminal will be 0.1 ohm. Simple physical reasoning serves to support this result. If we imagine applying a small voltage to the input, say 0.1 mV, then the Op Amp will immediately drive v_o to -A times 0.1 mV, or -10 volts. So resistor R_f has a large voltage across it, hence a large current will flow. This large current must come from the input source, and is 10^5 times as large as one might expect for such a small input voltage. Large current for small voltage means the effective input resistance will be very small, in fact roughly the feedback resistor R_f divided by A.

In accordance with our initial assumptions, the complete input resistance of the inverting Op Amp, including resistor R_s, is

$$R_i' = R_i + R_s \tag{15.39}$$

as can be verified by calculating the input resistance directly from Figure 15.12 including R_s. Because R_i is so small,

$$R_i' \simeq R_s. \tag{15.40}$$

15.4.3 INPUT AND OUTPUT R FOR NON-INVERTING OP AMP

The active-region output resistance of the non-inverting Op Amp circuit can be calculated in much the same way as for the inverting circuit. We set the *independent* source to zero and apply a test current source to the output terminals, as shown in Figure 15.13. Now calculate v_t. As usual, we apply the node method to find three independent equations. First find expressions for v^+ and v^-, and then write KCL at the output node. Again we assume r_i is much larger than R_2 to simplify the math:

$$v^+ = 0 \tag{15.41}$$

$$v^- = v_t \frac{R_2}{R_1 + R_2} \tag{15.42}$$

$$i_t - \frac{v_t}{R_1 + R_2} - \frac{v_t - A(v^+ - v^-)}{r_t} = 0. \tag{15.43}$$

Hence

$$\frac{i_t}{v_t} = G_o = \frac{1}{R_1 + R_2} + \frac{1}{r_t} + \frac{AR_2/(R_1 + R_2)}{r_t}. \tag{15.44}$$

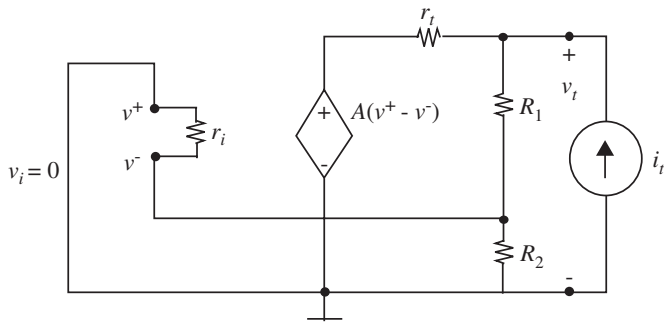


FIGURE 15.13 Output resistance calculation, non-inverting circuit.

For large A and reasonable R_1 and R_2,

$$R_o \simeq \frac{r_t}{AR_2/(R_1 + R_2)}. \tag{15.45}$$

This is the Thévenin output resistance r_t of the Op Amp alone, divided by the loop gain, or, more accurately, from Equation 15.44, 1 + (loop gain). As before, the output resistance is *very low*.

The input resistance for the active (nonsaturated) region can be found from the circuit in Figure 15.14. As before, we need expressions for v^+ and v^-, and a KCL equation involving i_t:

$$v^+ = v_t \tag{15.46}$$

$$v^- = v_t - i_t r_i. \tag{15.47}$$

KCL at Node 1 yields

$$i_t + \frac{A(v^+ - v^-) - v^-}{R_1 + r_t} - \frac{v^-}{R_2} = 0. \tag{15.48}$$

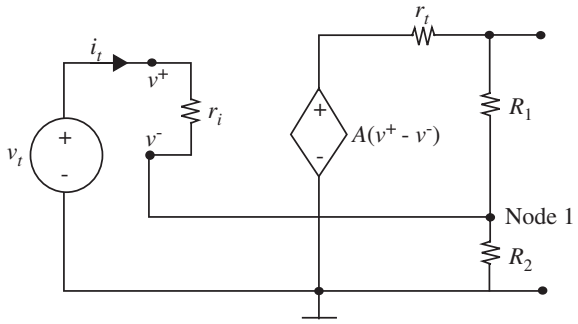


FIGURE 15.14 Input resistance calculation, non-inverting Op Amp.

Substituting and solving, assuming A is large, we find

$$R_i = \frac{v_t}{i_t} \simeq r_i \left[\frac{AR_2}{R_1 + r_t + R_2} \right]. \tag{15.49}$$

This expression shows that for the non-inverting connection, the effective input resistance in the active region is *very high*, (roughly the Op Amp input resistance r_i multiplied by the loop gain) in contrast to the result for the inverting case, Equation 15.38. Reasoning physically, if we apply a voltage v_t at the input, the output voltage adjusts itself so that v^- is very nearly equal to v_t, so there is very little voltage across r_i, hence much less current flowing in it than we might expect. Hence the circuit input resistance is large. This property enables the non-inverting connection to be particularly useful in buffering applications.

This point of view suggests an alternative approach to the calculation. If we assume at the outset that $v^+ - v^- \simeq 0$, then

$$v_t \simeq A(v^+ - v^-) \frac{R_2}{R_2 + R_1 + r_t}. \tag{15.50}$$

But $v^+ - v^-$, although small, must not be zero for finite r_t:

$$v^+ - v^- = i_t r_i. \tag{15.51}$$

When Equation 15.51 is substituted into Equation 15.50, we find R_i as before (Equation 15.49).

WWW 15.4.4 GENERALIZATION ON INPUT RESISTANCE *

15.4.5 EXAMPLE: OP AMP CURRENT SOURCE

We have shown that both the inverting and non-inverting Op Amp connections have very low output resistance, that is, they approximate ideal voltage sources. But in some circuit applications, we may want the Op Amp to look like a current source, that is, we want a very *high* output resistance. It follows from the discussion at the end of Section 15.4.1 that such a design can be realized by a change in the *topology of the output circuit.*

In the two circuits already discussed, the feedback network sends a signal back to the negative input terminal that is proportional to the *output voltage* v_o. Thus the circuit tends to stabilize this variable, thereby creating a voltage source. By analogy, to make a current source, we must arrange to feed back a signal proportional to the *output current* flowing in the circuit being driven by the Op Amp. One possible topology is shown in Figure 15.15a. The circuit looks, at first glance, like the non-inverting connection shown in Figure 15.15b,

but there is an important difference. In the new topology, the resistor R_L we are trying to drive is now part of the voltage divider feedback network. Thus in Figure 15.15a we are using the resistor R_s to *sample the current through* R_L, whereas in Figure 15.15b R_1 and R_2 sample the *voltage across* R_L. The distinction seems trivial until we think in terms of R_L varying in value, or even being nonlinear. Then it is clear that there is a fundamental difference in the two topologies.

Once the topological issues are understood, the circuit analysis is trivial. Assuming $v^+ \simeq v^-$, we note from Figures 15.15a or 15.15c

$$v^+ = v_i \tag{15.52}$$

$$v^- = i_L R_s \tag{15.53}$$

$$v^+ \simeq v^-. \tag{15.54}$$

Therefore

$$i_L \simeq \frac{v_i}{R_s} \tag{15.55}$$

independent of the value of R_L.

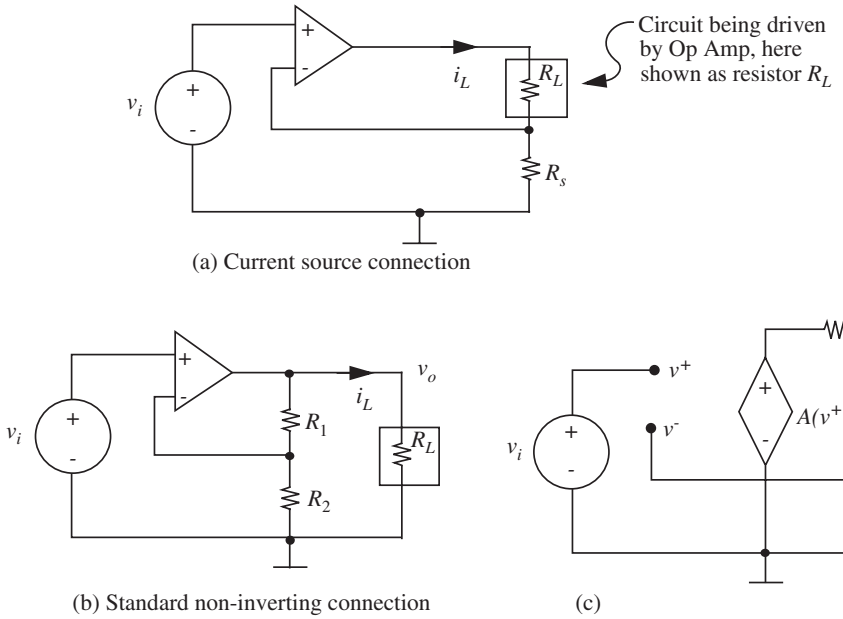


FIGURE 15.15 Op Amp current source.

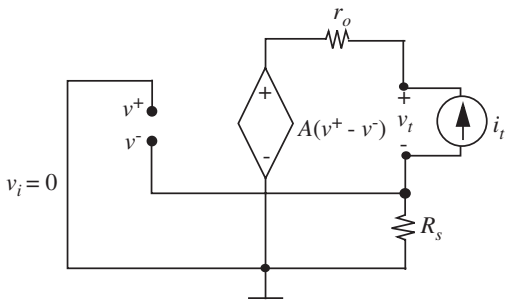


FIGURE 15.16 Output resistance of current source.

The fact that the current through R_L is independent of the value of R_L suggests that the Op Amp circuit looks like a current source. It is a simple matter to verify this more formally: Replace R_L by a test source, and find the Thévenin output resistance of the circuit. In this case we choose a test current source i_t, as in Figure 15.16:

$$v^- = -i_t R_s \tag{15.56}$$

$$v^+ = 0 \tag{15.57}$$

$$v_t = A(v^+ - v^-) + i_t r_o - v^- \tag{15.58}$$

$$= (1 + A) i_t R_s + i_t r_o \tag{15.59}$$

$$R_o = \frac{v_t}{i_t} = (1 + A) R_s + r_o. \tag{15.60}$$

For reasonable circuit parameters, R_o could well be many megohms.

Again these results can be generalized to summarize the effect of negative feedback on the effective output resistance of a circuit. If the Op Amp, the load resistor R_L and the feedback network appear to be connected in series, in a loop, hence sharing a common current, then the output resistance will be high. If the Op Amp, R_L, and the feedback circuit all appear to be in parallel, tied to a common node, sharing a common voltage, then the output resistance will be low.

15.5 ADDITIONAL EXAMPLES

This section contains a number of examples of Op Amp circuits. They are intended both to illustrate the versatility of the Op Amp as a circuit design building block and to serve as a review and extension of analysis techniques introduced earlier in this chapter.

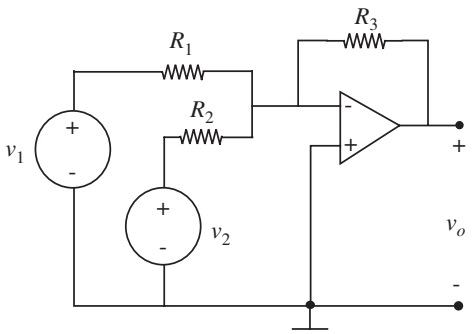


FIGURE 15.17 Adder.

15.5.1 ADDER

An Op Amp circuit for adding two signals together is shown in Figure 15.17. If we assume $v^+ \simeq v^-$, then application of KCL to the v^- node yields

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_o}{R_3} \simeq 0. \tag{15.61}$$

Therefore

$$v_o \simeq -\left(\frac{R_3}{R_1}v_1 + \frac{R_3}{R_2}v_2\right), \tag{15.62}$$

which represents the weighted sum of the two input signals.[3] Note that within the accuracy of the voltage constraint $v^+ - v^- \simeq 0$, the two input signals do not cross-couple; that is, no current from v_2 flows in R_1, and vice versa. Thus the circuit is an *ideal adder*.

15.5.2 SUBTRACTER

If we wish to take the difference between two signals, then the circuit of Figure 15.18 is appropriate. Direct application of superposition to the *independent sources* yields the two subcircuits shown in Figures 15.18b and 15.18c. In Figure 15.18b, source v_2 has been set to zero. On the assumption of $i^+ \simeq 0$, there will be no current through R_3 and R_4, so $v^+ \simeq 0$, and the topology is seen to be that of an inverting amplifier. Hence

$$v_{oa} = -\frac{R_2}{R_1}v_1. \tag{15.63}$$

3. Because the Op Amp model is linear, the same result can be derived using superposition.

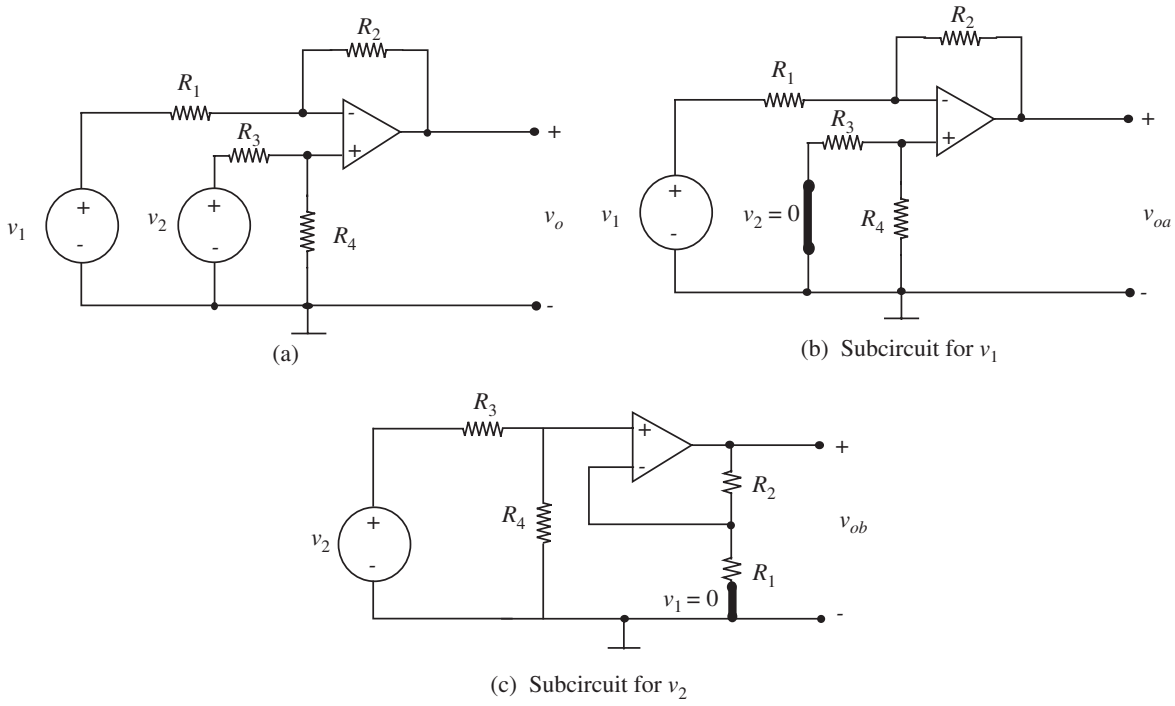


FIGURE 15.18 Subtracter.

When source v_1 is set to zero, and the circuit slightly rearranged, the non-inverting topology emerges, with a voltage divider at the input, as indicated in Figure 15.18c. Hence

$$v_{ob} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)v_2. \tag{15.64}$$

The total output voltage is the sum of the two voltages v_{oa} and v_{ob}. To make a subtracter, the resistor ratios in Equations 15.63 and 15.64 should be equal. This can be achieved by setting $R_3 = R_1$ and $R_4 = R_2$. Then

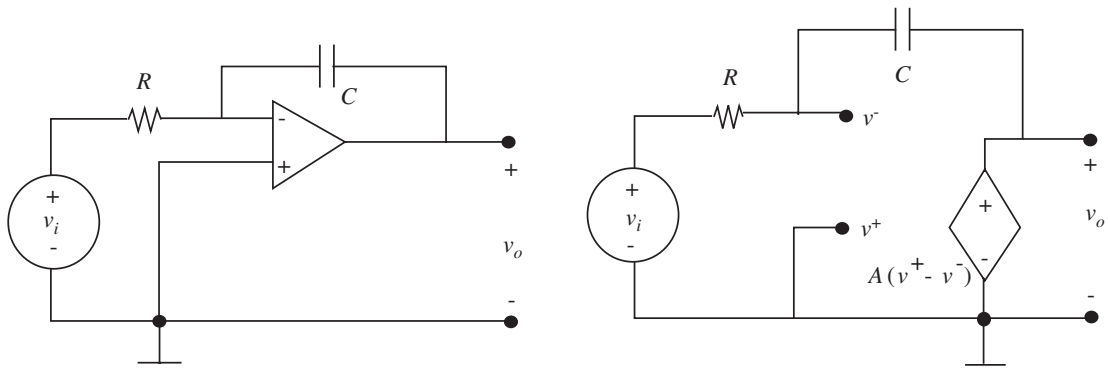
$$v_o = \frac{R_2}{R_1}(v_2 - v_1). \tag{15.65}$$

Now v_o is proportional to the difference between the two input voltages.

15.6 OP AMP RC CIRCUITS

15.6.1 OP AMP INTEGRATOR

The circuit in Figure 15.19 gives a much closer approximation to ideal integration than the simple RC circuits discussed in Chapter 10. The analysis to



(a) Circuit (b) Active region subcircuit

FIGURE 15.19 Op Amp Integrator.

show this is quite straightforward. Assuming linear-region operation, we replace the Op Amp by the dependent-source model, as in Figure 15.19b, and analyze the resulting linear circuit using the node method. KCL at the v^- node yields

$$\frac{v_i - v^-}{R} + \frac{Cd(v_o - v^-)}{dt} = 0. \tag{15.66}$$

If we assume at the outset that the Op Amp gain A is large enough to ensure that

$$v^+ \simeq v^- \tag{15.67}$$

then because $v^+ = 0$, Equation 15.66 reduces to

$$\frac{v_i}{R} + \frac{Cdv_o}{dt} \simeq 0 \tag{15.68}$$

or,

$$v_o \simeq -\frac{1}{RC}\int v_i dt. \tag{15.69}$$

That is, the circuit calculates the (negative) integral of the input voltage.

A more exact calculation involves substituting the Op Amp equation:

$$v_o = A(v^+ - v^-) \tag{15.70}$$

into Equation 15.66, again noting $v^+ = 0$:

$$\frac{v_i}{R} - \frac{v^-}{R} - CA\frac{dv^-}{dt} - C\frac{dv^-}{dt} = 0. \tag{15.71}$$

Hence

$$RC(1 + A)\frac{dv^-}{dt} + v^- = v_i. \tag{15.72}$$

The effective time constant of the circuit (by analogy with Equation 10.150, for example) is

$$\tau = (1 + A)RC. \tag{15.73}$$

Thus the time constant associated with the passive elements alone is multiplied by the gain of the Op Amp. This is often referred to as the Miller Effect, originally in reference to the fact that a small input to output capacitance in early vacuum tubes seriously limited the frequency response of amplifier circuits. The time constant can be made very large for modest component values. For example, if the RC time constant is 1 second, and A is 10^5 or greater, the effective circuit time constant in measured in days. On this time scale almost any waveform lasting for less than a minute or so will seem like a "short pulse." Thus the analysis of Section 10.6.3 is applicable, and on the time scale of minutes, the circuit acts like an integrator.

The ultimate test of an integrator is to apply a small voltage step, V, and see how closely the integrator output conforms to a ramp. From Equations 15.70 and 15.72,

$$(1 + A)RC\frac{dv_o}{dt} + v_o = -AV. \tag{15.74}$$

For v_i a small fixed value V after $t = 0$, v_o will follow the usual exponential charging curve toward $(-AV)$, (see Equation 10.101, for example). That is,

$$v_o = -AV\left(1 - e^{-t/(1+A)RC}\right). \tag{15.75}$$

This curve is plotted in Figure 15.20 on the basis that the RC time constant (without the Op Amp) is roughly one second. Obviously on the time scale of minutes, the circuit looks like an almost-perfect integrator, provided, of course, the Op Amp is always operating in the active region.

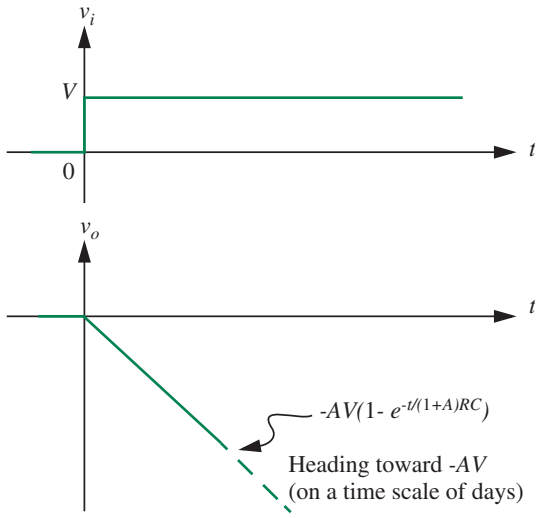


FIGURE 15.20 Waveforms of integrator.

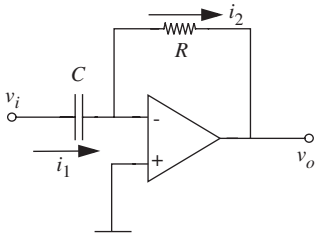


FIGURE 15.21 Differentiator circuit.

15.6.2 OP AMP DIFFERENTIATOR

The Op Amp differentiator shown in Figure 15.21 complements the integrator. Because $v^- \simeq v^+$ and $v^+ = 0$, we know that the current i_1 through the capacitor is given by:

$$i_1 = C\frac{dv_i}{dt}.$$

Since virtually no current flows into the Op Amp, $i_1 = i_2$, and therefore

$$v_o = -Ri_1.$$

Eliminating i_1 from the preceding two equations, we obtain

$$v_o = -RC\frac{dv_i}{dt}. \tag{15.76}$$

That is, this circuit calculates the (negative) time derivative of the input voltage.

Sample input and output waveforms for the differentiator are shown in Figure 15.22. For the square-pulse input shown, the outputs are a pair of spikes each at the time instant the input makes a transition. As illustrated in the example, the differentiator circuit is often used in detecting shape transitions in waveforms.

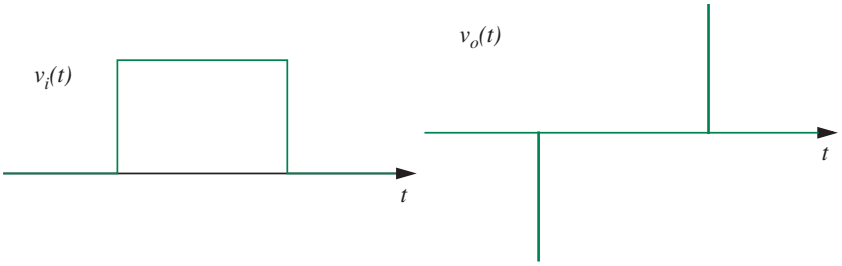


FIGURE 15.22 Differentiator waveforms.

15.6.3 AN RC ACTIVE FILTER

An Op Amp embedded in a more complicated RC circuit is shown in Figure 15.23a. This is an *RC active filter*, with all of the useful resonance properties of a capacitor-inductor circuit. To show this, we calculate the output voltage v_o in terms of v_i. First draw the linear-region circuit model with the dependent source, Figure 15.23b. Then write Node equations, taking current entering the node as positive. We assume at the outset $v^+ - v^- \simeq 0$. because v^+ is zero in this circuit, the appropriate constraint is $v^- \simeq 0$. For Node v_1,

$$(v_i - v_1)g_1 - C_1\frac{dv_1}{dt} + C_2\frac{d(v_o - v_1)}{dt} = 0 \qquad (15.77)$$

and for Node v^-

$$C_1\frac{dv_1}{dt} + v_o g_2 = 0. \qquad (15.78)$$

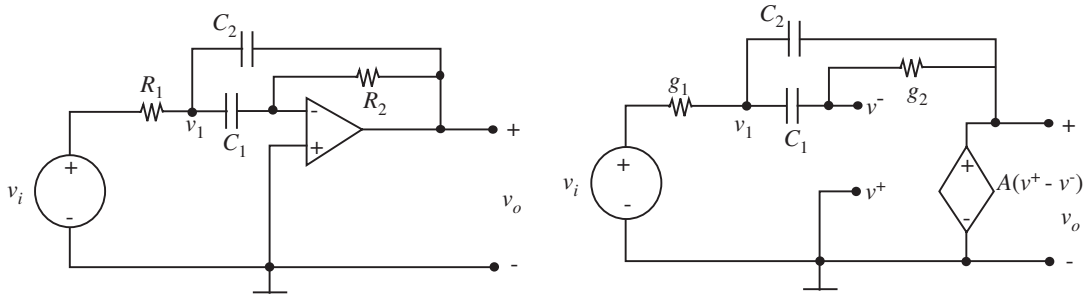


FIGURE 15.23 Op Amp RC active filter.

Hence

$$v_i g_1 = g_1 v_1 + (C_1 + C_2)\frac{dv_1}{dt} - C_2\frac{dv_o}{dt} \tag{15.79}$$

$$0 = C_1\frac{dv_1}{dt} + v_o g_2. \tag{15.80}$$

These equations can be solved by taking the derivative of both sides of both equations, and eliminating terms in v_1 and its derivative by substitution from Equation 15.80 and the derivative of Equation 15.80. By so doing we obtain a second order differential equation for v_o:

$$\frac{d^2 v_o}{dt^2} + g_2\frac{C_1 + C_2}{C_1 C_2}\frac{dv_o}{dt} + \frac{g_1 g_2}{C_1 C_2}v_o = -\frac{g_1}{C_2}\frac{dv_i}{dt}. \tag{15.81}$$

This equation is identical in form to that of an RLC resonator (see Equation 12.119), but this circuit contains no inductors. The effect of an inductor is created by an active element, in this case the Op Amp, and the capacitors, hence the name *RC active filter*. The advantages of an RC active filter (this is only one realization; there are many others) are that it can provide a power gain unlike an RLC network and that it does not require inductors. Because inductors are difficult to fabricate in VLSI technology, this is an important design advantage for integrated circuits. Furthermore, inductors are not very ideal elements, especially for low-frequency applications (for example, for frequencies below perhaps 100 kHz). Thus in this frequency range, resonant circuits are often built out of Op Amps, resistors, and capacitors.

The properties of filter circuits were explored previously in Chapters 10 and 13. As we did in Chapter 13, the circuit of Figure 15.23 can also be analyzed using the impedance method by using impedance values $1/sC_1$ and $1/sC_2$ for the capacitors (see Section 15.6.4). We will also see other examples of impedance based analysis for Op Amps later in this chapter.

Since Equation 15.81 is identical in form to Equation 12.119 for the RLC circuit, we can readily determine the behavior of our RC active filter. Notice that the output response v_o of the Op Amp RC active filter corresponds to the capacitor voltage v_C in Section 12.5. The equation corresponding to the series RLC circuit in Section 12.5 was

$$\frac{d^2 v_C}{dt^2} + \frac{R}{L}\frac{dv_C}{dt} + \frac{1}{LC}v_C = \frac{1}{LC}v_{\text{IN}} \tag{15.82}$$

with the damping factor $\alpha = R/2L$ and the undamped resonant frequency $\omega_o = 1/\sqrt{LC}$.

Thus, the corresponding damping factor in our Op Amp circuit is

$$\alpha = g_2 \frac{C_1 + C_2}{2C_1C_2} \tag{15.83}$$

and the undamped resonant frequency is

$$\omega_o = \sqrt{\frac{g_1 g_2}{C_1 C_2}}. \tag{15.84}$$

15.6.4 THE RC ACTIVE FILTER—IMPEDANCE ANALYSIS

Let us analyze the Op Amp active filter circuit of Section 15.6.3 for a sinusoidal drive. Since the Op Amp is a linear device (namely, a VCVS) we can use the impedance method for the analysis.

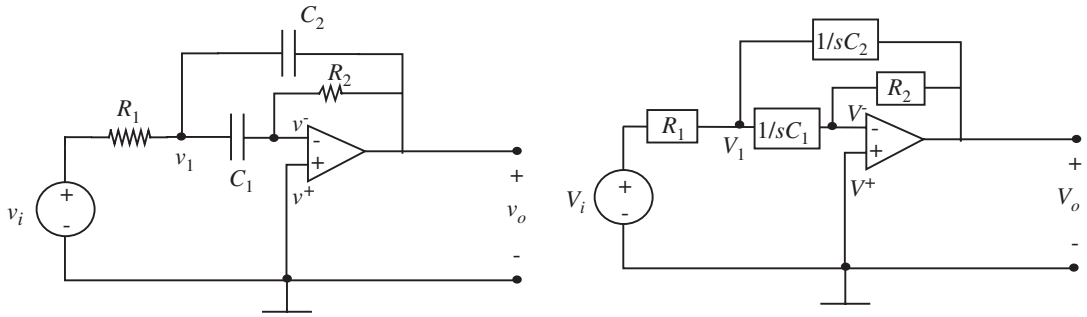
The circuit configuration is repeated in Figure 15.24a. The impedance model for the circuit is shown in Figure 15.24b. The circuit is sufficiently complicated that node analysis is advisable. At node V_1 assuming $v^+ \simeq v^-$,

$$(V_i - V_1)\, g_1 + (V_o - V_1)\, sC_2 - V_1 sC_1 = 0 \tag{15.85}$$

where $g_1 = 1/R_1$. At the V^- node,

$$V_1 sC_1 + V_o g_2 = 0 \tag{15.86}$$

where $g_2 = 1/R_2$.



(a) Circuit (b) Impedance model

FIGURE 15.24 RC active filter analysis using the impedance method.

Now V_o can be found by Cramer's Rule. First, rewrite with source terms on the left

$$V_i g_1 = V_1 \left[g_1 + s\left(C_1 + C_2\right)\right] - V_o s C_2 \tag{15.87}$$

$$0 = V_1 s C_1 + V_o g_2 \tag{15.88}$$

(These equations should be compared to the corresponding differential equations, Equations 15.79 and 15.80.) Solving for the complex amplitude V_o,

$$V_o = \frac{-g_1 s C_1 V_i}{\left[g_1 + s\left(C_1 + C_2\right)\right] g_2 + s^2 C_1 C_2} \tag{15.89}$$

$$= \frac{-g_1 s C_1 V_i}{g_1 g_2 + s\left(C_1 + C_2\right) g_2 + s^2 C_1 C_2} \tag{15.90}$$

$$= \frac{-s\left(g_1/C_2\right) V_i}{s^2 + s\frac{C_1+C_2}{C_1 C_2} g_2 + \frac{g_1 g_2}{C_1 C_2}}. \tag{15.91}$$

Equation 15.91 has exactly the form of Equation 14.19 (except for the minus sign), hence the circuit is equivalent to a parallel RLC filter. By comparing corresponding terms we find, as in Chapter 12,

$$\text{Resonant frequency} = \omega_o = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \tag{15.92}$$

$$\text{Bandwidth} = g_2 \frac{C_1 + C_2}{C_1 C_2}. \tag{15.93}$$

With these scaling factors, the frequency response plot of Figure 14.12 directly applies to this circuit (except for the additional 180° in the phase), along with all other properties discussed in Section 14.1.

WWW 15.6.5 SALLEN-KEY FILTER

15.7 OP AMP IN SATURATION

Thus far we have used the Op Amp in its active region. In the active region, the voltage-controlled voltage source model of the Op Amp shown in Figure 15.6 applies. Furthermore, when negative feedback is applied, and the Op Amp is operated in the active region, we can use the input voltage constraint given by $v^- \simeq v^+$. However, the voltage-controlled voltage source model and the input voltage constraint no longer apply when the Op Amp output reaches saturation. In saturation, the Op Amp output will be close to one of the power supply voltages, +12 or −12 V. In positive saturation, the output will be close to +12 V and in negative saturation the output will be close to −12 V.

The Op Amp exits the active region and enters the saturation region when the external inputs are such that the Op Amp output is required to go above +12 or below −12 V. As an example, suppose the Op Amp has power supply voltages of +12 and −12, then if two volts are applied as the input to a non-inverting Op Amp amplifier circuit with a gain of 10, the Op Amp will be driven into positive saturation. Similarly, if minus two volts are applied to the same amplifier, the Op Amp will be driven into negative saturation.

How do we model the Op Amp when it is in saturation? When an Op Amp enters positive saturation, a near-short circuit forms between the Op Amp output and the positive power supply. Similarly, when the Op Amp enters negative saturation, a near-short circuit forms between the Op Amp output and the negative power supply. Accordingly, simple positive and negative saturation models for the Op Amp are illustrated in Figure 15.28. The normal dependent voltage source is not shown in the saturation models because its output gets limited by the power supply voltages and so it turns into a simple voltage source.

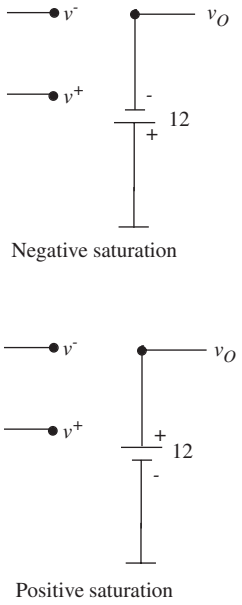


FIGURE 15.28 Op Amp model in saturation.

15.7.1 OP AMP INTEGRATOR IN SATURATION

If the Op Amp integrator in Figure 15.19 is driven into negative saturation, then the appropriate subcircuit is shown in Figure 15.29. Our negative saturation model for the Op Amp says that v_O is fixed at some voltage close to the negative power supply voltage, say −12 V. Because of the 12-V battery assumed at the output when the Op Amp is in saturation, the dependent source is no longer involved in the calculations, so the circuit reduces to a simple series RC configuration, as indicated in Figure 15.29b.

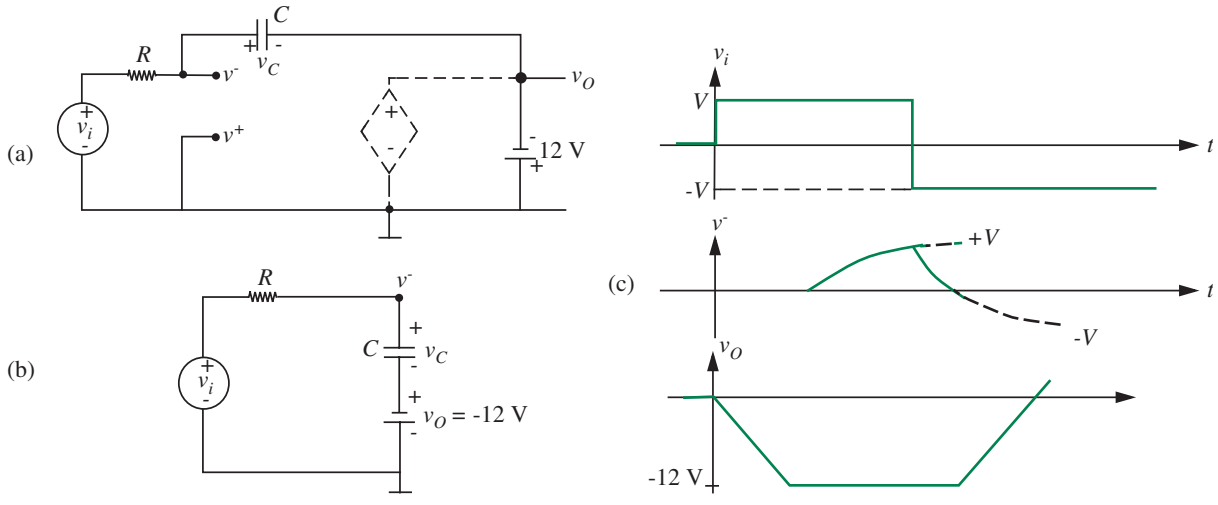


FIGURE 15.29 Integrator Op Amp in saturation.

Assuming a step input of v_i as in Figure 15.29c, the solution for v_C and v^- can be found by inspection using the methods of Section 10.5.3. The voltage across v_C at the instant before entering saturation is

$$v_{\text{init}} = +12\,\text{V} \tag{15.104}$$

because v^- at this point is almost zero due to the Op Amp constraint. If the transient went to completion, the final capacitor voltage would be

$$v_{\text{final}} = V + 12\,\text{V}. \tag{15.105}$$

Hence from Equation 10.62, assuming a time origin at the instant of entering saturation,

$$v_C = 12e^{-t/RC} + (V + 12)(1 - e^{-t/RC}) \tag{15.106}$$

$$= V(1 - e^{-t/RC}) + 12. \tag{15.107}$$

(This is a general result for fixed voltages in series with capacitors: By superposition such problems can be solved without the fixed voltage, then the fixed voltage can be added back in. In other words, the transient part is unaffected by the fixed voltage.) It follows that

$$v^- = V(1 - e^{-t/RC}) \tag{15.108}$$

(a result that an experienced analyst of RC circuits would have written down directly). Waveforms appropriate to these equations are shown in Figure 15.29c.

An important issue of circuit performance is how long it takes the circuit to recover from the effects of saturation. To this end, assume that the input step is now reversed in polarity. The Op Amp will still be held in saturation by the large positive voltage on the v^- terminal, and will remain in saturation until v^- has decayed virtually to zero. Figure 15.29b remains the appropriate circuit representation for this interval. Thus with $v_i = -V$,

$$v^- = -V + 2Ve^{-t/RC} \tag{15.109}$$

$$v_O = -12 \tag{15.110}$$

where the time origin is now defined to be at the instant of negative transition of v_i. Appropriate waveforms are shown in Figure 15.29c. As noted earlier, this saturation state persists until v^- has decayed almost to zero. Only then will the Op Amp come out of saturation, and integrate back toward zero, as shown in Figure 15.29c.

In summary, driving the Op Amp into saturation has two serious consequences on the performance of the integrator. First, the integration is truncated

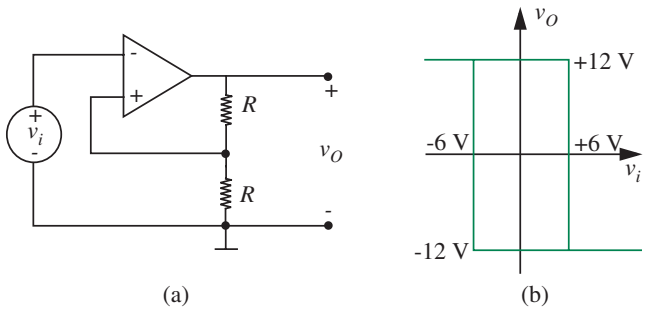


FIGURE 15.30 Positive feedback.

when the Op Amp saturates. Second, when the input wave goes negative, there is a substantial *delay* before the circuit recovers, and again acts as an integrator.

15.8 POSITIVE FEEDBACK

In every Op Amp circuit discussed thus far, the feedback network has been connected from the Op Amp output to the *negative* input terminal of the Op Amp. Such a connection provides *negative feedback*, which tends to make the circuit more linear, more temperature independent, more reliable. An obvious question: What happens if the feedback is connected to the *positive* input terminal, as in Figure 15.30a?

The complete relation between v_O and v_i, Figure 15.30b, shows both saturation and hysteresis. To understand the circuit action, assume that v_O is initially positive and v_i is negative. Then, because of the feedback, v^+ is still at +6.

To get the Op Amp out of saturation, v_i must be made positive enough to bring $(v^+ - v^-)$ approximately to zero, hence v_i must be approximately +6 volts. If v_i is slightly more positive than +6, v_O will be driven negative, whereupon v^+ will be driven negative, driving v_0 even more negative. Hence, v_O undergoes a regenerative negative transition to −12 V. Now v_i must be made more negative than −6 volts to initiate a regenerative transition to +12 V. the width of the hysteresis region can be controlled by the ratio of the feedback resistors.

The circuit is obviously no longer a linear amplifier: The positive feedback has enhanced rather than suppressed the basic nonlinearity of the unadorned Op Amp. One application of this circuit is as a digital comparator, to convert a continuous analog signal to a two-state signal.

15.8.1 RC OSCILLATOR

Shown in Figure 15.31 is another Op Amp circuit that uses positive feedback. Assume that the power supply voltages are V_S and $-V_S$. This circuit behaves as an oscillator, and uses positive feedback to saturate the Op Amp at both positive and negative values of V_S. Let's examine how this oscillator works.

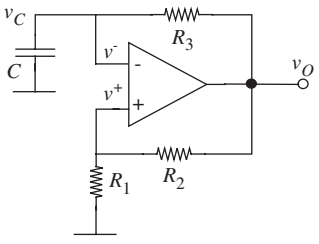


FIGURE 15.31 RC oscillator circuit.

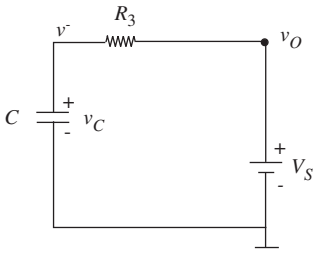


FIGURE 15.32 Equivalent circuit for the RC oscillator when the Op Amp is in positive saturation.

Let us first analyze the circuit qualitatively, referring to the waveforms for v_C and v_O in Figure 15.33. As depicted in Figure 15.33, let us assume that the system starts from rest so the capacitor voltage $v_C = 0$. Thus the inverting terminal v^- of the Op Amp is at 0 V. Let us also assume that the output is in positive saturation initially, in other words at the positive power supply voltage, V_S. Since the output is fed back to the positive input, we observe that

$$v^+ = \frac{V_S R_1}{R_1 + R_2}.$$

This positive voltage at the non-inverting input terminal will result in a positive voltage difference at the Op Amp input port (between v^+ and v^-), and consequently, the output will continue to be driven to the positive saturation voltage, namely V_S. The equivalent circuit is as shown in Figure 15.32. The capacitor C begins to charge up towards V_S through the resistor R_3. Since no current flows into the v^- terminal, the charging dynamics are that of a simple RC circuit.

As the capacitor charges up, eventually its voltage v_C crosses $v^+ = V_S R_1/(R_1 + R_2)$, resulting in an effective negative voltage across the Op Amp input port, namely across the v^+ and v^- terminals. The Op Amp amplifies this negative voltage difference at its input to a large negative voltage at its output. Since the negative voltage at the output is fed back to the non-inverting terminal by the voltage divider formed by R_1 and R_2, the non-inverting terminal voltage becomes negative, which makes the voltage difference at the Op Amp input even more negative, and which in turn makes the output voltage fall even more. This positive feedback process continues until the output reaches the negative saturation voltage $-V_S$. At this point, we have

$$v^+ = \frac{-V_S R_1}{R_1 + R_2}.$$

Notice that the output voltage transitions from V_S to $-V_S$ very quickly at the moment that the capacitor voltage v_C crosses $V_S R_1/(R_1 + R_2)$.

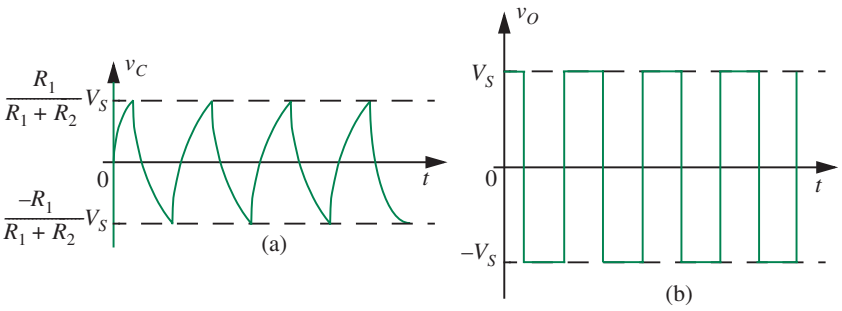


FIGURE 15.33 Oscillator behavior.

Therefore, at the instant the output reaches $-V_S$ and v^+ transitions to $-V_S R_1/(R_1 + R_2)$, we can assume that the capacitor voltage is still at approximately $V_S R_1/R_1 + R_2$, since the voltage across the capacitor changes much more slowly.

Now, since the capacitor voltage v_C is higher than the output voltage, the capacitor begins to discharge through R_3. Figure 15.34 shows that the equivalent circuit that applies. When the capacitor voltage falls below $-V_S R_1/R_1 + R_2$, the voltage v^- will be lower than v^+ resulting in a positive voltage difference at the Op Amp input. The Op Amp amplifies this positive difference to a positive voltage at its output, which when fed back to the non-inverting terminal causes a larger positive voltage to appear across the Op Amp input. The resulting positive feedback causes the Op Amp output to go into positive saturation. Thus, the output voltage reaches V_S and that at v^+ will again be

$$v^+ = \frac{V_S R_1}{(R_1 + R_2)}.$$

As in the beginning, the capacitor voltage is now lower than the output and therefore the capacitor begins to charge up. This cycle repeats and results in a square wave at the output of the Op Amp.

Let us derive the time period of the oscillator in Figure 15.31. Assume that at time T_1, v_O transitions from V_S to $-V_S$ as illustrated in Figure 15.35. We know that at T_1^-, $v_O = V_S$ and from the voltage-divider relationship, we know that $v^+ = R_1 V_S/(R_1 + R_2)$. We also know that v^- is lower than v^+ at T_1^-, and that the capacitor voltage is increasing.

At time T_1^+, v^- becomes slightly greater than v^+. In other words, $v^- \approx V_S R_1/(R_1 + R_2)$. Output v_O transitions virtually instantaneously to $-V_S$ and v^+ becomes $-R_1 V_S/(R_1 + R_2)$. The capacitor now begins to discharge and v^- begins to decrease. We know that v_O will transition from low to high when v^- falls below $v^+ = -R_1 V_S/(R_1 + R_2)$.

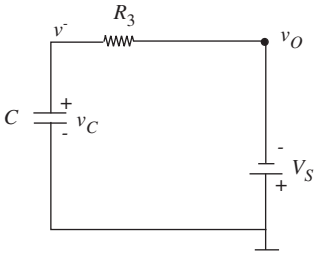


FIGURE 15.34 Equivalent circuit for the RC oscillator when the Op Amp is in negative saturation.

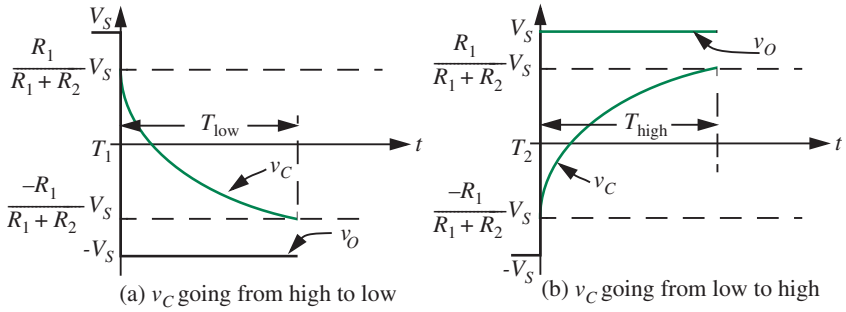


FIGURE 15.35 Computing the time period of the oscillator.

Thus the interval T_{low} is the time taken for the capacitor to discharge from its initial value of $V_S R_1/(R_1 + R_2)$ to its final value of $-V_S R_1/(R_1 + R_2)$. The capacitor discharge dynamics are governed by a simple first-order differential equation whose solution is given by

$$v_C = -V_S + \left(\frac{R_1}{R_1 + R_2} + 1\right) V_S e^{-t/R_3 C}. \tag{15.111}$$

We need to find T_{low}, the time taken for v_C to drop below $-R_1 V_S/(R_1 + R_2)$ from Equation 15.111. In other words, we need to solve for the time that satisfies

$$v_C = -V_S + \left(\frac{R_1}{R_1 + R_2} + 1\right) V_S e^{-t/R_3 C} < -\frac{R_1}{R_1 + R_2} V_S. \tag{15.112}$$

Thus,

$$-V_S + \left(\frac{R_1}{R_1 + R_2} + 1\right) V_S e^{-T_{\text{low}}/R_3 C} = -\frac{R_1}{R_1 + R_2} V_S,$$

which yields

$$T_{\text{low}} = R_3 C \ln\left(1 + \frac{2R_1}{R_2}\right). \tag{15.113}$$

It is easy to verify that the duration of the high period T_{high} is exactly the same as the low period. Thus, the period T of the oscillator is simply

$$T = 2R_3 C \ln\left(1 + \frac{2R_1}{R_2}\right).$$

WWW 15.9 TWO-PORTS*

15.10 SUMMARY

- The Op Amp is a widely used amplifier abstraction that forms the foundations of much of electronic circuit design. Op Amp devices are constructed using primitive elements such as transistors and resistors.
- The Op Amp is a four-ported device. The ports include an input port with terminals usually labeled v^+ and v^-, an output port with one terminal labeled v_o, and the other being ground, a positive power supply port with a $+V_S$ voltage applied with respect to ground, and a negative power supply port with a $-V_S$ voltage applied with respect to ground. Although the ground terminal is not explicitly shown in the Op Amp symbol, it is very much a part of all Op Amp circuits.
- The Op Amp behaves like a voltage-dependent voltage source. Its input-output relationship can can be expressed mathematically as

$$v_o = A(v^+ - v^-)$$

  where A is a large number called the open loop gain of the amplifier. In most practical Op Amp applications, A is treated as infinity.
- Most useful Op Amp circuits are built using the negative feedback connection, in which a portion of the output signal of the Op Amp is fed back to the v^- input of the Op Amp. Examples of Op Amp circuits built this way include inverting and non-inverting amplifiers, buffers, adders, integrators, and differentiators.
- We commonly apply the constraint:

$$v^+ \approx v^-$$

  in analyzing Op Amp circuits, if the Op Amp is not saturated and the feedback is negative.
- Op Amp circuits are sometimes built using the positive feedback connection, in which a portion of the output signal of the Op Amp is fed back to the v^+ input of the Op Amp. Examples of such Op Amp circuits include oscillators and comparators.

EXERCISES

EXERCISE 15.1 Find the Thévenin equivalent for the circuit in Figure 15.41. The circuit contains two resistors and a dependent current source.

EXERCISE 15.2 Calculate v_O in terms of I_1, V_1, and V_2 in Figure 15.42. You may assume the operational amplifier has ideal characteristics.