A 130 nm Operational Amplifier: Design and Schematic Level Simulation

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***Abstract*—In this paper an operational amplifier of general purpose is presented. The unified current-control model is used to synthesize a standard, two-stage topology based circuit. The design procedure is discussed thoroughly and every step is explained in details. The results obtained include open loop gain of 74 dB, the gain-bandwidth product of 100 MHz and the phase margin higher than 46°. Supply voltage and temperature coefficients are analyzed and discussed within the paper. Process variations are investigated through corner analysis. The results presented are obtained through schematic level simulations using the Spectre Simulator from Cadence Design System and a standard 130 nm CMOS technology process.**

Keywords–CMOS, integrated circuits, op amp design, unified current-control model, schematic level simulations

I. Introduction

The operational amplifier represents one of the most useful and one of the most used building blocks for analog integrated circuits. Even though it was established 80 years ago, by Harry Black [1], the fundamental idea remains the same: to make an amplifier stable over temperature changes and power-supply variations, we build an extremely high gain amplifier and introduce it in the negative feedback configuration.

The term operational amplifier (op amp) was used for the first time in 1947, in [2] where certain applications of the circuit were also presented. In the following two decades, op amps became more and more popular with the development of the bipolar integrated circuits technology [3]. The first comprehensive study of the op amps circuit was given by Solomon in [4]. During more than half a century of development, the op amp has been used in a variety of applications, such as: instrumentation amplifiers, continuous-time and switched capacitor filters, D/A and A/D converters, non-linear analog operators, signal generators and voltage regulators [5], [6], [7].

In this paper, the design and synthesis of a two-stage frequency compensated op amp are performed using the unified current-control model (UICM) [7], [8]. Open loop gain achieved at nominal conditions is 74 dB, whereas phase margin and gain-bandwidth product are 46°and 100 MHz, respectively. Process, voltage and temperature (PVT) variations and stability are also analyzed within this paper. Simulations are performed using the Cadence Design System toolchain a standard 130 nm CMOS technology process.

II. Model Used

The design methodology is based on the UICM model [7], [8]. It is a current-based MOSFET model that uses the concept of inversion level. According to the UICM model, the drain current can be split into the forward (I_F) and reverse (I_R) currents:

$$I_D = I_F - I_R = I_S(i_f - i_r), \tag{1}$$

where I_S is the normalization specific current, and i_f and i_r are inversion levels, forward and reverse, respectively. The forward and reverse currents depend on the gate to source and gate to drain voltages, respectively. If the transistor operates in saturation, we have:

$$I_F \gg I_R, \text{ thus: } I_D \approx I_F = I_S \cdot i_f. \tag{2}$$

The normalization current is a function of the technology:

$$I_S = \frac{\mu C_{ox} \phi_T^2 n}{2} \frac{W}{L}, \tag{3}$$

where μ represents the charge mobility, C_{ox} gate-oxide capacitance per area, ϕ_T thermal voltage, n slope factor and W/L transistor aspect ratio.

The inversion level value signifies the transistor operation region in the following way: if $i_f < 1$, the transistor operates in weak inversion and if $i_f > 100$ the transistor operates in strong inversion region. If $1 < i_f < 100$, the transistor operates in moderate inversion region. The voltage and current are related in the following manner [7]:

$$\frac{V_P - V_{S(D)}}{\phi_T} = \sqrt{1 + i_{f(r)}} - 3 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right), \tag{4}$$

where V_P is the pinch-off voltage, given as the difference of the gate potential and the zero bias threshold voltage (modified by the slope factor):

$$V_P \approx \frac{V_G - V_{T0}}{n}, \text{ if } V_G \approx V_{T0}. \tag{5}$$

Transistor drain-source saturation voltage is calculated as:

$$V_{DSsat} = \phi_T \left(\sqrt{1 + i_f} + 3\right), \tag{6}$$

while the transconductance is given as:

$$g_m = \frac{2 I_D}{n \phi_T \left(\sqrt{1 + i_f} + 1\right)}. \tag{7}$$

Further detailed description of the model can be found in [7] and [8].

978-1-4673-7016-5/15 $31.00 © 2015 IEEE
DOI 10.1109/CICSyN.2015.50

III. The Proposed Circuit Theory Overview

One way to increase the voltage gain of a single-stage amplifier is to use cascode topology, since in this way the output impedance is increased. Such an approach also implies stacked transistors (telescopic and folded cascode topologies [7]), which means that the output swing and the overdrive voltage are reduced. This issue is even more significant when advanced technology nodes are in question, since the supply voltage also scales. A possible solution is to use cascaded stages instead. Such comfort is paid by introducing another pole in the system, which appears as a consequence of the second amplifying stage. Another pole in the system, if not handled properly, can put in question the circuit transient response. Therefore, a part of the two-stage op amp design is the task of frequency compensation.

The proposed circuit schematic is shown in Fig. 1. The topology is standard and commonly used and it consists of a differential amplifier (first stage), a common source amplifier (second stage) and the frequency compensating network. In this case, the compensating network consists only of the feedback capacitor, C_C. The detailed discussion and the full explanation of the frequency compensation technique and the Miller effect are beyond the scope of this paper, and here only a short overview is given.

Frequency compensation is generally required in a two-stage op amp in order to avoid the op amp in a feedback configuration being unstable or having an unacceptably under-damped oscillatory time response. Namely, for the stability of the feedback amplifier a necessary condition is that the phase delay introduced by the open-loop gain and the feedback network at the unity-gain frequency does not exceed 180°. In other words, to obtain a time response without excessive overshoot, a phase margin (PM) of 45°is needed [6]. An op amp characterized by such a feature will be stable, i.e. will not oscillate when connected in feedback configuration.

To analyze the two-stage system frequency situation, we observe the schematic in Fig. 1 assuming two different cases: $C_C = 0$ and $C_C \neq 0$. For the same purpose we adopt the following terminology: g_{oI} - the output conductance, g_{mI} - the transconductance and C_{oI} the output capacitance of the first stage; analog symbols apply for the second stage: g_{oII}, g_{mII} and C_{oII}. The full equation of the amplifier gain will not be discussed here, we will adopt from [5]-[7] that it contains two poles and a zero. These two poles are located relatively close to each other in general case ($C_C = 0$). The task of the compensation network, namely, the capacitor C_C, is to move them farther apart, as shown in Fig. 2. This technique is called pole splitting [4] and for $C_C \neq 0$ allows the assumption of $p_2 \gg p_1$, which makes p_1 the dominant pole. Taking into account certain approximations and the detailed theoretical discussion given in literature, we adopt

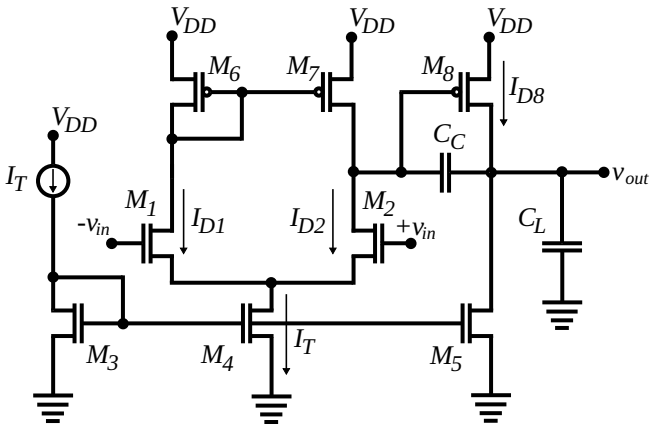

Figure 1. Proposed circuit schematic

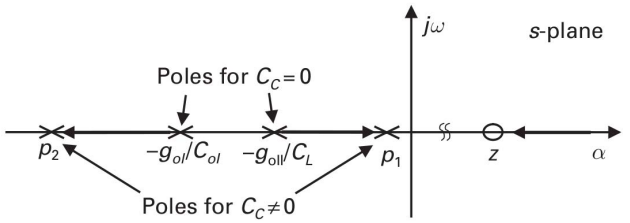

Figure 2. Feedback capacitor C_C influence on transfer function pole positions - pole splitting technique [7]

the following:

$$p_1 \approx -\frac{g_{oI} g_{oII}}{g_{mII} C_C}, \tag{8}$$

$$p_2 \approx -\frac{g_{mII}}{C_L} \text{ and} \tag{9}$$

$$z \approx \frac{g_{mII}}{C_C}. \tag{10}$$

where p_1, p_2 and z represent the frequencies of the first and the second pole and the zero of the system. In a well designed op amp: $p_2 > \omega_u$ and $z > 10 \cdot \omega_u$, where ω_u is the unit-gain frequency or the gain-bandwidth product (GBW) and can approximately be calculated as:

$$\omega_u = GBW = \frac{g_{mI}}{C_C}. \tag{11}$$

During simulation process a standard value for the load capacitor, C_L is of the order of 1 pF, and usually C_C is taken to be $0.5 \cdot C_L$ (for reasons discussed in the next section), i.e. $C_C = 500$ fF.

High-frequency circuit gain is completely characterized by these three equations, therefore we only provide the expression for the low-frequency gain [7]:

$$A_{v0} = A_{vI} A_{vII} = \frac{g_{mI} g_{mII}}{g_{dI} g_{dII}}, \tag{12}$$

where $A_{vI} = -g_{mI}/g_{dI}$ and $A_{vII} = -g_{mII}/g_{dII}$ represent the low-frequency gain of the first and second stage, respectively. At frequencies in question, we can assume that the

following is valid [7]:

$$\begin{array}{ll} g_{mI} \approx g_{m1} & g_{dI} \approx g_{d2} + g_{d6} \\ g_{mII} \approx g_{m8} & g_{dII} \approx g_{d5} + g_{d8} \end{array} \quad (13)$$

where g_{m1} and g_{m8} represent the transconductances of transistors M_1 and M_8, and g_{d2}, g_{d5}, g_{d6} and g_{d8} represent the output conductances of transistors M_2, M_5, M_6 and M_8.

IV. Op Amp Design Using UICM

Before employing the UICM to design the op amp, certain values need to be assumed. Short-channel effects severely affect transistor operation in advanced technology nodes [9], where 130 nm belongs. This technology intrinsic frequency limit is of the order of 100 GHz at minimum channel lengths. Since this circuit is intended for applications of the order of MHz, it is not mandatory to use minimum channel length. This means that we have the liberty to use larger channel lengths, so that the short-channel effects are not dominant. Therefore, in this paper $L_{min} = 500$ nm. Further, we assume the minimum transistor width, because the mismatch is inversely proportional to the device size [10]. In order to improve device matching, we determine that no transistor channel width should be smaller than ten times the minimum assumed length: $w_{min} = 5$ μm. For the transistor model in use, the nominal voltage is $V_{DD} = 3.3$ V. All transistors must operate in saturation ($i_f \gg i_r$) and the drain-source saturation voltages are of the order of 0.3 V. For the simplicity of calculations, we assume that the inversion level is the same for all transistors in the circuit.

Using the transistor model approximate parameters, it is possible to calculate the sheet normalization current for n-channel:

$$I_{SHN} = \frac{I_{SN}}{W/L} = \frac{\mu_N C_{ox} \phi_T^2 n}{2} = 61 \text{ nA}, \quad (14)$$

and for p- channel devices:

$$I_{SHP} = \frac{I_{SP}}{W/L} = \frac{\mu_P C_{ox} \phi_T^2 n}{2} = 13.4 \text{ nA}. \quad (15)$$

Since it directly defines the transistor working point, we first calculate the inversion level. Taking into account equations given in section II of this paper and the schematic in Fig. 1, the easiest way to obtain the inversion level is to assume $V_{DSsat4} = 0.3$ V for transistor $M_4$and apply equation (6):

$$i_f = \left(\frac{V_{DSsat4}}{\phi_T} - 3 \right)^2 - 1 = 73.44 \approx 80. \quad (16)$$

Therefore, the transistors operate in moderate inversion.

Next, we determine the tail current, i.e. I_{D4}, the drain current of M_4. In order to do so we notice that $I_{D4} = I_{D1} + I_{D2} = 2 \cdot I_{D1}$ and actually first calculate I_{D1} using equation (7):

$$I_{D1} = I_{D2} = \frac{g_{m1} n \phi_T}{2} \left(\sqrt{(i_f + 1)} + 1 \right). \quad (17)$$

The unknown value of g_{m1} is obtained using equations (11) and (13) as:

$$\begin{aligned} g_{m1} = \omega_u \cdot C_C &= 2\pi \cdot 100 \cdot 10^6 \cdot 500 \cdot 10^{-15} = \\ &= 314 \cdot 10^{-6} \approx 350 \mu\text{S}, \end{aligned} \quad (18)$$

where a bit higher transconductance value is taken to guarantee the needed performance. Using (18) in (17), we obtain $I_{D1} = 44.56$ μA ≈ 45 μA, which enables us to find the geometry ratios of transistors M_1 and M_2:

$$\left(\frac{W}{L} \right)_1 = \left(\frac{W}{L} \right)_2 = \frac{I_{D1}}{I_{SHN} i_f} = 9.53 \approx 10. \quad (19)$$

Since L_{min} = 500 nm, we write: $W_1 = W_2 = 5$ μm. Keeping in mind, $I_{D4} = 2 \cdot I_{D1}$, it follows $W_4 = 2 \cdot W_1 = 10$ μm.

From Fig. 1, we see that $I_{D6} = I_{D7} = I_{D1}$. This conclusion, along equation (15) enables the M_6 and M_7 geometry calculation as follows:

$$\left(\frac{W}{L} \right)_6 = \left(\frac{W}{L} \right)_7 = \frac{I_{D1}}{I_{SHP} i_f} = 41.97 \approx 42, \quad (20)$$

which further means that $W_6 = W_7 = 21$ μm.

Since transistor M_3 should be identical to M_4, we now have all the information needed to simulate the op amp first stage - the differential amplifier. This is done to check the transistors DC operating points. Running the simplest DC simulation, we find that the M_1 operating point is a bit different, but acceptable: $I_{D1} = 46$ μA and $g_{m1} = 360$ μS. We also check the DC gain by reading the output conductance values and using equations (12) and (13:

$$A_{vI} = \frac{g_{m1}}{g_{d2} + g_{d7}} = \frac{360}{1.83 + 4.40} \approx 58. \quad (21)$$

where minus sign is omitted since it represents only the 180°phase shift. This gain magnitude does not satisfy the starting requirement of A_{v0} =74 dB, where the first stage should provide the gain of 37 dB, i.e. 70. Since the main purpose of the PMOS transistors, M_6 and M_7, is to act as loads and that their output conductance directly influences the DC gain - we will improve A_{vI} by decreasing g_{d7}. The transistor output conductance is inversely proportional to the channel length. Therefore, to obtain an acceptable level of gain in the first stage, we increase the M_6 and M_7 channel lengths to $L_6 = L_7 = 600$ nm and adopt the new values of channel widths accordingly: $W_6 = W_7 = 28.6$ μm. Rerunning the DC simulation, we find $A_{vI} = 36.52$ dB which is acceptable.

The second stage transistor operating points and geometries we derive from the phase margin requirement. The PM is actually the difference in phase of the output and the input signal at ω_u frequency. Since this circuit transfer function is characterized by a zero and two poles, phase difference of output and input is:

$$PM(\omega) = \tan^{-1}\left(\frac{\omega}{z}\right) - \tan^{-1}\left(\frac{\omega}{p_1}\right) - \tan^{-1}\left(\frac{\omega}{p_2}\right). \quad (22)$$

Since we are interested in the value of PM at $\omega = \omega_u$, we use equations (8)-(11) to obtain:

$$\begin{aligned} PM(\omega_u) &= \tan^{-1}\left(\frac{\omega_u}{10\cdot\omega_u}\right) - \\ &- \tan^{-1}\left(\frac{g_{mI}}{C_C}\cdot\frac{g_{mII}C_C}{g_{dI}g_{dII}}\right) - \\ &- \tan^{-1}\left(\frac{\omega_u}{p_2}\right). \end{aligned} \quad (23)$$

The first member of this equation is 0.1 and the second one is, according to (12), the op amp DC gain, A_{v0}. Assuming that $A_{v0} = 74$ dB as required and remembering (13), we write:

$$PM(\omega_u) = 84.29^\circ - \tan^{-}1\left(\frac{\omega_u}{p_2}\right) \geq 45^\circ \quad (24)$$

which further yields: $p_2 \geq 1.22\cdot\omega_u$. Equations (10), (11) and (24) provide us with the conditions:

$$g_{m8} \geq 10\cdot g_{m1} \quad \text{and} \quad C_C \geq 0.13C_L. \quad (25)$$

The first condition we match by setting $g_{m8} = 3.5$ mS, while the second one is already fulfilled. Applying (17) to M_8, we obtain its drain current: $I_{D8} = I_{D5} = 465$ μA, which, using (15) and (19) further yields the geometry ratio: $W_8/L_8 = 434$ μm. According to (12) and (13), g_{d8} decisively influences the second stage gain, so we keep the channel length modification, i.e. L_8 =600 nm and $W_8 = 260.4$ μm. The M_5 is calculated in the same manner: $W_5 = 48$ μm.

Finally, all the circuit components are calculated and the DC simulation of the op amp yields promising values:

$$A_{vII} = \frac{g_{m2}}{g_{d5}+g_{d8}} = \frac{3400}{14.63+35.37} \approx 68 = 37 \text{ dB}. \quad (26)$$

Running a simple AC analysis, we find that A_{v0} of around 74 dB and PM of 53°are satisfactory, but that ω_u is only 80 MHz. The easiest change that we can make to the circuit, without affecting the transistor operation points is to vary the C_C. According to condition (25), we can make C_C as low as 130 fF. Even though decreasing its capacitance does increase ω_u, this procedure also decreases the PM, e.g. at C_C = 200 fF, ω_u = 110 MHz but $PM = 39^\circ$. Therefore, we must turn to the first condition in (25) and further increase g_{m8}/g_{m1} ratio, e.g. $g_{m8} = 12\cdot g_{m1}$. In this case, the second stage transistor geometries are: (W_8/L_8) = (312.6 μm / 600 nm) and (W_5/L_5) = (57.5 μm / 500 nm).

After some fine tuning through the feedback capacitor variation, we find that the requirements of 74 dB, 100 MHz and 46°in the nominal case are fulfilled for the capacitor value of C_C=290 fF. Such performance is paid by power consumption of 2.61 mW for a supply voltage of 3.3 V.

V. Simulation Results

In Fig. 3 the op amp in open loop configuration AC simulation results are given. As designed in section IV, the circuit shows the fulfillment of the given requirements in the nominal conditions, i.e. at room temperature, supply voltage of 3.3 V and using the transistor model of typical values. The unity-gain frequency, $\omega_u = 2\pi\cdot f_u$ is $2\pi\cdot$100 MHz, while the DC gain is 73.91 dB and PM is 46°. Further, the op amp transfer function poles and zero are also shown. The dominant pole, p_1, is the one which introduces the gain decrease of -20 dB per decade and the phase shift of 90°, marked as 3 dB frequency in the figure. The second pole introduces the additional -20 dB per decade to the gain decrease at frequency of 210 MHz. Obviously it is beyond f_u, which means that we successfully employed the frequency compensation technique through the feedback capacitor C_C to remove its influence on the op amp operation at frequencies of interest. The zero is shown at frequency of beyond 2 GHz. Therefore, both conditions mentioned in section III theory discussion, $p2 > \omega_u$ and $z > 10\cdot\omega_u$ are fulfilled.

For the input signal amplitude of 1 μV and frequency of 20 kHz, both input and output are shown in Fig. 4. The circuit introduces a time delay of 4.4 μs. From Fig. 5 we conclude that the op amp output takes an interval of 65 μ to settle.

In Tab. I process, voltage and temperature (PVT) variations influences to the op amp characteristics are shown. Process variations are analyzed through running the simulations with different component nodes. Namely, the DC current ideal source shown in Fig. 1 is actually replaced by a resistor model available for the 130 nm technology process. Also, the process variations of the feedback capacitor are included in the worst case analysis. Voltage variations are introduced by setting the supply voltage to $\pm$10 % values of the nominal, i.e. 2.97 V and 3.63 V. Temperature influence is analyzed by varying the temperature over the whole range for which the technology models are valid, namely -40°up to 125°.

Besides these simulations performed with the op amp in the open loop configuration, the stability analysis is performed for the nominal case. For this simulation, the op amp is connected in the closed loop configuration with unity feedback. This stability simulation purpose is to show the circuit's behavior when the loop is closed and determine whether there is a possibility to oscillate. The op amp designed in this paper, because of all the precautions taken and careful calculations in section IV does not oscillate and the characteristics for this configuration are given in Tab. I.

Important characteristics of an op amp also include: common-mode rejection ratio ($CMRR$), power supply rejection ratio ($PSRR$), input common mode range ($ICMR-$ and $ICMR+$), output range (V_{Omax} and V_{Omin}) and slew

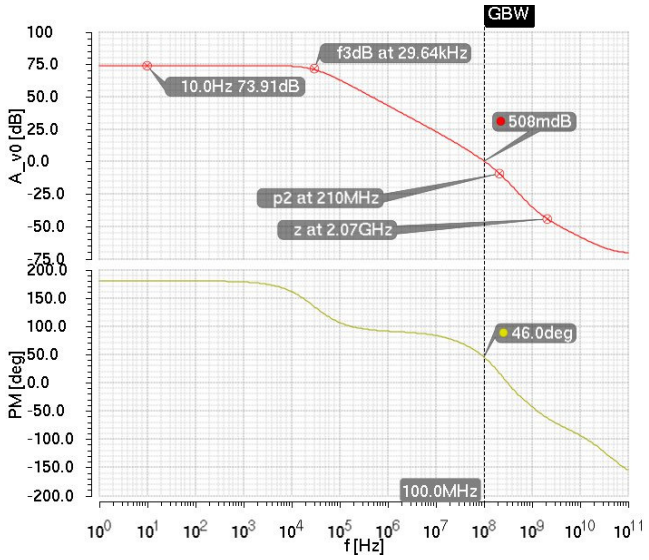

Figure 3. Op amp open loop gain and phase

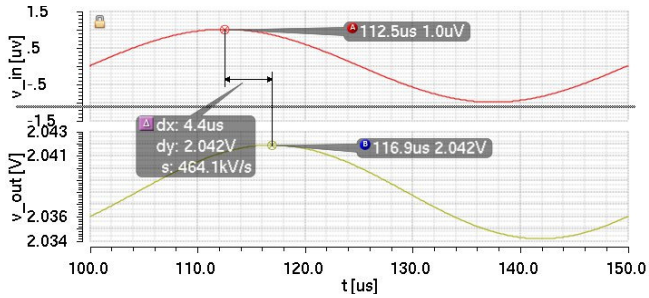

Figure 4. Op amp input and output signals showing the delay of 4.4 μs

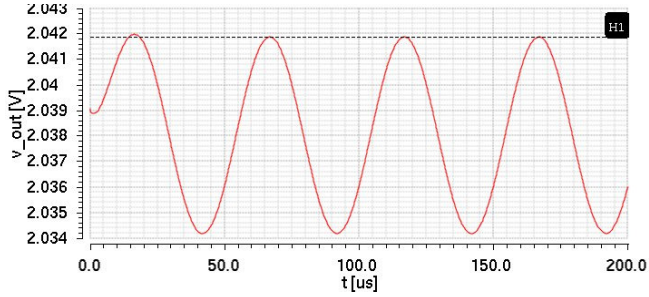

Figure 5. Op amp output signal showing the settling time of 65 μs

TABLE I
PVT AND STABILITY ANALYSIS

		A_{v0} [dB]	f_u [MHz]	PM	I_T [μA]
Nominal		73.91	100	46°	98
Process	SS	76.13	96.25	42°	80
	FF	71.42	113	47°	122
Voltage	2.97 V	73.57	97	45°	86
	3.63 V	74	109	45°	110
Temp	-40°C	75	117	44°	93
	125°C	73	92	45°	104
Stability		73.16	122	62°	n/a

rate (SR). Through simulations, the values obtained for each of these features are: 122 dB, 200 dB, 1.3 V, 3 V, 290 mV, 3.06 V and 172 V/μs, respectively.

VI. DISCUSSION

In Tab. II the amplifier characteristics yielded through the described process of design and simulation are given along those found in literature.

The authors in [11] present a novel folded cascode op amp that uses positive feedback technique to improve the open-loop gain. Even though that is the prime goal of the design, the other characteristics are not influenced. Similar to this work, high performance is traded for higher power consumption. The same principle is applied in [12], even though the open-loop gain is significantly less than that of [11] at almost the same level of power consumption. In this case lower performance is a consequence of an older and less advanced node - the circuit is designed using a 0.35 μ CMOS technology process. The author's goal in [13] was to design a low power rail-to-rail op amp characterized with high $CMRR$. Therefore, the authors used a lower value supply voltage and additional circuitry, which did not influence the open-gain but did significantly decrease the gain-bandwidth product, i.e. f_u. In [14] the design of a two-stage op amp is presented, the main goal being area optimization. Such design decisions caused the circuit to consume less power, but also significantly decreased the f_u. Different op amp topologies, namely folded cascode, telescopic and two-stage, are discussed in [15]. These are analysed in detail, both in the context of topology and parameter tradeoffs. The authors show that the two-stage topology yields best results and use it to design and simulate a low power op amp.

TABLE II
OP AMP CHARACTERISTICS FOUND IN LITERATURE AND OF THIS WORK

	[11]	[12]	[13]	[14]	[15]	This
node [nm]	180	350	180	180	130	130
V_{DD} [V]	1.8	1.8	1	$\pm$1.8	1.2	3.3
A_{v0} [dB]	76	51	71	75	86	74
f_u [MHz]	513	513	32	7.3	55	100
PM [°]	75	76	55	48	n/a	46
P_{DD} [mW]	2.1	2.2	0.22	0.4	0.11	2.6
$CMRR$ [dB]	n/a	n/a	159	82	61	122
$OCMR$ [V]	1.6	1.6	rtr	3.4	1.1	1.7
SR [V/μs]	516	506	15	10	44	172

The op amp designed in this paper uses the highest supply voltage of the circuits mentioned in this section. The value of 3.3 V is chosen because it is still standard. The open-loop gain and the gain-bandwidth product belong to the higher end of the scale in II. As a tradeoff, this work's power consumption is also the highest among the circuits. As a consequence, some other figures of merit also show high-end performance, such as $CMRR$ and SR. The op amp

phase margin is at the lower limit of acceptability, but still good enough as proven in section IV. This circuit is designed with no application as a goal, but it is of a general purpose. Once it is applied to a specific task, the tradeoffs can be optimized.

The parameters and the whole Tab. II are in no way a direct one-on-one comparison between the designed circuits and in no mean are given to claim that one or another op amp is better or worse. As discussed in the previous passage, all of the circuits mentioned, including the one developed in this paper, are designed with different ideas of their respective authors and therefore show different characteristics. The purpose of Tab. II is only to show that the results yielded by the design process presented in sections III-V of this paper are of the order of magnitude found in recent literature.

VII. Conclusion

The op amp designed and simulated in this paper satisfies the initial requirements of 74 dB DC gain, 100 MHz gain-bandwidth product and 46°of phase margin in nominal conditions. The combination of calculations using the UICM model and Spectre Simulator from Cadence Design Systems allows quite straightforward and clear circuit synthesis process.

Stability analysis shows that the op amp developed is not subject to oscillations when in closed loop configurations. This characteristic is ensured through careful design while fulfilling all the conditions predefined through the theory discussion provided within the paper.

PVT variations analysis shows that the circuit is susceptible to these influences, but never failing for more than 8 % of the nominal case. Additional simulations performed give insight in more important op amp features, such as $CMRR$ and $PSRR$, all of which are also satisfying.

In future work, the first step is the circuit layout through which special attention is to be dedicated to process and mismatch variations. Temperature and voltage variations are also to be improved. High performance set by the initial requirements is accompanied by somewhat higher power consumption. When this op amp is applied to a specific task, there might be room for the optimization of this trade-off.

Acknowledgment

This work is funded from the European Union's Seventh Framework Program for research, technological development and demonstration under grant agreement no. 289481 - project SENSEIVER.

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