Low Power Operational Amplifier in 130nm Technology

V. Ashok kumar, Student at JNTU-GV CEV

***Abstract*—In this paper a low power operational amplifier consists of two stages and operates at 1.8V power. It is designed to meet a set of provided specification such as high gain and low power consumption. Designers are able to work at low input bias current and also at low voltage due to the unique behavior of the MOS transistors in sub-threshold region. This two-stage op-amp is designed using the Skywater 130nm technology library. The proposed two stage op-amp consists of NMOS current mirror as bias circuit, differential amplifier as the first stage and common source amplifier as the second stage. The first stage of an op-amp contributed high gain while the second stage contributes a moderate gain. The results show that the circuit is able to work at 1.8V power supply voltage (VDD)**

Keywords: op-amp, two-stage, miller capacitor, gain, ICMR, PSRR, CMRR, slew rate, low power, power dissipation.

I. INTRODUCTION

A low power operational amplifier gives advantages in many applications owing to prolongation of battery life and thus makes it suitable for portable devices. In analog devices product development, it offers high power efficiency without compromising the speed, noise and precision. Low power op-amp is widely used as a bio-potential amplifier where it is used to amplify and filter extremely weak bio-potential signals[6]. In industrial sections, it is widely used in the usage of barcode scanner.

Nowadays, the need on smaller size chip with very small power dissipation has increased the demand on low power design. But the obstacles on designing a good performance of a low power op-amp are on operating with power supplies that is smaller than 1 Volt, on getting an ideal characteristic of op-amp specification and on designing a circuit with the same or better performance than circuits designed for a larger power supply.

II. PRINCIPLE OF GENERATION

The proposed two-stage operational amplifier design features an input differential amplifier that delivers high input impedance, excellent common-mode and power supply rejection ratios, low offset voltage, low noise, and high gain, all while providing a single-ended output. The second stage performs level shifting to adjust the DC voltage for optimal biasing, adds gain for sufficient amplification, and converts the differential output from the first stage to a single-ended format. This configuration ensures robust performance in demanding applications by maintaining signal integrity and stability despite noise and power supply variations.

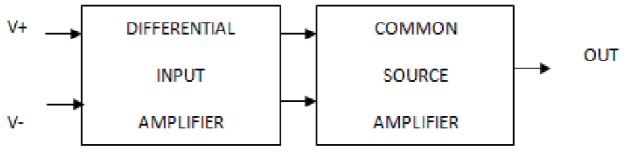


Figure 2. Block diagram of two-stage op-amp

III. IMPLEMENTATION

This consideration will be used to determine the width and length of the transistor. Based on the proposed schematic in Figure 3, the W/L ratio for M3 and M4 will be found from the max ICMR +, M1 and M2 will be found from the tranconductance gm1 and GBW, the current flow through M5 will be found from the slew rate, M5 and M6 will be found from minimum ICMR -, M6 from gain and the design of M3 and M4, I6 current flow to the second stage is related to the design of M3,M4 and I5, M7 is related to I5 because of the same biasing voltage and lastly the Cc value from phase margin. The length of the transistor value used when involving the two stage op-amp is L ≥ Lmin. Lmin is the technology used which is 130nm. So in this design the length used are either L=1000nm or L=500nm but only 500nm will be used. The 1000nm value will only be used if needed to satisfy the condition required. This large value is used to avoid channel length modulation and also the lambda, λ.

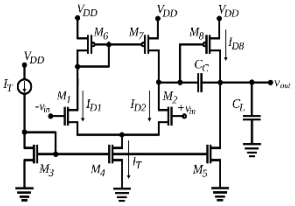
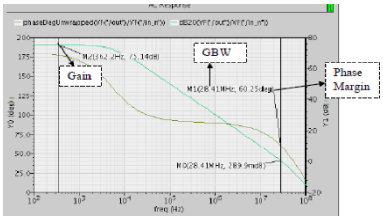


Figure 1. Proposed circuit schematic



IV. ISSUES AND IMPROVEMENTS

In this design, M8 is optimized to enhance gain, and the compensation capacitor Cc optimized improve the gain-bandwidth product (GBW). Adjusting parameters such as the ratios of M1 and M2 can increase gain and GBW, while high ratios for M3 and M4 boost maximum ICMR+, and large ratios for M5 and M6 minimize ICMR- near ground. M7 and M8 affect the second stage gain, with smaller sizes increasing overall gain. Only Cc and M8 are specifically optimized in this project.

V. CONCLUSION AND FUTURE SCOPE

Hence the low power two stage amplifier is designed and the gain, GBW are measure with respect to the normal design. By decreasing or increasing the W/L ration of the transistors or compensating capacitance the power is decreased without any decrease in the gain and other parameters of the OpAmp.

VI. REFERENCES

1. Khan, S. R. (2015). Design Analysis and Performance Comparison of Low Power High Gain 2nd Stage Differential Amplifier Along with 1st Stage. Journal of Automation and Control Engineering. 3(1), 82–86.

2. K. Raut, R. Kshirsagar, and A. Bhagali, “A 180 nm low power cmos operational amplifier,” in Computational Intelligence on Power, Energy and Controls with their impact on Humanity (CIPECH), 2014 Innovative Applications of, Nov 2014, pp. 341–344.