N-BIT RING COUNTER :

FPGA :

A field-programmable gate array (FPGA) is an integrated circuits designed to be configured by a customer or a designer after manufacturing, hence the term field programmable gate. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).Circuit diagrams were previously used to specify the configuration, but this is increasingly rare due to the advent of electronic design automation tools.

FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects allowing blocks to be wired together. Logic blocks can be configured to perform complex combinational functions, or act as simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. Many FPGAs can be reprogrammed to implement different logic functions, allowing flexible reconfigurable computing as performed in computer software.

FPGAs have a remarkable role in embedded system development due to their capability to start system software development simultaneously with hardware, enable system performance simulations at a very early phase of the development, and allow various system trials and design iterations before finalizing the system architecture.

RING COUNTER :

A ring counter is a type of counter composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "ring" structure.

There are two types of ring counters:

1.A straight ring counter, also known as a one-hot counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring.

2. A twisted ring counter, also called switch-tail ring counter, walking ring counter, Johnson counter, or Möbius counter, connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring.

Ring counters are often used in hardware design (e.g. ASIC and FPGA design) to create finite-state machines. A binary counter would require an adder circuit which is substantially more complex than a ring counter and has higher propagation delay as the number of bits increases, whereas the propagation delay of a ring counter will be nearly constant regardless of the number of bits in the code.

APPLICATIONS :

- Ring counters are used to count the data in a continuous loop.
- 2 stage, 3 stage, 4 stage ring counters are used in frequency divider circuits as divided by 2, divided by 3, and divided by 4, respectively.
- The 5 stage ring counter circuit is generally use as synchronous decade(BCD) counter and also as divider circuit.

ADVANTAGES :

- It doesn't need a decoder i.e. it is a self decoding circuit.
- It can be implemented using JK and D flip-flops.

DISADVANTAGES :

- In ring counter only 4 of the 15 states are being utilized. `

TRUTH TABLE:

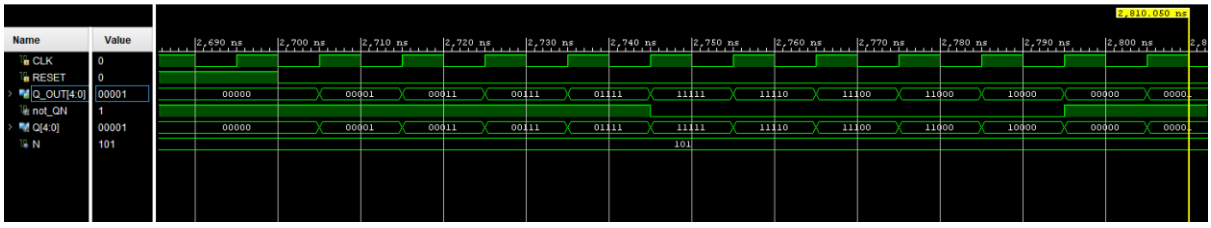
Clock	Q4	Q3	Q2	Q1	Q0
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	1
4	0	0	1	1	1
5	0	1	1	1	1
6	1	1	1	1	1
7	1	1	1	1	0
8	1	1	1	0	0
9	1	1	0	0	0
10	1	0	0	0	0
11	0	0	0	0	0

VHDL CODE:

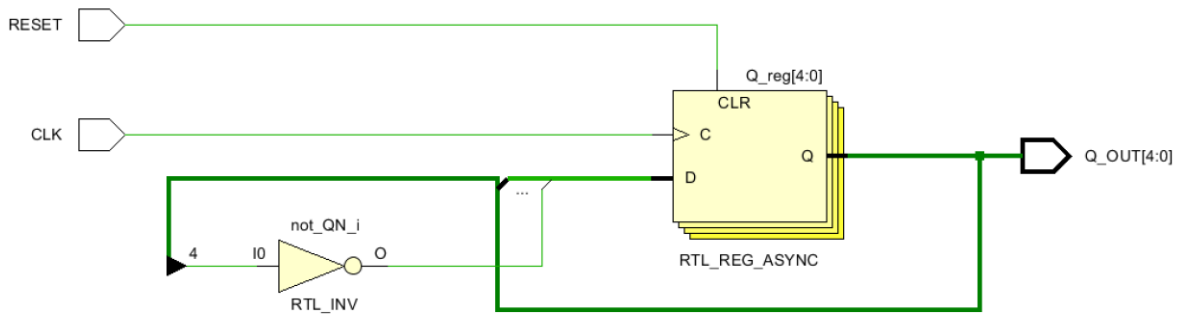
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Ringcounter is
generic ( N : integer:=5 );
port (
 CLK: in std_logic; -- clock
 RESET: in std_logic; -- reset
 Q_OUT: out std_logic_vector(N-1 downto 0) -- output
 );
end Ringcounter;
```

```
Architecture Behavioral of Ringcounter is
signal not_QN : std_logic;
signal Q : std_logic_vector(N-1 downto 0):=(others => '0');
begin
not_QN <= not Q(N-1);
process(CLK,RESET)
begin
 if(RESET='1') then -- asynchronous reset
 Q <= (others => '0');
 elsif(rising_edge(CLK)) then
 Q <= Q(N-2 downto 0) & not_QN; -- Switch TAil ring counter
 end if;
end process;
Q_OUT <= Q;
end Behavioral;
```

SIMMULATION WAVE FORMS:



SCHEMATIC DIAGRAM:

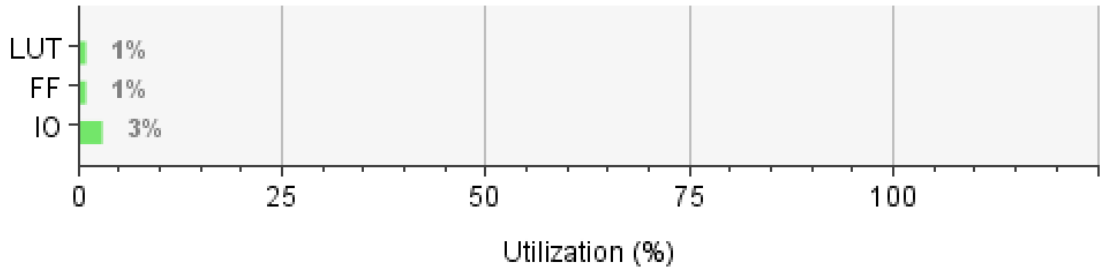


UTILIZATION REPORT:

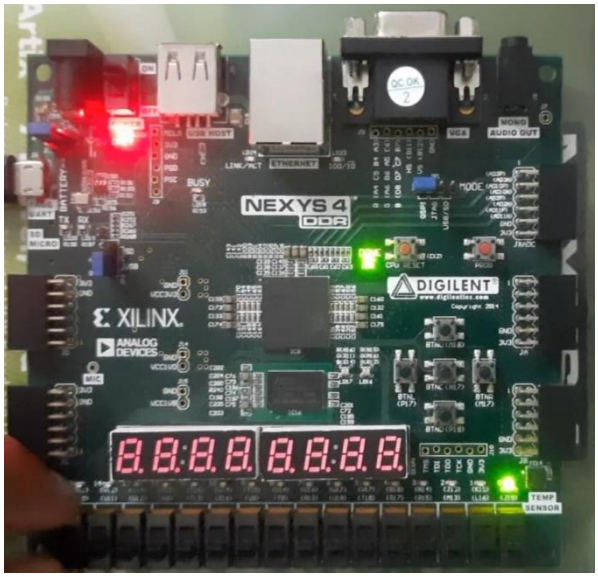
Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
Ringcounter	1	10	4	1	7	1

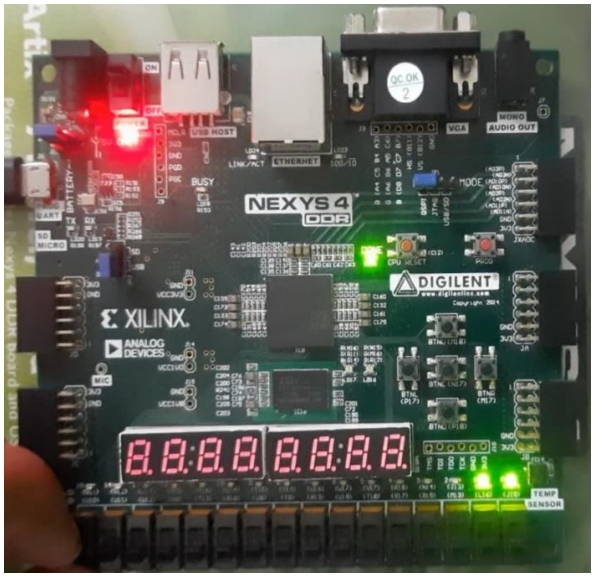
Summary

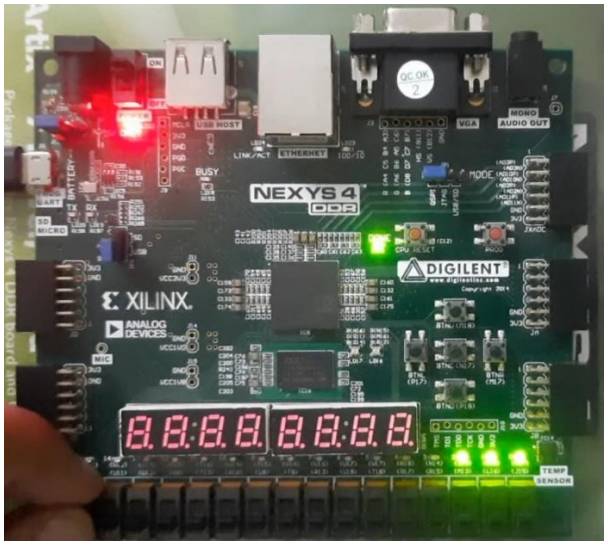
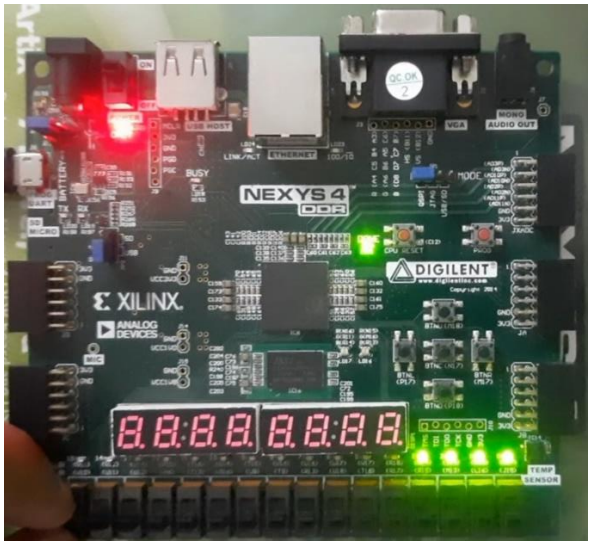
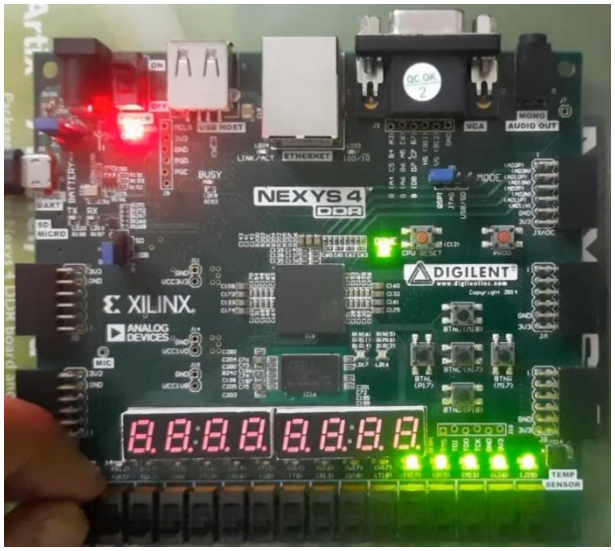
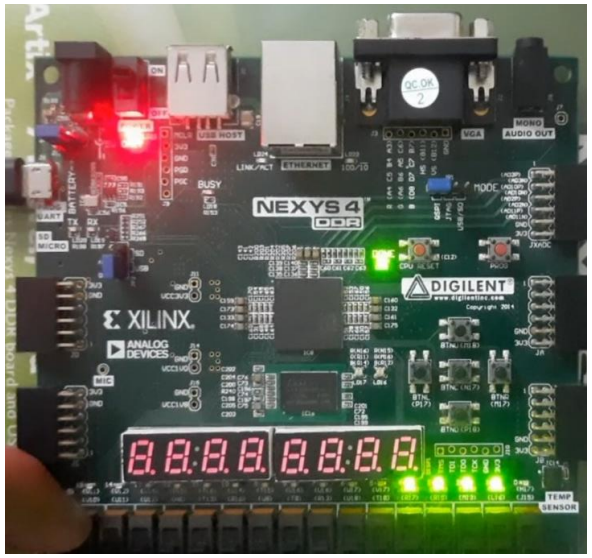
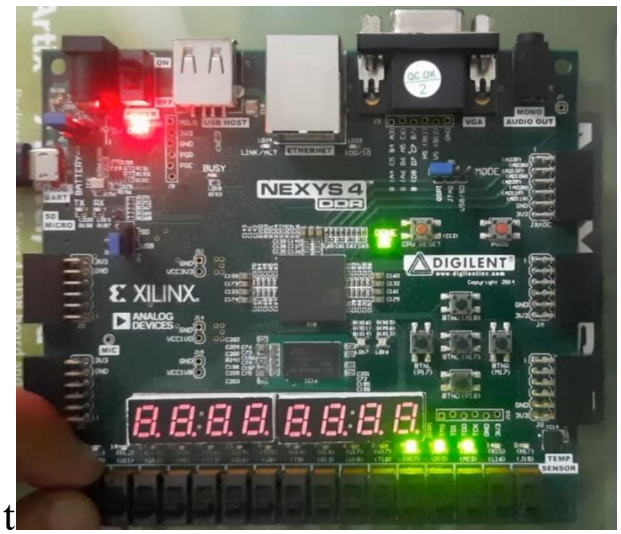
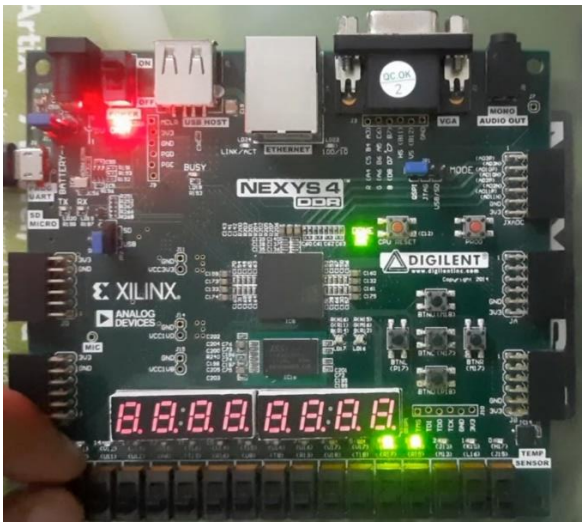
Resource	Utilization	Available	Utilization %
LUT	1	63400	0.00
FF	10	126800	0.01
IO	7	210	3.33



OUTPUTS:



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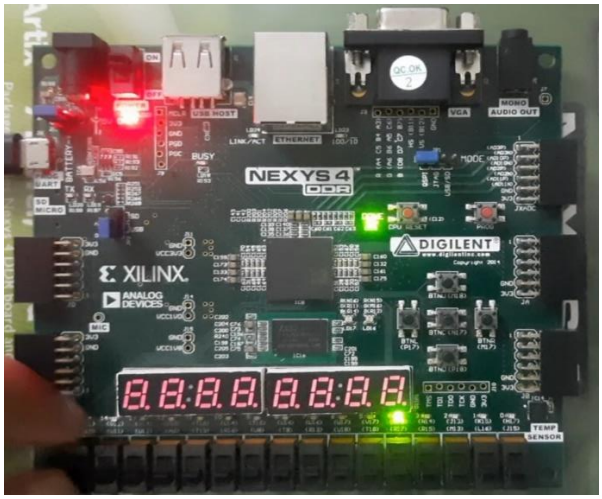

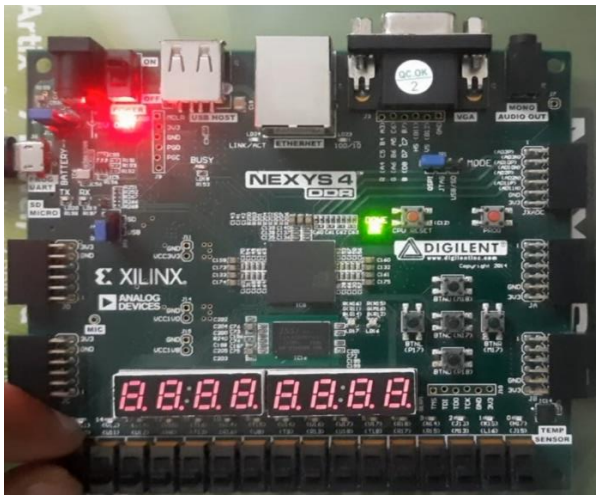

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