

```
1  /*****
2  *
3  * Decimal counter with 7-segment output.
4  * ATmega328P (Arduino Uno), 16 MHz, AVR 8-bit Toolchain 3.6.2
5  *
6  * Copyright (c) 2018-2020 Tomas Fryza
7  * Dept. of Radio Electronics, Brno University of Technology, Czechia
8  * This work is licensed under the terms of the MIT license.
9  *
10 *****/
11
12 /* Includes ----- */
13 #include <avr/io.h>           // AVR device-specific IO definitions
14 #include <avr/interrupt.h>    // Interrupts standard C library for AVR-GCC
15 #include "timer.h"           // Timer library for AVR-GCC
16 #include "segment.h"         // Seven-segment display library for AVR-GCC
17
18 uint8_t singles = 0;
19 uint8_t decimals = 0;
20
21
22 /* Function definitions ----- */
23 /**
24  * Main function where the program execution begins. Display decimal
25  * counter values on SSD (Seven-segment display) when 16-bit
26  * Timer/Counter1 overflows.
27  */
28 int main(void)
29 {
30     // Configure SSD signals
31     SEG_init();
32
33
34
35     // Test of SSD: display number '3' at position 0
36     SEG_update_shift_regs(3, 0);
37
38     //SEG_clear();
39
40
41     /* Configure 8-bit Timer/Counter0
42      * Set prescaler and enable overflow interrupt */
43     TIM0_overflow_4ms();
44     TIM0_overflow_interrupt_enable();
45
46     /* Configure 16-bit Timer/Counter1
47      * Set prescaler and enable overflow interrupt */
48     TIM1_overflow_262ms();
49     TIM1_overflow_interrupt_enable();
50
51     // Enables interrupts by setting the global interrupt mask
52     sei();
53
```

```
54     // Infinite loop
55     while (1)
56     {
57         /* Empty loop. All subsequent operations are performed exclusively
58          * inside interrupt service routines ISRs */
59     }
60
61     // Will never reach this
62     return 0;
63 }
64
65 /* Interrupt service routines ----- */
66 /**
67  * ISR starts when Timer/Counter0 overflows. Display value on SSD.
68  */
69 ISR(TIMER0_OVF_vect)
70 {
71     static uint8_t position = 0;
72     if (position == 0)
73         SEG_update_shift_regs(singles, 0); //first position
74     else
75         SEG_update_shift_regs(decimals, 1); //second position
76     position = !position; //change position (0 1)
77 }
78
79 /**
80  * ISR starts when Timer/Counter1 overflows. Increment decimal counter.
81  */
82 ISR(TIMER1_OVF_vect)
83 {
84     // number AB = 0-5 0-9
85     // LEd counter 0-59
86     singles++;
87     if(singles > 9)
88     {
89         singles = 0;
90         decimals++;
91         if(decimals > 5)
92             decimals = 0;
93     }
94 }
```