

```

1  #ifndef TIMER_H
2  #define TIMER_H
3
4  /*****
5   *
6   * Timer library for AVR-GCC.
7   * ATmega328P (Arduino Uno), 16 MHz, AVR 8-bit Toolchain 3.6.2
8   *
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10  * Dept. of Radio Electronics, Brno University of Technology, Czechia
11  * This work is licensed under the terms of the MIT license.
12  *
13  *****/
14
15 /**
16  * @file timer.h
17  * @brief Timer library for AVR-GCC.
18  *
19  * @details
20  * The library contains macros for controlling the timer modules.
21  *
22  * @note
23  * Based on Microchip Atmel ATmega328P manual and no source file is
24  * needed for the library.
25  *
26  * @copyright (c) 2019-2020 Tomas Fryza
27  * Dept. of Radio Electronics, Brno University of Technology, Czechia
28  * This work is licensed under the terms of the MIT license.
29  */
30
31 /* Includes ----- */
32 #include <avr/io.h>
33
34 /* Defines ----- */
35 /**
36  * @brief Defines prescaler CPU frequency values for Timer/Counter0.
37  * @note F_CPU = 16 MHz
38  */
39 #define TIM0_stop()          TCCR0B &= ~(1<<CS02) | (1<<CS01) | 7
40                             (1<<CS00));
41 #define TIM0_overflow_16us() TCCR0B &= ~(1<<CS02) | (1<<CS01)); 7
42                             TCCR0B |= (1<<CS00);
43 #define TIM0_overflow_128us() TCCR0B &= ~(1<<CS02) | (1<<CS00)); TCCR0B | 7
44                             = (1<<CS01);
45 #define TIM0_overflow_1ms()  TCCR0B &= ~(1<<CS02); TCCR0B |= (1<<CS01) | 7
46                             (1<<CS00);
47 #define TIM0_overflow_4ms()  TCCR0B &= ~(1<<CS01) | (1<<CS00)); TCCR0B | 7
48                             = (1<<CS02);
49 #define TIM0_overflow_16ms() TCCR1B &= ~(1<<CS01); TCCR0B |= (1<<CS02) | 7
50                             (1<<CS00);
51
52 /**
53  * @brief Defines interrupt enable/disable modes for Timer/Counter0.

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48 */
49 #define TIM0_overflow_interrupt_enable()    TIMSK0 |= (1<<TOIE0);
50 #define TIM0_overflow_interrupt_disable()   TIMSK1 &= ~(1<<TOIE0);
51
52
53 /**
54  * @brief Defines prescaler CPU frequency values for Timer/Counter1.
55  * @note F_CPU = 16 MHz
56  */
57 #define TIM1_stop()                        TCCR1B &= ~((1<<CS12) | (1<<CS11) |      ↗
58     (1<<CS10));
59 #define TIM1_overflow_4ms()                TCCR1B &= ~((1<<CS12) | (1<<CS11)); TCCR1B |= ↗
60     (1<<CS10);
61 #define TIM1_overflow_33ms()               TCCR1B &= ~((1<<CS12) | (1<<CS10)); TCCR1B |= ↗
62     (1<<CS11);
63 #define TIM1_overflow_262ms()              TCCR1B &= ~(1<<CS12); TCCR1B |= (1<<CS11) | ↗
64     (1<<CS10);
65 #define TIM1_overflow_1s()                 TCCR1B &= ~((1<<CS11) | (1<<CS10)); TCCR1B |= ↗
66     (1<<CS12);
67 #define TIM1_overflow_4s()                 TCCR1B &= ~(1<<CS11); TCCR1B |= (1<<CS12) | ↗
68     (1<<CS10);
69
70
71 /**
72  * @brief Defines interrupt enable/disable modes for Timer/Counter1.
73  */
74
75 #define TIM1_overflow_interrupt_enable()    TIMSK1 |= (1<<TOIE1);
76 #define TIM1_overflow_interrupt_disable()   TIMSK1 &= ~(1<<TOIE1);
77
78
79 /**
80  * @brief Defines prescaler CPU frequency values for Timer/Counter2.
81  * @note F_CPU = 16 MHz
82  */
83 #define TIM2_stop()                        TCCR1B &= ~((1<<CS22) | (1<<CS21) |      ↗
84     (1<<CS20));
85 #define TIM2_overflow_16us()               TCCR1B &= ~((1<<CS22) | (1<<CS21));      ↗
86     TCCR2B |= (1<<CS20);
87 #define TIM2_overflow_128us()              TCCR1B &= ~((1<<CS22) | (1<<CS20));      ↗
88     TCCR1B |= (1<<CS21);
89 #define TIM2_overflow_512us()              TCCR1B &= ~(1<<CS22); TCCR2B |= (1<<CS21) ↗
90     | (1<<CS20);
91 #define TIM2_overflow_1ms()                TCCR1B &= ~((1<<CS21) | (1<<CS20));      ↗
92     TCCR2B |= (1<<CS22);
93 #define TIM2_overflow_2ms()                TCCR1B &= ~(1<<CS21); TCCR2B |= (1<<CS22) ↗
94     | (1<<CS20);
95 #define TIM2_overflow_4ms()                TCCR1B &= ~(1<<CS20); TCCR2B |= (1<<CS22) ↗
96     | (1<<CS21);
97 #define TIM2_overflow_16ms()               TCCR1B |= (1<<CS21) | (1<<CS22) |      ↗
98     (1<<CS20);
99
100
101 /**
102  * @brief Defines interrupt enable/disable modes for Timer/Counter2.
103  */
104

```

```
87 #define TIM2_overflow_interrupt_enable()    TIMSK2 |= (1<<TOIE2);
88 #define TIM2_overflow_interrupt_disable()    TIMSK2 &= ~(1<<TOIE2);
89
90 #endif
```