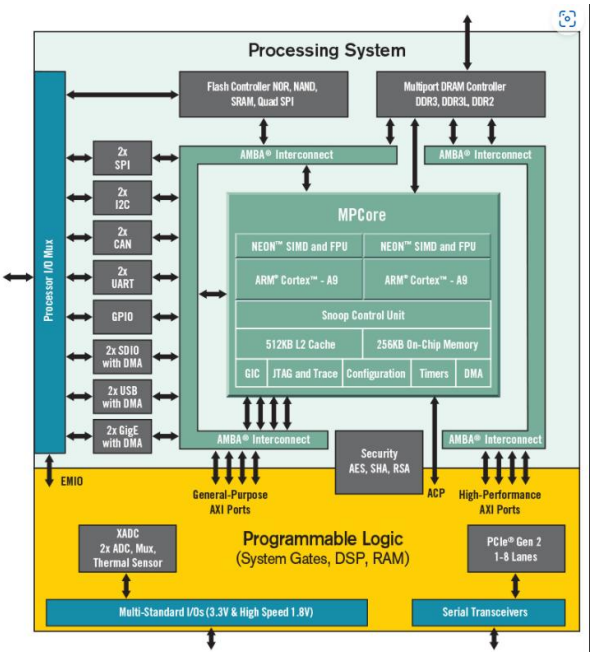
NIC BOARD QUICK START

1.0 Board Overview

The NIC board is a PCIe plug in smart Ethernet NIC card built around the Xilinx/AMD Zynq 7030 FPGA. The details on the FPGA can be found at the following link: Zynq 7000 SoC (xilinx.com).

The Zynq 7000 FPGA contain a dual core ARM processor along with an FPGA fabric coupled to the AXI bus. The block diagram of the FPGA is shown below.



The specific device used on this board is XC7Z030-1FBG676I which is an industrial grade part (rated at -40 to 85 C operation) in a 676 pin BGA package.

Th board consists of several interfaces which will be shown in the following sections. The board can be power through an external power source through a connector provided on the back of the board or by plugging it into the PCIe slot on a PC.

The package that has been shipped contains the following items:

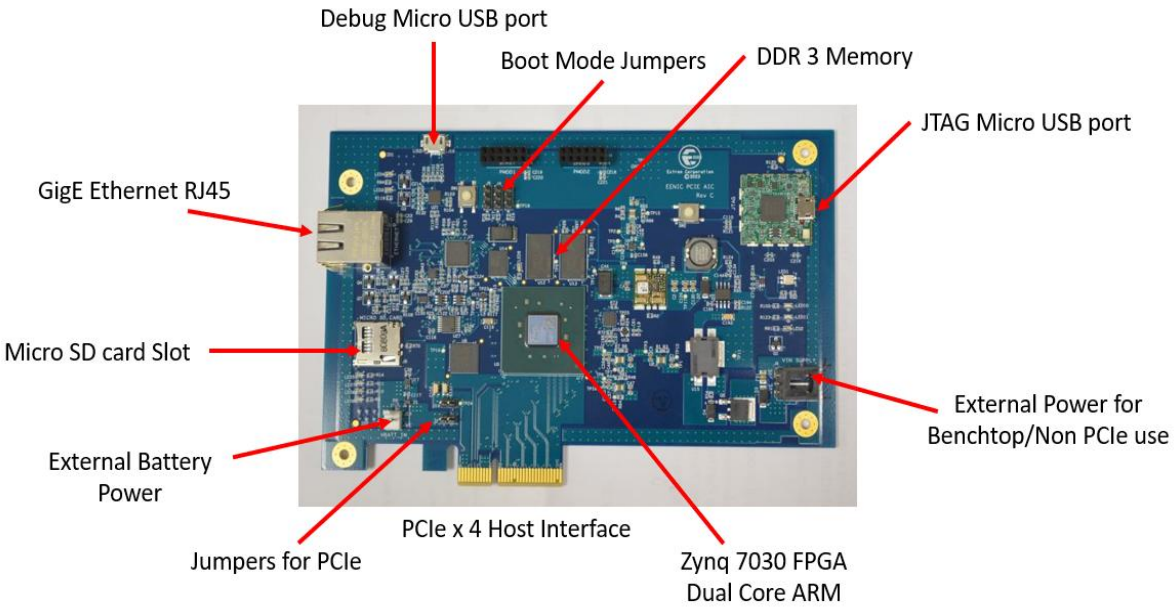
- Four standoffs
- 5 Jumpers
- A cable for benchtop powering up of the card

What is not included are micro-USB to USB cables to connect the JTAG port to the host computer and the debug port which allows access to the processor to the debug port. These cables are required.

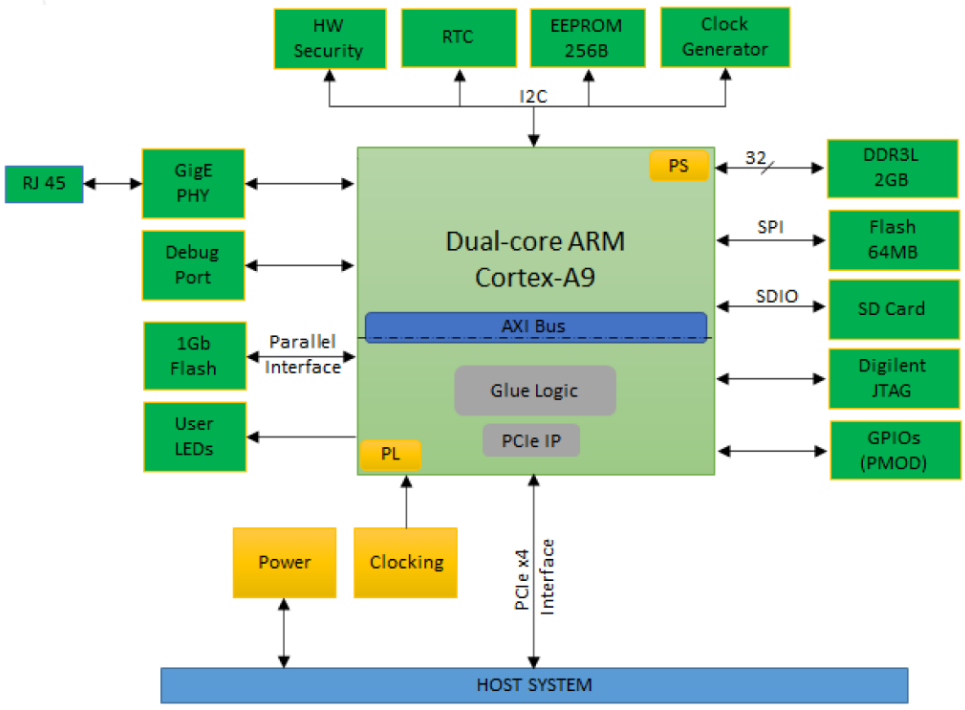
Also a free download of the Vivado software and the Xilinx/AMD ARM development software is required to start using the board.

NEVER CONNECT THE PCIe and EXTERNAL POWER AT THE SAME TIME

The following picture shows the board and its major interfaces:



The board can be powered through an external bench top supply or through PCIe interface. The overall block diagram of the card is shown below



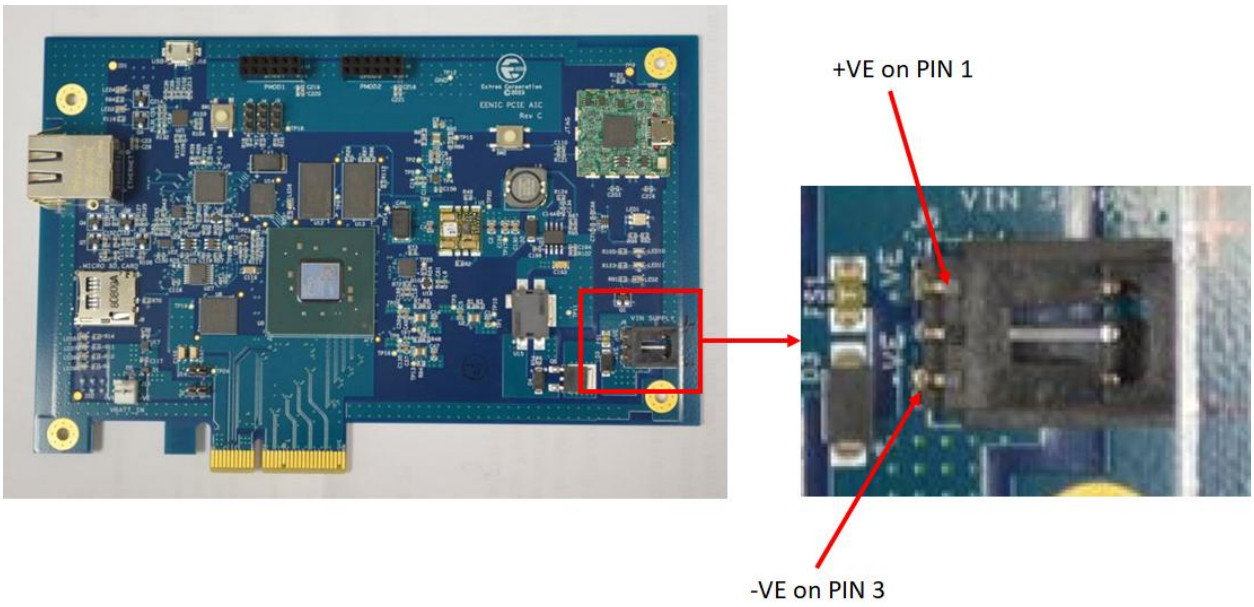
The next section shows how the board can be powered up and the usage of the board.

2.0 Quick Start

As described earlier the board can be powered up EITHER (NOT BOTH AT THE SAME TIME) through PCIe or through an external benchtop supply.

2.1 Benchtop Supply Operation

1. Need a bench top supply that can provide 12 Volts at 3 Amps
2. Mount the board on the standoffs with the FPGA side up
3. Use the cable provided to connect the +ve of the cable to pin 1 and -ve to pin 3. These are clearly labelled as +ve and -ve wires. Accordingly connect them to the benchtop supply

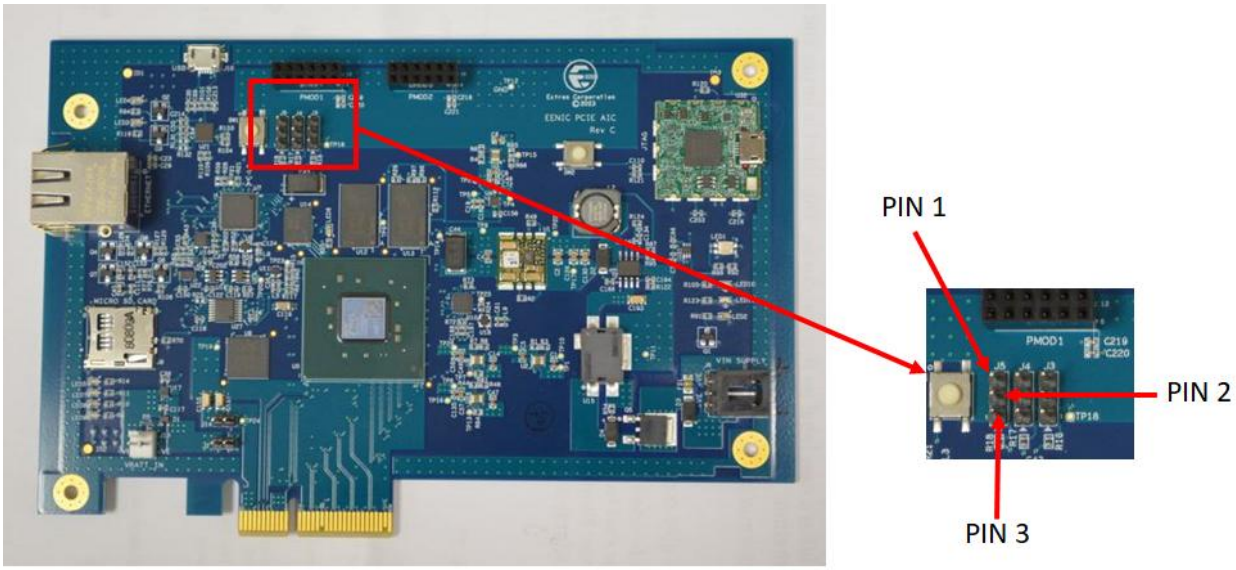


4. Connect the other end of the cable to the power supply (The supply should be set to 12 V @ 3A) or as close as possible (2% deviation is easily tolerated)
5. Connect the micro-USB cable 1 to the JTAG port and the other side to the PC USB port
6. Connect another micro-USB cable to the debug port on the card and the other side to the PC USB port

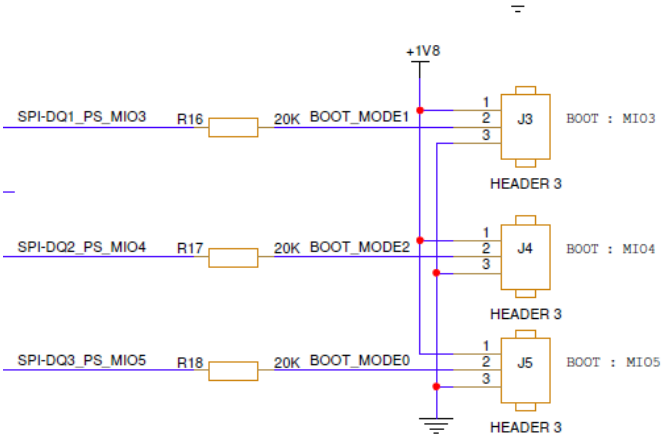
Both of these cables should be like the one shown below:

7. The next step is to put in the boot mode jumpers on the board. These jumpers are located towards the top of the board and are labelled J3, J4 and J5. The purpose of these jumpers is to determine how the card boots up (i.e. how the FPGA starts on power up and where it reads it's configuration from).

   Since the device is not programmed and nothing has been done with the card the configuration of the jumpers needs to be set to JTAG boot. So they need to be set to "000" as shown below:



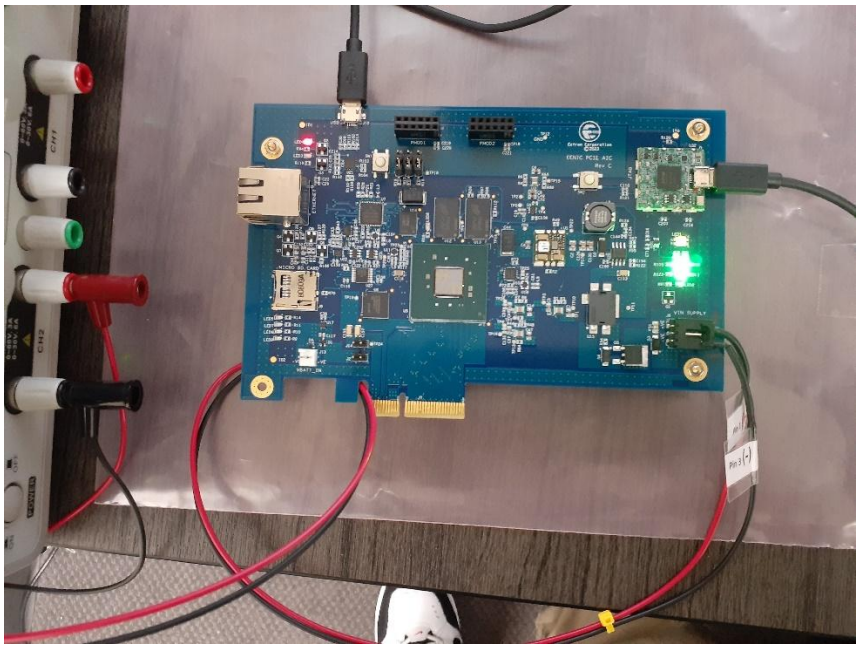
For JTAG boot pins 2 and 3 need to be shorted using the jumpers provided in the bag that came along with the board.



BOOT Mode	J5 MIO5	J4 MIO4	J3 MIO3
JTAG Boot Mode	0	0	0
NOR Boot	0	0	1
NAND Boot	0	1	0
Quad-SPI Boot	1	0	0
SD Card Boot	1	1	0

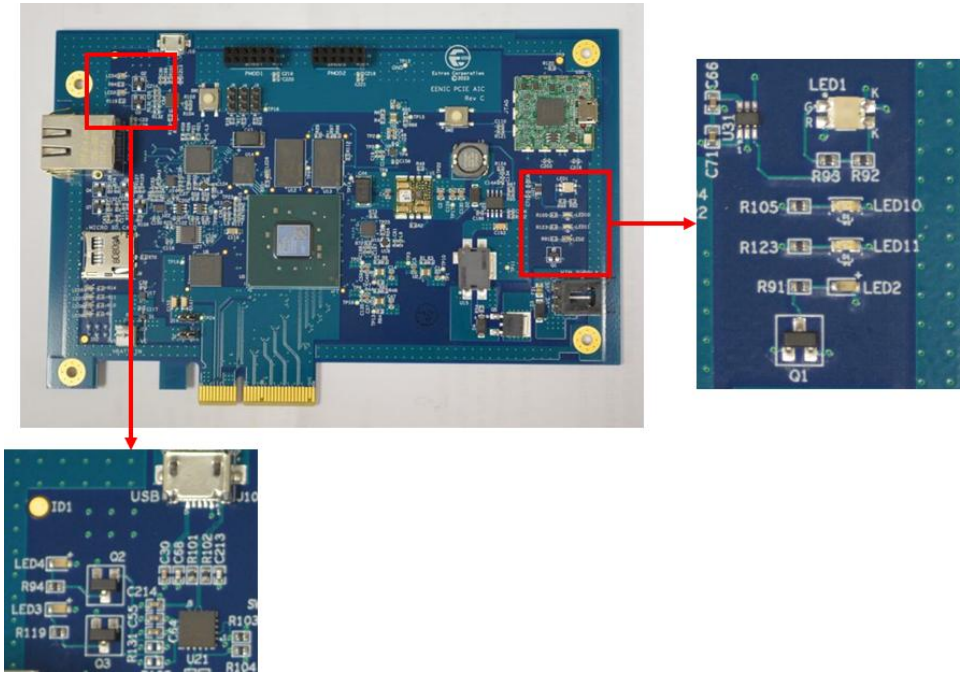
Grounding the boot mode pin according to the table shown in above makes the setup to be "000" for the boot mode selection.

So all the connections and jumper settings should look like the figure shown below when all the steps have been followed:



8. Power up the board.

9. The red led at the top left hand corner of the board lights up showing the debug port is active, the leds on the right hand side light up. If you press the reset switch at the top of the board next to the boot mode jumpers the LED



- **LED 1 is the init LED, it will glow green as long as the system is not in a reset state. Pressing SW 1 which is next to the debug port will turn it red. SW 1 is the processor reset switch.**

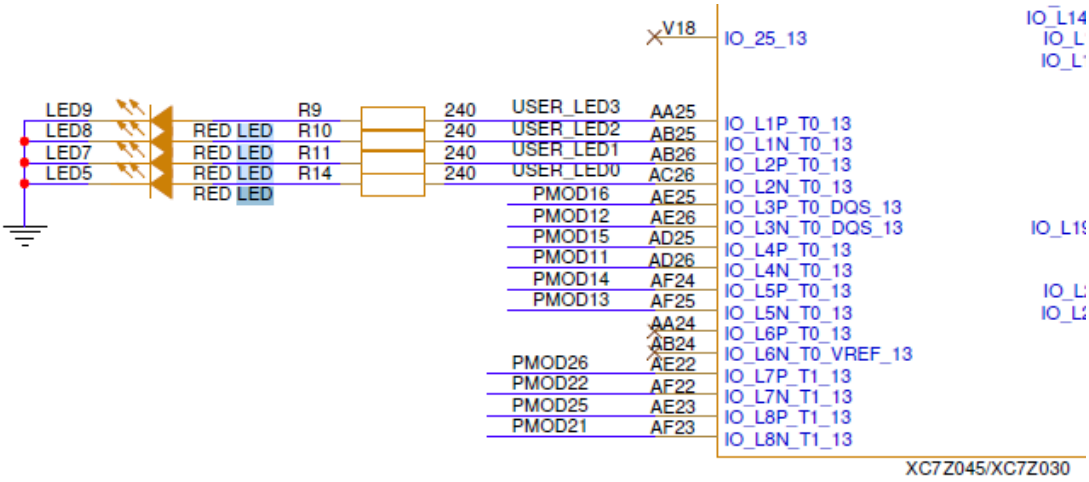
  Pressing SW 2 which resets the FPGA will also turns it red. SW2 is located next to the JTAG port.

  To turn it back to green press the SW 1reset switch again. The processor automatically comes out of reset after a second or so turning the LED back to green if SW 1 is pressed.

- **LED 2 will not be glowing but will turn red once the FPGA is programmed.**

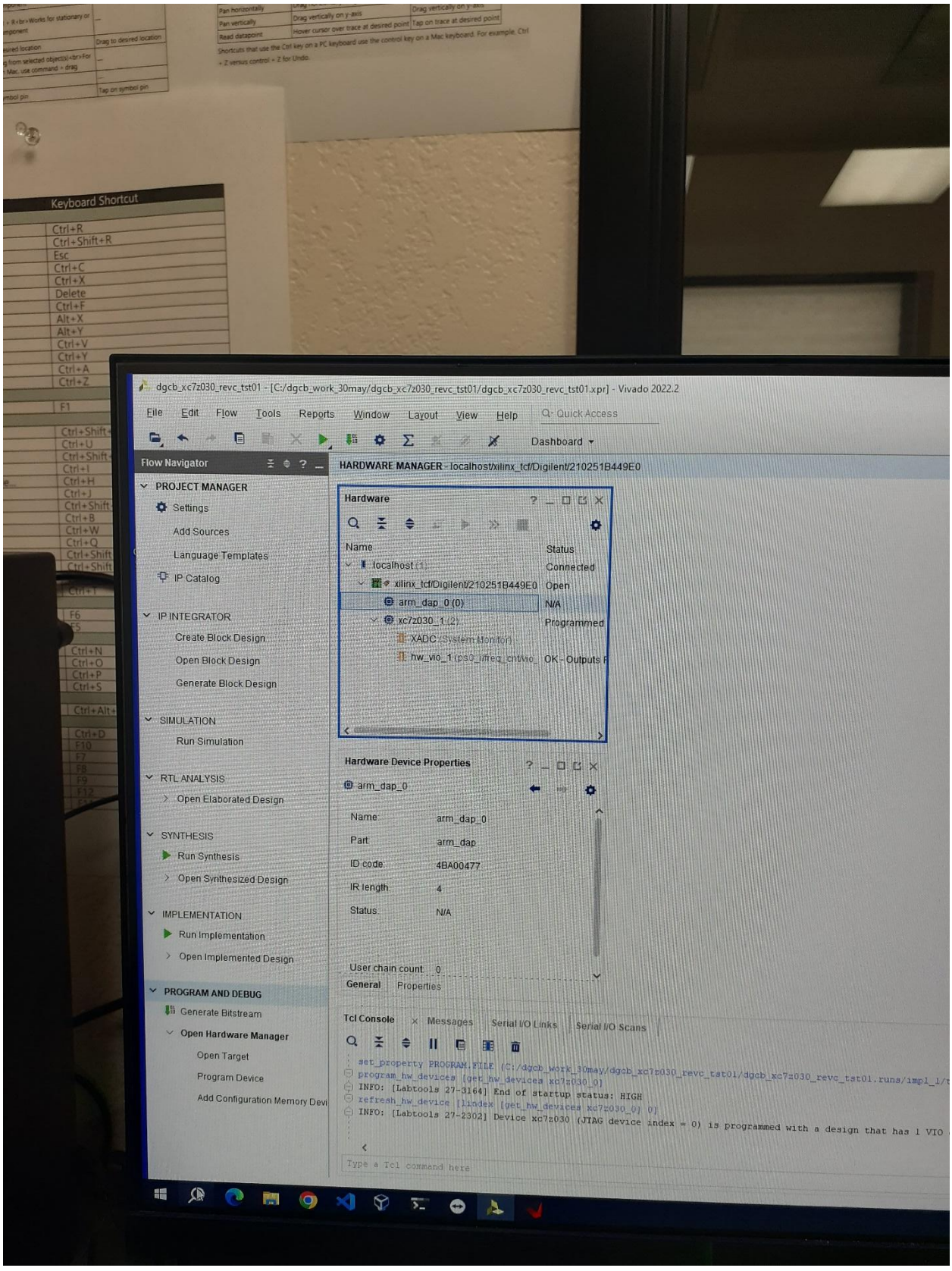
- **LED 3 and LED 4 are the Rx and Tx LEDs on the debug port**

- **LEDs 5,7,8 and 9 are user defined LEDs and are connected to the FPGA**



- **LED 10 and LED 11 will glow green at power up.**

10. **Start Vivado on the host PC after powering up and making sure the USB cables are connected to the board**
11. **Open hardware manager from the start window of Vivado**
12. **Click on open target from the window, the following should show up on the screen after clicking open target. In case this screen does not show up (which seems to be a temporary bug in the AMD software), programming the device will make the processor show up and visible in the software.**


Keyboard Shortcut
Ctrl+R
Ctrl+Shift+R
Esc
Ctrl+C
Ctrl+X
Delete
Ctrl+F
Alt+X
Alt+Y
Ctrl+V
Ctrl+Y
Ctrl+A
Ctrl+Z
F1
dgcb_xc7z030_revc_tst01 - [C:/dgcb_work_30may/dgcb_xc7z030_revc_tst01/dgcb_xc7z030_revc_tst01.xpr] - Vivado 2022.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Dashboard
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Devi
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210251B449E0
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210251B449E0
Open
arm_dap_0 (0)
N/A
xc7z030_1 (2)
Programmed
XADC (System Monitor)
hw_vio_1
OK - Outputs
Hardware Device Properties
arm_dap_0
Name arm_dap_0
Part arm_dap
ID code 4BA00477
IR length 4
Status N/A
User chain count 0
General Properties
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
set_property PROGRAM.FILE {C:/dgcb_work_30may/dgcb_xc7z030_revc_tst01/dgcb_xc7z030_revc_tst01.runs/impl_1/
program_hw_devices [get_hw_devices xc7z030_0]
INFO: [Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7z030_0] 0]
INFO: [Labtools 27-2302] Device xc7z030 (JTAG device index = 0) is programmed with a design that has 1 VIO
Type a Tcl command here

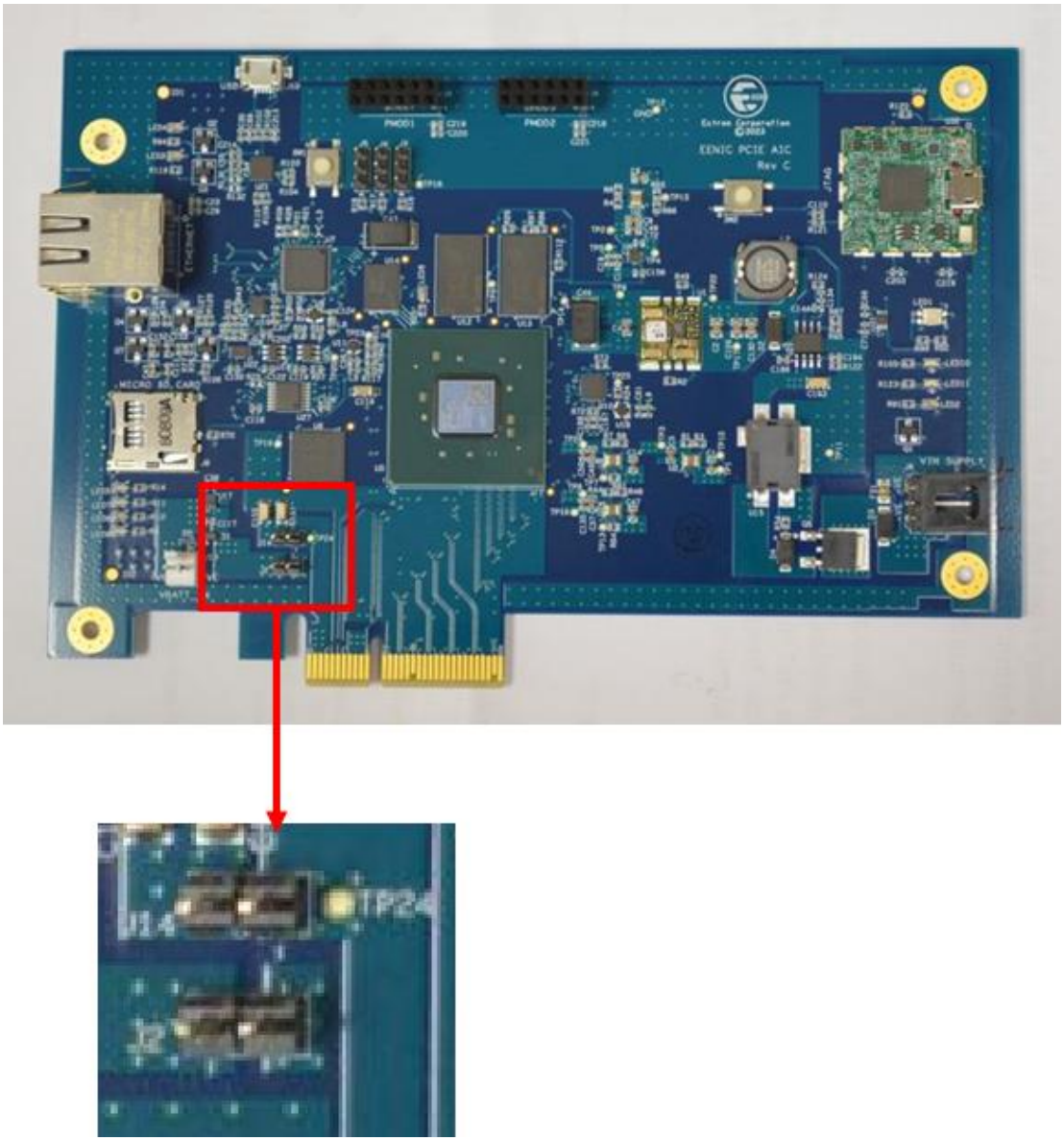
2.2 PCIe operation

For PCIe operation there are only two differences:

1. Remove the external power connector cable

2. Remove the stand offs

3. Short the Jumpers J14 and J2 which allow the card to draw the 12 V and 3.3 V from the PCIe interface

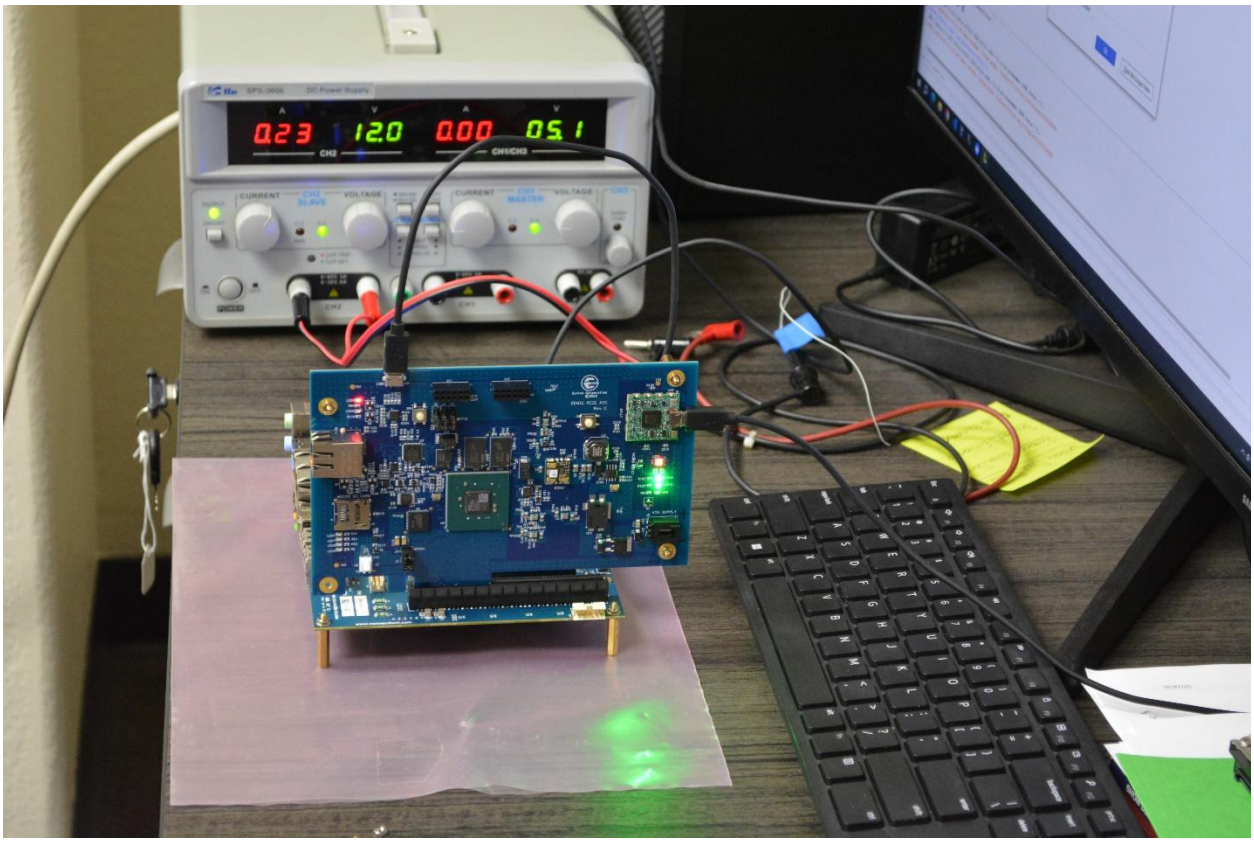


4. Turn on the Power and the card should have the same behavior

5. For driver development for the card we recommend Jungo WinDriver software

   WinDriver - Device Driver Development Toolkit | Jungo

6. When powered up through PCI Express the board should look the same



We have used a motherboard to power up the board in a PCIe slot without the CPU in the above picture, however this can also be inserted into a test PC.

List of Interfaces and their location in the SoC

UART (Debug Console Port) - PS

JTAG (Digilent JTAG-USB module) - PS

DDR3 Memory - PS

QSPI Flash - PS

Ethernet - PS

SD Card - PS

Parallel Flash - PL

PCI Express - PL

GPIO PMOD - PL

GPIO LEDs – PL

BOARD ID GPIO - PL

I2C Interface - PS

- RTC
- EEPROM (256 byte)
- Clock Generator
- Hardware security chip

Power On Built-in-Self-Test

QSPI Flash Boot

SD Card Boot

Petalinux Images and Boot