Venkata Srinivas Kiran Kumar Jasti

venkatajasti6@gmail.com| Phone (C): 8732882797| **LinkedIn**

SUMMARY

- Enthusiastic and motivated **Systems and Computer Engineer** with **+4 years** of professional engineering expertise in Database Management Systems, Information Systems and Organizations, signal processing, and wireless networking. Consistently recognized for technical troubleshooting skills used to resolve challenging technical issues rapidly and efficiently. Possess strong problem-solving, time management, written and verbal communication skills, and team leadership abilities. Team player who excels in fast-paced and challenging environments
- Solid graduate education with emphasis on electronics, software, device testing, and networking

WORK EXPERIENCE

Proctor, Carleton University, Ottawa — Sep'20 to present

- supervised test-takers in a virtual environment with a hands-on experience using Big Blue Button application
- assured adherence to the rules of the testing center by maintaining academic integrity
- demonstrated strong communication skills through writing technical reports and presenting creative solutions tailored to troubleshoot and diagnose exam support queries from students

Teaching Assistant, Carleton University, Ottawa — Jan'20 to Dec'20

- engaged one-on-one with students during office hours, resulting in an improvement of more than 10% in their grades
- managed and organized student grade book entries using Microsoft Excel which helped to generate graphical representations for evaluating student's performance. Created forums on CUlearn for general discussions
- Provided timely and appropriate feedback and guidance to 200+ students

Intern, Electronics Corporation of India Limited (ECIL), India — Jun'17 to Aug'17

- learned and acquired great knowledge of RTL design and verification using Verilog/VHDL.
- Developed System Verilog/UVM testbenches at Top/Sub-system/Block-levels
- Worked on designing pseudo random pattern generator using Verilog and increased the number of bits generated by reducing the complexity of pattern generator.

SKILLS

Hardware Modeling Languages	:	VHDL, Verilog, Network Design and Analysis, Circuit Design & Analysis, Embedded Systems, TCP/IP, Prototyping, Python, PCB design & Analysis, TCL Perl, System Verilog
EDA Tools	:	HSpice, Orcad Pspice 9.2/10.5, Xilinx ISE 8.1i, AFM, TEM, Raspberry Pi, Visual Studio, LabVIEW, Arduino
Programming Languages	:	C, C++, JavaScript, MongoDB, Node.js, Express.js, React, Assembly languages, SQL
Operating Systems	:	Unix, Linux, MS-DOS, Windows
Simulators	:	ModelSim, MATLAB Simulink, Synopsys VIVADO, cadence
Software	:	MS-office, MS-word, MS-Excel, MS-PowerPoint, AutoCAD, CAD, Ravit

EDUCATION

Master of Engineering (M.Eng. Non-Thesis), Systems and Computer Engineering **CGPA: 11.1/12** Jan'19 to Dec'20

Carleton University, Ottawa, Canada

- Relevant Courses: Advanced topics in Computer Communication, Networking, Internet of Things

Bachelor of Engineering (B.E), Electronics and Communication Engineering **CGPA: 8.0/10** Aug'14 to May'18

J.B. Institute of Engineering, Hyderabad, India

- Institutional rank holder (4^{th})

PROJECTS

Carbon Nanotube-based biosensor for ultrasensitive detection Dec'20

- Used Carbon nanotube as a sensing channel in a Field Effect Transistor configured Biosensor for the detection of viruses and bacterium
- Measured biosensor's sensitivity based on the resistance change in the sensing channel represented in V-I curves and simulated the model in **LabVIEW software**
- Performed Data Analysis on the **FBDB dataset** merged into **excel spreadsheets**. The performance metrics of the biosensor is visualized using pivot tables and charts. Analyzed results showed **94% sensitivity** of the biosensor by varied resistance

Automatic Collision detection in smart cars Mar'19

- Designed a system that can detect the obstacles and avoid collisions by measuring the distance between the obstacle and the vehicle using **ultrasonic sensors** embedded in the front, having a range of 5 meters and rotation angle of 180 degrees
- Fed information to the **raspberry pi circuit** which then executes the data and provides a possible alternative path
- Used a camera module to record the video and upload to cloud. And a **trans receiver module** to send emergency messages to the local emergency centers through radiofrequency broadcasting

Pseudo Random Pattern Generator Jun'17

- increased the number of bits generated by reducing the complexity of pattern generator. Concatenated 32-bit code words to get **1024-bit pseudo pattern**
- Designed in the front-end using Verilog software
- used in BIST (built in self-test) circuits to generate random input pattern to test any IC's. It is also used to generate security code while encoding the signals during satellite communication

CERTIFICATIONS AND ACHIEVEMENTS

- IETE Honor Society member Apr'16 to present
- Pseudo random pattern generator- Acclaimed as the best project (Received 1000 CAD) Jun'17
- Electronics Corporation of India Limited (ECIL) Intern Certificate Jun'17
- BHEL, Project Work Training (PWT) Certificate Apr'16
- ORACLE®, Certified Associate and Professional in JAVA Dec'15