# Muvva Venkata Kasi Raju

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7569943884
Fresher

Have a good experience in Verilog, system Verilog, and UVM with hand sonic, ability to do critical analysis

## Profile Summary

As a trained fresher, I am passionate about pursuing a career in VLSI, aiming to join a pioneering company where I can deploy my skills, acquire new knowledge, and contribute to collective progress.

## Education

2023, Full Time
**B.Tech/B.E., lakireddy balireddy college of engineering,** 7.4/10

2019
**12th, Andhra Pradesh, English,** 90-94.9%

2017
**10th, Andhra Pradesh, English,** 80-84.9%

## Projects

31 Days
**Interrupt controller design and verification**

**Working Tools:** GVIM, Verilog, APB interface, Model sim / EDA playground
**Description:** An interrupt controller is a device that helps a processor handle multiple interrupt requests from different sources. It can prioritize, mask, and acknowledge interrupts, and deliver them to the processor in a suitable way.
**Responsibilities/ Outcomes:**
1. realized the importance of Interrupt in a SOC & its execution mechanism in processor and peripheral communication
2. designed Verilog code of the Interrupt controller architecture with a processor and peripheral interfacing
3. developed different test cases for various interrupt handling possibilities

20 Days
**SPI design& verification**

**Working Tools:** GVIM, Verilog, Model sim / EDA playground
**Description:** Serial Peripheral Interface (SPI) is an asynchronous serial communication interface protocol used to communicate between microcontrollers and peripheral devices such as Sensors, SRAM,

and others. The data is transferred and received in the form of byte-by-byte communication with Full-duplex mode. SPI uses SCLK, MOSI, MISO and CS to connect master to slave.
**Responsibilities/ Outcomes:**
1. designed the SPI controller Verilog HDL
2. developed the test bench development and test case coding

25 Days

**Configurable Memory design and verification**

**Working Tools:** GVIM, Verilog, SV/UVM, Model sim /EDA playground
**Description:** Memory is a basic element in most of the electronic devices. In SRAM, data is stored in a flip-flop-based configuration, allowing for faster and direct access to data without the need for refreshing cycles.
**Responsibilities/ Outcomes:**
1. developed memory Verilog code with different parameters
2. developed TB Architecture using front door and back door access tasks
3. developed testcases in design verification
4. analyzed the waveform for checking memory write/reads

## Key Skills

Verilog HDL | Ethernet | UVM | Verilog | RTL Design | Debugging Skills | System Verilog | RTL Coding | ASIC Verification | digital | Digital Electronics | vlsi | Design Verification | spi | Apb | FIFO | C Programming Language | VHDL | EDA Tools | Mentor Graphics | Simulation | QuestaSim

## Internship

**SRC -e sollutions**
IOT using Rasberry pi
4 Weeks

Along with an exponential growth in connected devices, each thing in IoT communicates packets of data that require reliable connectivity, storage, and security. With IoT, an organization is challenged with managing, monitoring, and securing immense volumes of data and connections from dispersed devices. In addition to scaling and growing a solution in one location, cloud computing enables IoT solutions to scale globally and across different physical locations while lowering communication latency and allowing for better responsiveness from devices in the field.

## Language

| Telugu | English | Hindi | Kannada |
|---|---|---|---|
| Proficient | Proficient | Beginner | Beginner |

## Personal Details

| Date of Birth | Gender | Marital Status |
| --- | --- | --- |
| **4th June 2002** | **Male** | **Single / Unmarried** |

Address
**1-36B, P Venkatapuram(V)**

## Other Interests

Teamwork
Decision making
Ability to adapt new technologies quickly

## Extra-curricular Activity

Participated in LAKSHYA 2020 technical fest during graduation. Certified in the

CRUIZE6.0 competition conducted by LBRCE College.

## Declaration

I hereby declare that the information provided above is true to the best of my knowledge.

M. VENKATA KASI RAJU