Printed Circuit Board DOCUMENTATION

SCHEMATICS

- First foremost, working with the PCB not as much as tough, but it has some trickier part with the PCB Routing.
- Find a valid circuit diagram from the online or other's diagrammatic ideas with a concept of input and output and other parameters
- Try to find out which PCB Valid Licensed software is apt for the easier to design [i.e., either CADENCE or ALTIUM or KiCAD or EASYEDA etc.,] as per the industry standards.
- Try to understand the concepts of the appropriate software working.
- At the start, try to photocopy the provided circuit diagram / component connection diagram to the schematics area using the datasheets and software readme documents.
- After finishing, clear up the ELECTRICAL RULE CHECKING (ERC) Errors by correcting the issues faced.
- Save the file as <Schematics_ "FILE NAME "."FILE EXTEN"> and export the Net lists for the cross – verification.
- Export the file as the PDF format.

PCB:

- For the PCB exporting, you have to get the inputs with respect to the circuit provided.
- Inputs: Total Number of the Layers that PCB should incorporate and Type of stackup layers that make PCB proper routing.
- Proceed with the stackups in appropriate PCB.
- Then generate the Footprints / Import the appropriate Footprints by studying the appropriate datasheets.
- COMMONLY USED TRACING WIDTH : 2.5 Mils-20 Mils (0.0635 mm – 0.508 mm) { or something with respect to number of layers proceeded}
- COMMONLY USED TRACE CLEARANCE : 2.5 Mils – 10 Mils (0.0635 mm – 0.254 mm) { or something with respect to number of layers proceeded}
- Connect the Respective pads through the vias (any one of the 4 types) {if needed}.
- Logically thinking of such routing will result in neglecting the rat-line or net-line.
- Clear the Design Rule Checking (DRC) Errors which have generated.
- Try to incorporate the Copper Area Outline, if the Design has more the 4 layer Stackup.
- Process some working / IC labeling identification on Both TOP and BOTTOM SLICKSCREEN LAYERS and save the file.

- Save the File as PDF and Generate the Gerber file after senior's approval.
- Try to take all documents backup (such as Gerber, Bill of Materials , Schematics , Net lists ,PCB coverage , Pick / Place , etc.) In PDFs and Doc File and try to save the documents name with the respective dates to ignore the confusions.
- Try to save either 3D / 2D view as TOP AND BOTTOM view to verify the cross-correction as. jpeg or .pdf files respectively.
- Try to save the PCB information (either in .doc or .txt file) for the Fabrication Process.
- The Correction Loop continues till the fabrication ends it with the PCB Board printed.
- After Fabrication succeeded, kindly Test with any short – circutation caused with continuity Testing process.

  It is recommended to continue the study of basic concepts either by browsing or watching content videos in YouTube before designing the circuit:

  - PCB and its basics & Software, its basics.
  - Steps in Manufacturing of PCB boards in industry
  - SI/PI Integrity.
  - EMI/EMC Testing

PCB Basics:

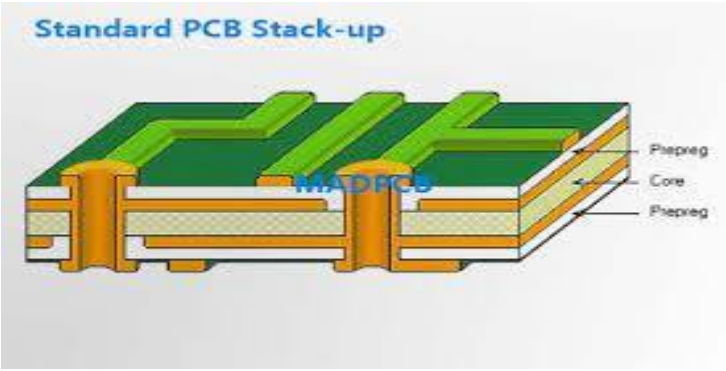
Before beginning the process, kindly view the Previous PCBs for the clarification.

Types:

- Single Layer PCB
- Double Layer PCB
- Multilayer PCB
- High Dimensional Interconnect (HDI) PCB
- High Frequency PCB

PCB Essentials/ Stack lineup:

- Top Silk screen Layer
- Top Solder Mask
- Top Copper Foil
- Pre- Preg Bonding Material
- Core
- Pre-Preg Bonding Material
- Bottom Copper Foil
- Bottom Solder Mask
- Bottom Silk Screen Layer



PCB Softwares used (Any 1)

- Autodesk Eagle
- KiCAD
- Altium
- Cadence Allegro
- PCB Web Designer
- EasyEDA (STD and Pro), etc.

Universal PCB:

Several Solder Pads and the most common types of connectors and communication elements.

Wire (W): To connect between the pads.

Ratline: The airline that yet to be wired between the two pads

Bus (B): The common connection between the two or more pads to the same ratline

Off – Page Connector: To intra-connect the wire with the same schematics pages

No- Connection: Good practice to provide the no-connect pins for the port not needed to connect in your design.

Electrical Rule Check (ERC) : Verify your design by checking for any open connection and floating pins leftover.

Net lists:

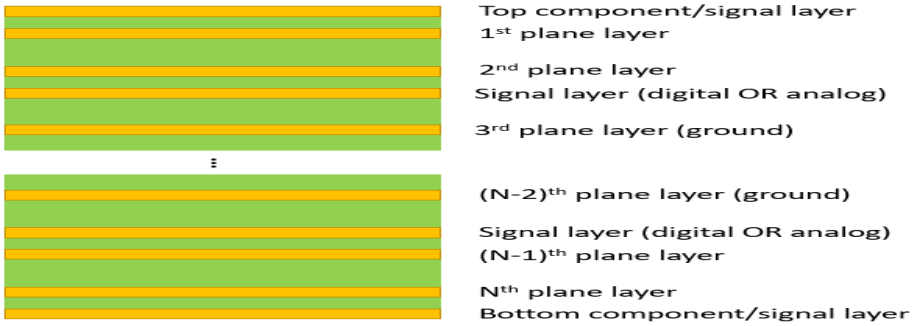
If a Net is connection between two components, a net list is simply a list of the connection that describes the circuit.

PCB Editor:

Board Creation:

Create the board outline that suites all components precisely well.

Stackups idea: Based on the design parameters stackups can be used



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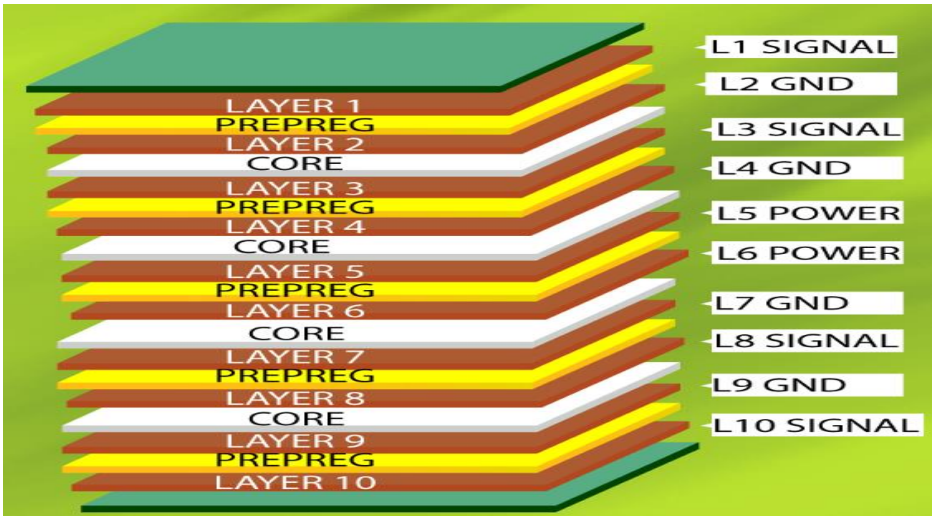


Design Rule Check(DRC) : Verify your design by checking for any no ratlines and according to the design parameters leftover.

Traces : Electrical Connections between the two components . They used to prevent the chemicals from externally
Slikscreen : For Adding the text and Graphics

SolderMask: Prevents Copper on the PCB from being oxidized over time and make it easier to solder by hands

Copper Fill or Copper Area : Large Area of the board that contains copper to prevent chemicals

FR4 Materials: (FR- Flame Retardant) Glass Reinforced epoxy laminate composite materials. (Very light and strong)

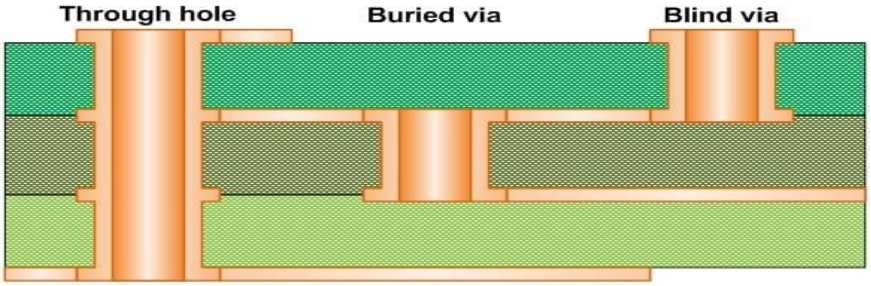
Pads and Holes: Component secured on the board on pads

Component Types:

- Through Hole
- Surface Mount Device (SMD)

Via (Vertical Interconnect Access) : Is a Hole that connect between the PCB layers. It sides covered with the Copper or Gold, that Trace to continue its route across layers.

Types:



Gold Fingers: Gold plated Conductors placed on the Edge of the PCB. Gold Fingers are useful for the interconnecting one board to another.

Multilayer PCB: For a Small and Medium Scale circuits, only two layers of PCB should be convenient.

Professional Equipment Circuit Designing and complex circuit like military equipment, computers, mobiles, etc.

Used Via and Hole Concept:

In Two layers, Through Hole places a vital role

In Multilayer (more than 2), the wiring is done by Blind and Buried Vias.

On the Ground and VCC layers, the interconnection cannot be done as all pins are automatically interconnected.

Footprint Methodology:

- Need of

- Number of Pins
- Pitch Between pins
- Width Between Pins
- Length Between Pins
- Offset of pins compared to package

$$= \frac{footprint\ size - package\ size}{2}$$

PCB Design Tool Tips:

1. Reference Designs: Use a reference designs. Typical Application PCB (or) Open-Sourced Design
2. Working in Blocks: Arrange the components before tracing the Areas on to a whole blocks.
   Move the components that used to be in specific places.
3. MOVE, ROTATE, REPEAT: Move and rotate the components to get the easiest way of the routing.

4. Important Traces first: First of all, make the traces for the important routes. It could gets started the traces to be given.
5. Use Trace Width Calculator: It may be provide the width of the traces that could easily carry the current for the path.
6. Use Net Labels: Use a net labels that provided by the DRC or ERC. It will be the good Idea.
7. Print on Paper: Check whether the application can be done physically printed on a paper without any errors found on naked eye.
8. Extra Footprints: Using the extra footprints to get matched to the workspace area as it until provide the test points for the real and natural applications.
9. Use a 3D Viewer: The 3D Viewer will get the idea of the product visually.
10. Use DRC : Using the DRC will enable you to manufacture capability checks for any errors that have been made.

Common Placement Good Practices:

- Do not Place the Through Hole and SMD Components on the same side of the PCB (Top and Bottom) . If placing Through Hole on Top Side , Then Place SMD on Bottom Side or Vice Versa.
- Try to place the components as per sections. (Meaning do not place the Power components in the controller section)

- Keep the Analog and Digital Section separately.
- Avoid the placement of controller section on edges, place it in middle.
- Place I/O or Thermal sections on any one of sides. Avoid keeping terminals of multiples.
- If there is any RF module in circuit, then try to keep it away from the controller section.
- Place Protection Components such as ,Fuse, TVS, etc., on the other edge of the PCB.
- For the routing the multilayer PCB (4 or more) , then you have to enable the allowance of blind and buried vias option. In below area, you can add the multiple sizes of the vias and traces as per requirements.
- Add Copper Planes on the TOP and Bottom Layer. As this could protect the sensitive components such as controllers, sensors, IC‘s etc., from external noise or EMI.

Critical Routing: Connect the pads on the planes provided as it improves the flow of current.

Crystal Routing: A crystal is basically a continually varying signal which is required for any microcontroller to operate and used as reference signal. This should be very close to the microcontroller and its trace should be short as possible.

Select Route traces and mention 10 mils .If its congested go with 8 mil or less. The ground of the crystal should be

connected to nearest ground pin. Placing a via will be an effective one.

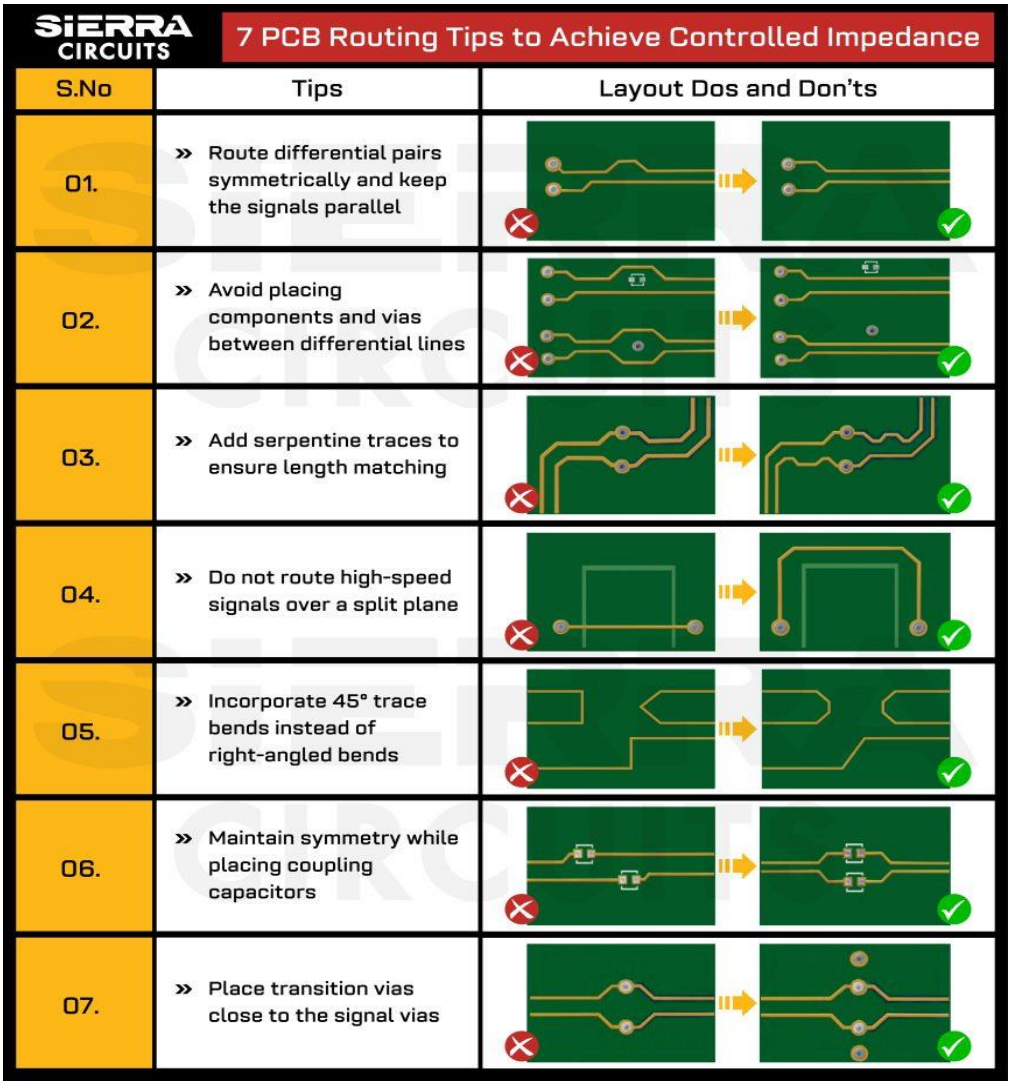
Decoupling Capacitors Routing: For Decoupling capacitors, via will go through the VCC planes as it will not disturb the other planes .Decoupling capacitors can be connected using the above technique.

Routing Technique:

- Orthogonal Entry
- 90° Angle / 135° Angle
- Using various types of Vias.

Differential Pairs:

The most critical traces in routing are differential pairs. Both wires in differential pairs must be identical in length and width; gaps must be 5 times the width of differential pairs.



Fiducials: These are normally not connected In the circuit, by they are required as the reference during manufacturing to indicate the proper orientation of the board . It will also help the placement components.

It is the circuit pattern recognition mark or marker.

Common Routing Practices:

- Route high speed signals over solid ground plane.

- Avoid the hotspots by placing vias in a grid.
- Keep trace bends at 135° instead of 90° avoid acute angles.
- Increase the spacing between traces to avoid cross-talk.
- Avoid long sub traces by implementing daisy chain routing
- Do not place any components or vias between differential pairs.
- Incorporate length matching to avoid skew between differential pairs.
- Do not route signals over a split plane.
- Separate analog and digital ground planes to reduce noise.
- Spilt the layouts virtually between analog and digital grounds
- Keep the trace width as per the size of discrete component.

Stitching Capacitors (10nF ≈100nF):

Enables the return current to travel from one reference plane to another .The capacitor should be placed closed to signal path so that the distance between forward and return path are kept small.

This 0.1µF stitching capacitor, without parasitic resistance (ESR) and parasitic inductance (ESL) serves as a signal return path in transmission line. Capacitor

should be placed close to the signal path between source and sink.
For best results, a designer should incorporate at least four layers PCB.

Bill of Material (BOM) File:

- Serial Number
- Part Description
- Designators matching the Schematics
- Quantity of Parts
- MPN
- VPN
- DNI (Do Not Install) Components (If any)

Keep out Areas:

- You want to exclude certain areas for your PCB from having copper files, tracks, or vias .Such Zones area called as Keep out areas /Zones.
- Use “Add a rule area “tool to draw a keep out zones.

Position File (or) Centroid File:

Automatic assembly of a PCB .This file tells a Pick and place Machine (PNP) where to place each components in what orientation.

Layers Basics: (Ki-CAD)

Front and Back Copper layer: This is where all visible copper tracks will be.

Front and Back Adhesive Layers: Applying any type of adhesive. Sometimes certain PCB parts have to glue together.

Front and Back Paste Layers: These layers contain locations where the solder paste should be applied on PCB. It is also used to create stencil.

Front Silkscreen and Back silkscreen: A silkscreen is a layer that contains all text labels. You usually see them as a white text on PCB

Front Masks and Back Masks : This tells where to and where not to apply the solder masks material .It is a paint like insulating material that protects copper layer from oxidation.

User. Drawings: This is auxiliary layer where you can place additional drawings which are not used for Fabrication.

Edge cuts: This layer contains the board outline and other cuts on PCB. The board outline determines the physical size and shape of PCB.

Steps to Review the PCB Layout / Design:

1. Before constructing the layout, verify the schematic drawings and BOM, Footprint dimensions assignment of DNI components, polarity, etc.
2. After finalizing the design, visually compare the schematics, constructed circuits to identify any errors. Run a DRC from the layer stack up to the components placements subsequently clean up the PCB layout to remove the identified errors.
3. Finally check for the missing data in production files before sharing the white fabrication house.
4. The arrangement of ground, signal and power layers is to produce an accurately functioning circuit.
5. If you planning for installing casing, ensure its dimensions meet all the requirements.
6. Placing Polygons (Copper pores) are the areas around the components /traces filled with copper. They are created only on signal layers.
7. Ensure no open nets are in circuit if any unconnected line, its length should be as short as possible.

Multiple sheets:

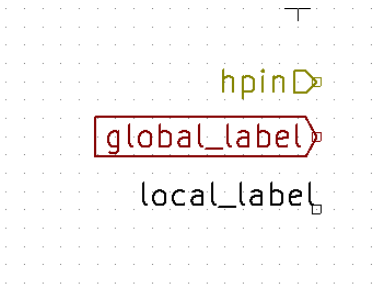
Hierarchical sheets will be acts like a subsequent in a MATLAB simulink. We can add multiple or delete the subsequent subsystems / sheets.

Rescuing the Cached Objects:

By default, KiCAD loads symbols from the Project Libraries according to the set path and library order. This can cause a problem when loading a very old project. If the symbols in the library have changed or have been removed or library no longer exists since they were used in the project, the ones in the project would be automatically replaced with the newer versions.

When the project is saved , a cache liberey with the contents of the current library symbol is saved along with the schematic . This allows the project to be distributed without the full libraries.

Electrical Connection between the hierarchical sheets:



The connections between the sheets are made with labels.

Local Label: only make connection within the sheet. Therefore a local label cannot be used to connect between sheets.

Global Label: make connection anywhere in schematic, regardless of sheet within file.

Hierarchical label: connect to hierarchical pins, assemble in parent sheet. Hierarchical designs rely only on H.labels and

pins to make connections between the parent sheet and child sheet.

CADSTAR PCB :

E- Nets : (Electrical Nets)

While a (logical) net comprises a set of nodes that are connected together on a schematic, an E-net describes a complete DC or AC current path, even if it passes through resistors, capacitors, inductors or diodes.

Benefits:* Gives a complete picture of what happens to electricity passing through.

*Very important for high speed design because everything on an electrical signal it carries.

Reinforcing Vias:
Otherwise known as “Stitching Vias” as it connect conductor areas on different PCB layers together in definable position.

Benefits: It makes easier to avoid errors such as overlapping via clearance gaps that create plane discontinues.
Ferrite Beads:
Also known as Ferrite clamp. It’s a passive device that improves your PCB’s power quality, designed to suppress high frequency signals on a power supply line. This is typically placed in power supply / ground line pair that’s incoming / outgoing to/ from a specific line.

Helps to reduce the EMI emitted from the board. Use of NiZn or MnZn beads. Nominal value of bead will be 100 ohms in 100 MHz

Tab Routing:
In Tab Routing Polarization, a router is used to cut through the FR4 between boards. Small tubs are left behind to hold boards together during assembly. These tabs can be used/ broken apart using depanelization tools, or carefully by hand.
Most of the time, the tabs of tab rate panels are perforated with a series of holes to make it easier to separate the boards
Routing: It is a layout of copper traces based on net lists. It can be performed interacting or automatically.

IT IS ESSENTIALLY PREFFERED MANUAL ROUTING UPON AUTO-ROUTING.

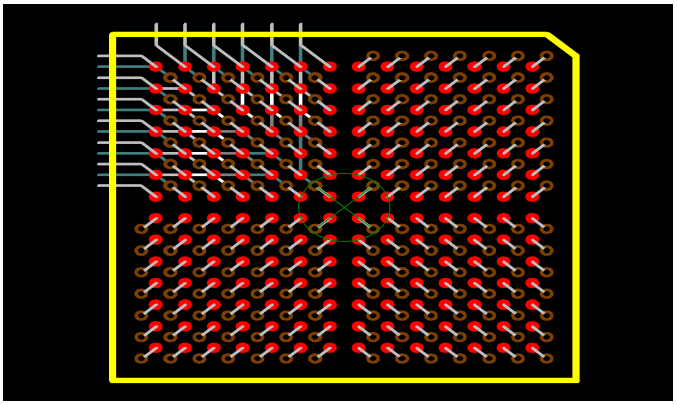
PCB Recommended Capability (4layers):

Free DFM Checking
Copper Thickness: Max to 6 oz inner copper
12 oz outer copper
Min Hole: 0.15mm by Mechanical drilling
0.1mm per layer
PCB thickness: 0.4mm - 6.5mm (1.65 mm preferred)
Surface Process: Immersive Gold, HASL-LF, Hard Gold, Immersive Tin, etc.

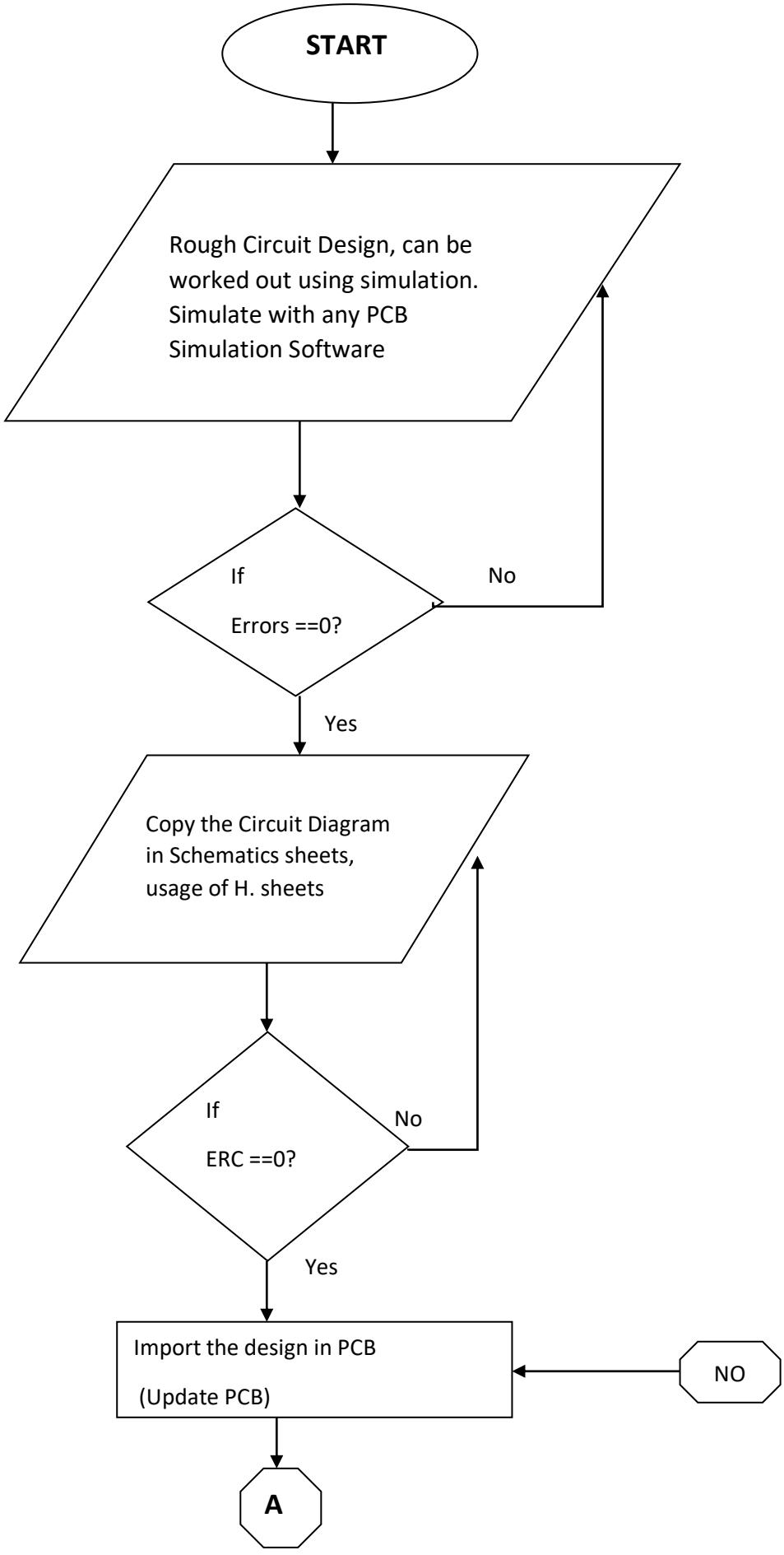
Solder Mask: Green, Yellow, White, Black or Custom
Silkscreen: White, Black, Yellow or custom.

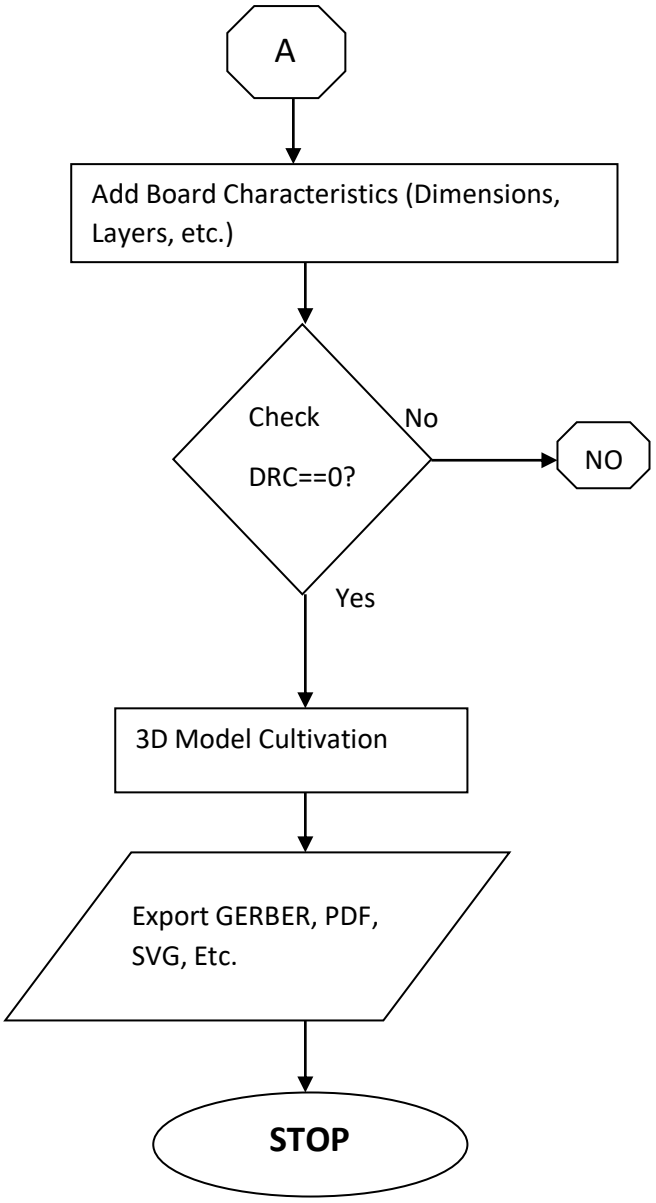
Generally, through hole, buried, blind holes are used to connect layers. There are more buried and blind holes than double side boards.

Note: When there is a BGA (Ball Grid Array) Package, The outer 2 rows can be directly pulled out to go to the top layer. The third and fourth layer can be drilled to go to the bottom layer, and fifth and sixth layer can be drilled to the bottom layer. However, inside power and ground layer cannot go out. An additional layer in design is required and two more layers are added.



PCB DESGIN WORK FLOW CHART (CONCEPTUAL):




A
Add Board Characteristics (Dimensions, Layers, etc.)
Check
DRC==0?
No
NO
Yes
3D Model Cultivation
Export GERBER, PDF, SVG, Etc.
STOP

File Formats:

Gerber (RS-274X) [VITALLY USED]{.gbr OR .gb}: The Gerber Format is an open, ASCII, Vector format for Printed Circuit Board. It is the default standard used by PCB industry software to describe the printed circuit board images, copper layer, solder mask, legend, drill data etc. It is the 2D representation that assists the manufacture to place components, solder mask, silkscreen layers, etc.

PNG (Portable Network Graphics){.png}: It can be saved as the image file for web processing which be lower resolution than .jpeg or .jpg formats. It is widely used on websites to display high quality digital images.

SVG (Scalable Vector Graphics){.svg}: It is a web friendly vector file format. As opposed to pixel based roster files like jpegs. Vector files store images. It is a tool for displaying two dimensional graphics , charts , and illustrations on websites, etc.

DXF (Drawing Exchange Format or Drawing Interchange Format){.dxf } : It is a type of vector file that developed based on CAD data file format. Many engineers used this type of AUTODESK file for 2D and 3D drawings during product designs.

ELECTROMAGNETIC INFERENCE (OR) COMPATIBILITY (EMC):

The capability of the electric and electronics systems, equipments, and devices to operate in their intended electromagnetic environment within the defined margin of safety, and at design levels of performances, without suffering or causing unacceptable degradation as a result of electromagnetic interference.

ELECTROMAGNETIC INTERFERENCE:

The process where disruptive electromagnetic energy is transmitted from one to another electronic device via radiated or conductive paths.

- Radiated Emissions: The component of roughly 10kHz to 100GHz, energy is transmitted through a medium, usually a free space as an electromagnetic field.
- Conducted Emissions: The components of energy transmitted as a propogative wave generally through a wire or interconnect cable. LCI {Line Conducted Interference} refers to the RF energy in Power Cord.

SUSCEPTIBILITY: The measure of a device ability ti be disrupted or damaged by EMI exposure.

IMMUNITY: The measure of a device's ability to withstand EMI exposure and still operating at a designated level.

Electrostatic Discharge: (ESD) A transfer of energy/ electric charge between the bodies of different electrostatic potential in proximity or through direct contact.

Radiant Immunity: The ability to withstand electromagnetic energy which is propagated through free space.

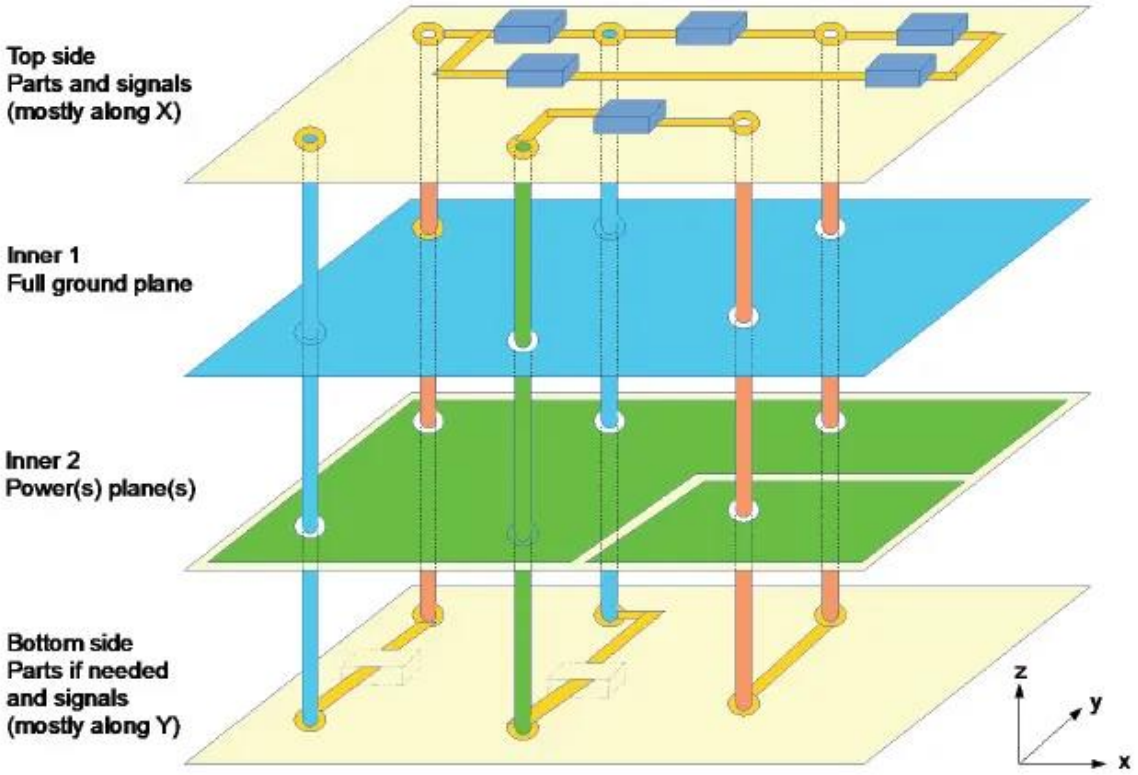
Conducted Immunity: The ability to withstand electromagnetic energy which enters through external cables and connection (power signal).

Contaminant: Keeping RF energy inside of an enclosure by providing a metal shield or plastic housing with RF conductive plant. Similarly, external energy can be kept out.

Suppression: Design techniques which reduce or eliminate RF energy from entering or leaving without using a standard method like shield or metal chassis.

2 LAYER BOARD ROUTING TECHNIQUES:

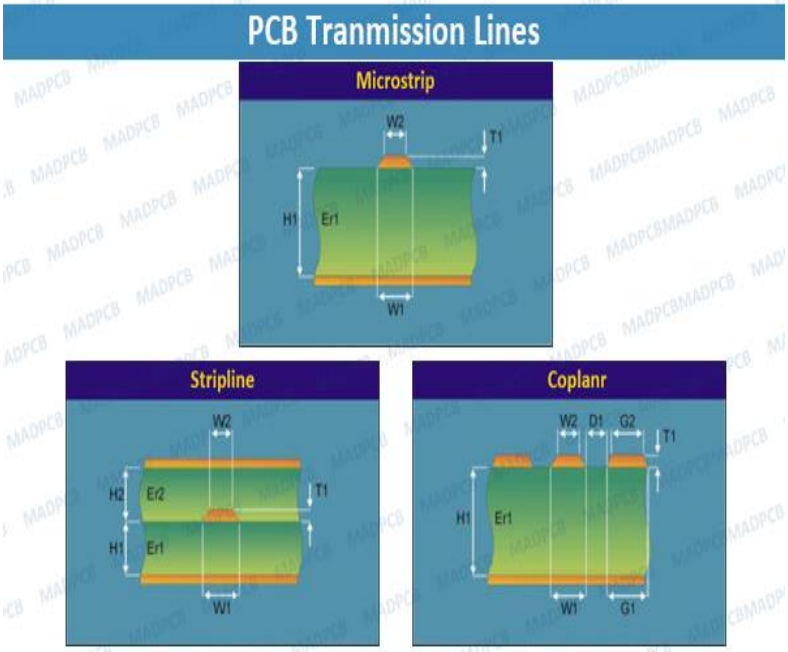
- Route power traces radically from the power supply.
- Route Power and Ground traces parallel to other.
- Signal flow should be parallel to ground.
- Don’t create current loops by tying different branches together.



MUTILAYER BOARDS ROUTING (MORE THAN 2 LAYERS):

- The boards are formed by the etching several double sided boards and then gluing them together with the material called pre-preg.
- The thickness and materials for both core and the pre-preg can be specified and controlled vias (or) holes which are electroplated after drilling and connect the different layers.

TRACES TYPES:



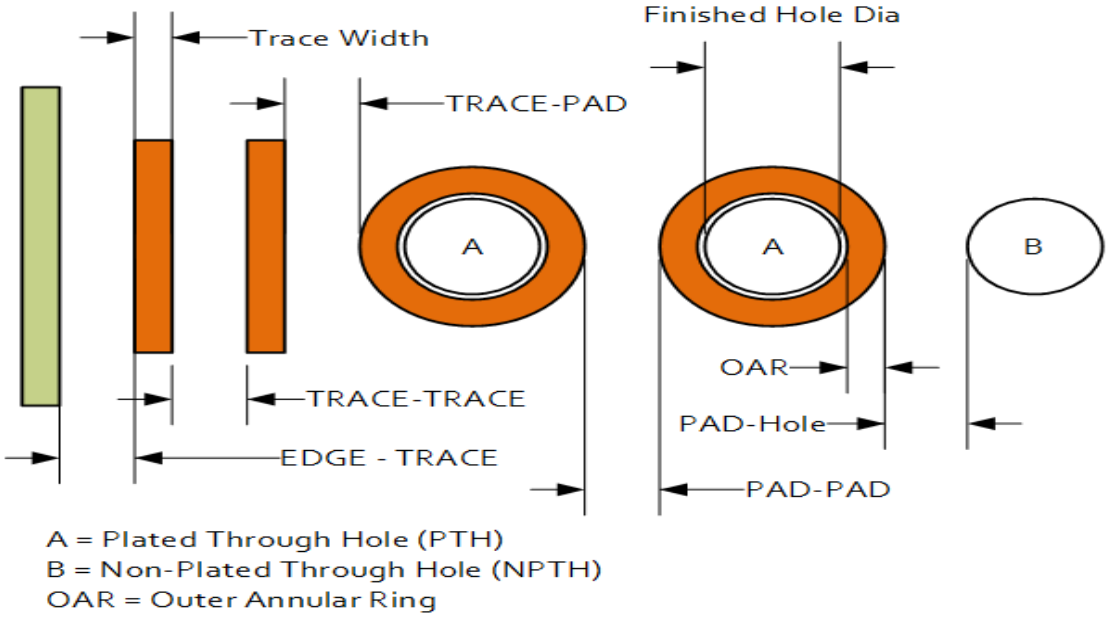
Microstrip: Faster Signals possible due to the lower capacitive conducting, but greater radiated RF.

$L_0 = Z_0{}^2 C_0$ (pH/in)

Stripline: Greatly reduced RF emissions but slower signals.

$L_0 = Z_0{}^2 C_0$ (pH/in)

TRACES AND VIA CHARACTERISTICS :



EMC FUNDAMENTALS:

Coupling Path is frequently dependent upon:

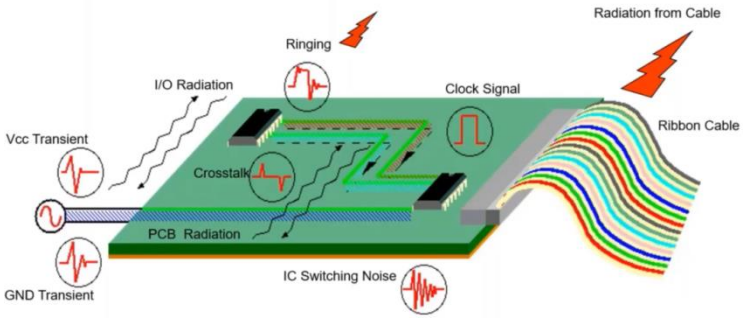
1. High Frequencies (Radiative)
2. Low Frequencies(Conductive)
3. Boundary is typically about 30MHz.

5 ASPECTS TO EMC when finding the Problems:

- Frequency
- Amplitude
- Time
- Impedance
- Dimensions.

PCB's Radiate RF Energy:

- Digital Signal with fast rise/ fall times contains very high frequency components even for the low clock frequencies. $F_{max} = \frac{1}{\pi \epsilon_r}$
- Z_0For air is about 377ohms.
- Discontinuities in RF return path $Z_{PCB}^{RF} \gg 377\ ohms$.
- RF current leaves in the board in favour of air = EMI.



EMI SUPPRESSION:

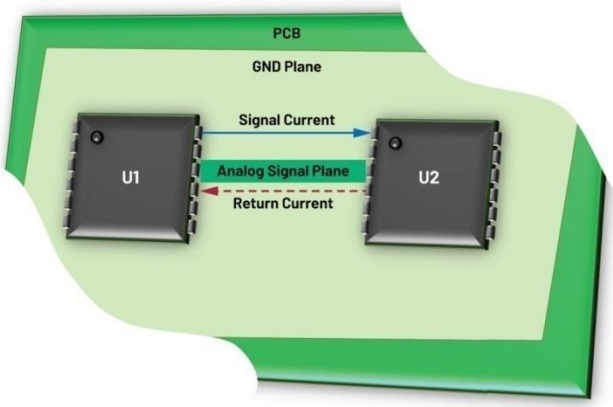
- Image planes
- The 20H rule
- System Level Grounding
- Portioning.

IMAGE PLANES:

A Layer of copper (either a voltage or a ground plane) which physically adjacent to the signal routing plane. The image plane provides low impedance path for the RF currents and reduces the EMI emissions since the RF currents use the planes instead of air.

Image Plane Violation:

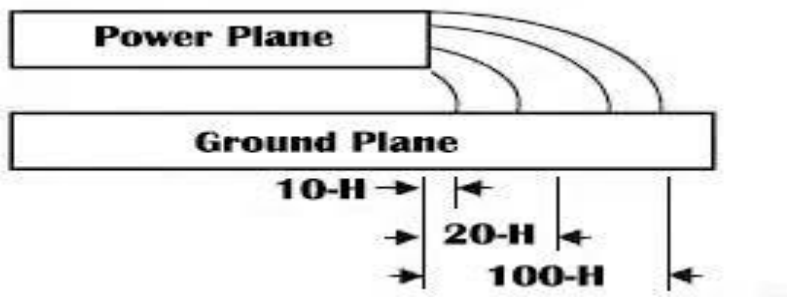
Routing traces in the image plane will create slots in the RF return path and create a large loop area and potential EMI.



THE 20H RULE:

- RF currents firing between the power and ground planes at the edges of the board can result in RF emissions.
- Reducing the size of the power plane with respect to the ground plane will reduce these emissions.
- This increases the intrinsic self resonant frequency of PCB.
- **It is recommended that the ground plane should exceed the power plane by 20xH, where H is the total thickness between power and ground plane.**

- 20H provides for approximately 70% reduction of the fringing flux and changing to 100H will provide about 98% reduction in void area.



- If power pin needs to be located near edge of the board, then it's okay for the plane to extend to 20H void to surround the pins.

SYSTEM LEVEL GROUNDING:

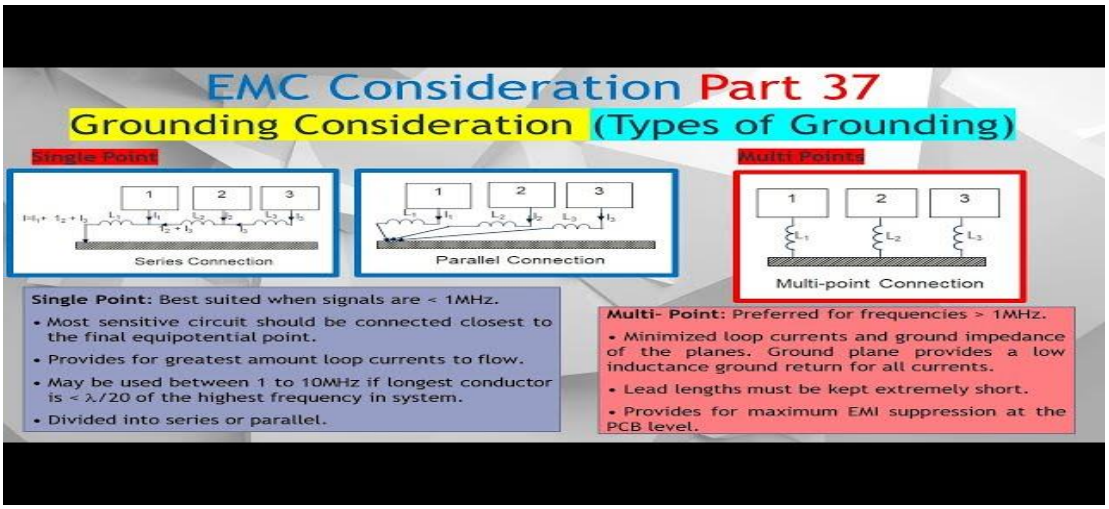
Three main system level grounding methods:

1. Single point grounding:
   Either series or parallel connection
   Best for frequency below 1MHz.
   Has the largest amount of the ground loop currents.

2. Multipoint Grounding:
   Preferred for frequency above 1MHz.
   Minimizes loop currents and ground impedance of planes.
   Lead lengths must be kept extremely short.
   Provides for maximum EMI suppression at the PCB level.

3. Hybrid Grounding:
   A mixture of both Single – point and Multi-point Groundings in the same system.
   Ground loops cause RF energy to be radiated when high inductance returns are provided.

In a multipoint grounding; the distance between the screws should not exceed λ/20 of the highest edge rate on the PCB.



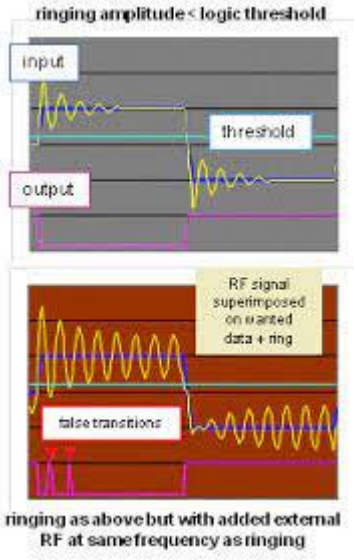
PARTIONING:

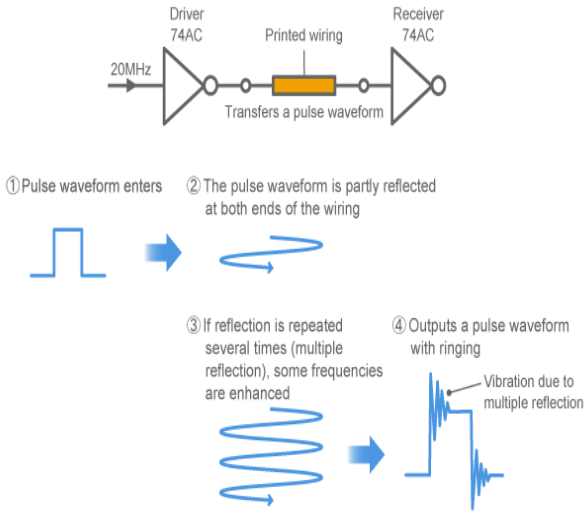
It consists of breaking a broad up into functional area with respect to the bandwidth of the functional block. Grounding connections are made around the perimeter of each functional block using spring fingers, screws, gaskets, etc. provided that the method has a sufficiently low inductance between the ground plane and chassis ground.

SIGNAL INTERGITY

- **RINGING AND REFLECTION:**
  Transmission line properties which occurs between the source and load.
  Possible causes:
  I. Changes in Trace Width.
  II. Lack of Terminations.
  III. T-Stubs, branched and Bi-Fabricated traces.
  IV. Connector transitions.
  V. Changes in traces impedance.

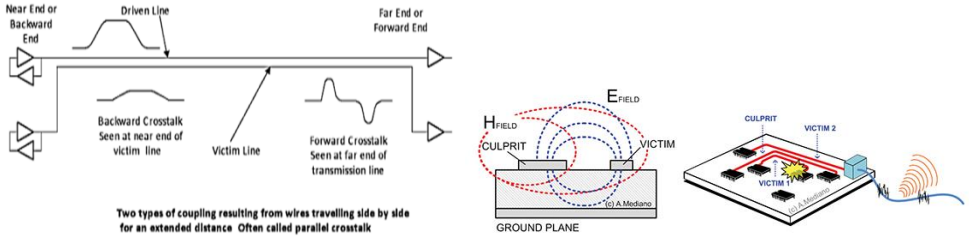
  Signal Distortion:





  - ✓ Ringing is minimized by proper terminations
  - ✓ Rounding means the nets is over-damped .Don't forget about the shunt capacitance of the trace as well as load capacitance.

- **CROSS-TALK: (aka Board Level EMI)**



  - ✓ Crosstalk is a signal integrity issue that occurs when the signal from one trace couples with another trace, causing interference. There are three essential principles of crosstalk: capacitive coupling, inductive coupling, and conductive coupling.
  - ✓ Cross talk requires a 3Wire Circuit.
  - ✓ Terminating resistors with a common pin is susceptible.

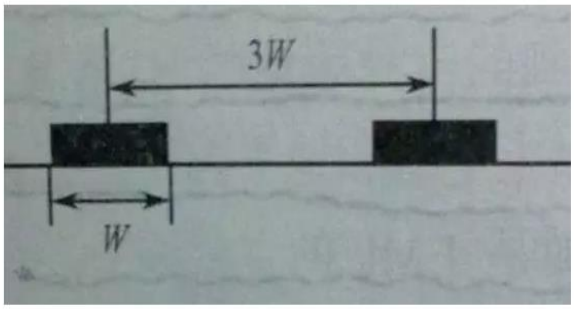
Preventing Measures:

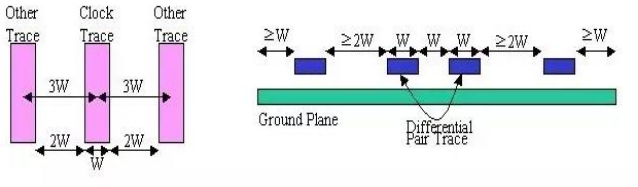
- ➢ Decreasing the trace separation will increase the mutual capacitance C_m and crosstalk.
- ➢ With parallel lines, longer parallel lengths increase the mutual inductance L_m and crosstalk.
- ➢ Decreasing the rise time of the signal, increase the crosstalk.
- ➢ Solutions:
  - Group and locate logic devices across to functionality.
  - Minimize the routed distance between components.
  - Minimize the parallel routed trace length.
  - Locate components away from the Input /output interconnect and other areas susceptible to data corruption.
  - Reduce trace impedance and/or signal drive level.
  - Avoid traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling (The 3W Rule) or use guard traces.

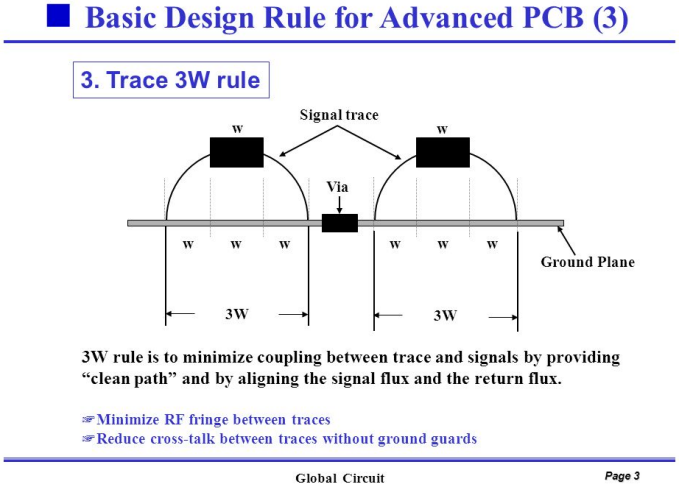
The 3H Rule:

This rule for trace separation will reduce the cross-talk flux by approximately 70%.

The distance of separation between traces must be three times the width of traces measured centre line to centre line.







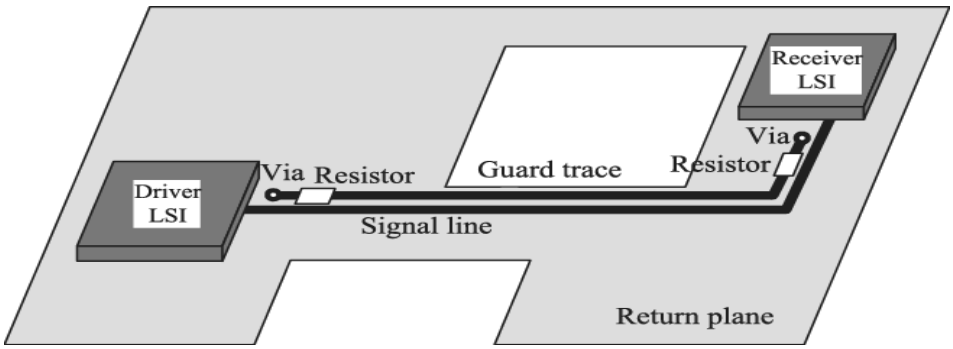
Guard /Shunt Traces:

Guard traces surround the high – threat traces (clocks, periodic signals, differential pair, etc.) and ground plane. They are very useful in 2 layer board.

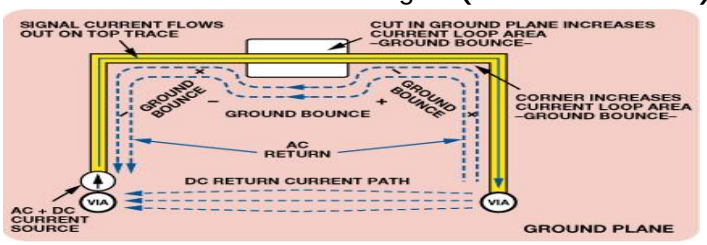
The guard trace should be smallest tolerable manufacture spacing from the signal.

If a ground plane is available, make ground connections no further than λ/20 apart, where$\lambda = \frac{1}{10 f_{max}}$.

Shunt traces are the traces located immediately above a high threat trace and follow the trace along the entire route. They are best used in multilayer (6 or more) boards.



- **POWER AND GROUND BOUNCE:**
  - Ground Bounce is caused by the simultaneously switching of drives in an IC package and may cause functionality as well as EMI Concerns. Ground bounce presents a situation where the ground reference system is not a constant 0V reference value.
  - Be sure to provide a separate ground connection for each ground pin directly to the ground plane. Connecting through ground plane turn together with a trace to angle via defect the purpose of having independent ground leads on device package.
  - Also, choose component packaging carefully use the device with a ground reference in centre of device to rotate the L_{gnd} (4ntt or 15ntt)



BYPASSING AND DECOUPLING:

- Capacitor usage and Resonance
- Parallel Capacitors
- Placement.

Types of capacitor usage:

I. Bulk: used to maintain constant DC voltage and currents when all signal pin and switch. Also prevents power dropout due to the $\frac{dI}{dt}$ .Current stages/surges from the components.

II. By-passing: Removes unwanted common node RF noise from components or cables by placing an AC short to ground. This keeps the unwanted energy from entering a protected area as well as limiting the Bandwidth. It is also used to divert RF energy from one area to another.

III. Decoupling: Removes RF energy injected into the power planes from high frequency components consuming power at device switching speed. They also provide a small amount of energy to function as localised bulk capacitors.

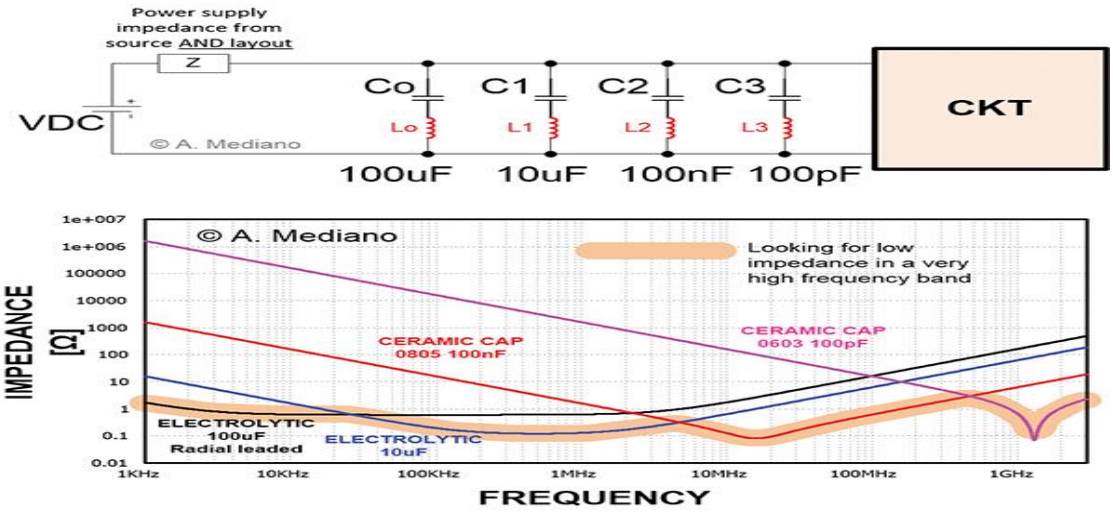
Resonance: Capacitors really have a ESL (Equivalent Series Inductance) and ESR (Equivalent Series Resistance).

- Through Hole Components: ESL ≈35nH and ESR ≈50Ω.
- Surface Mount Components: ESL ≈1nH and ESR ≈5mΩ.

Parallel Capacitors:

- Parallel capacitors of same value will increase the net capacitance and reduce the ESL and ESR. The reduction of ESL and ESR is the most important

property .Improvements of 6dB has been observed (replacing one capacitor with multiple smaller ones).



- Choose values such that the anti-resonant will not occur at a harmonics of a generated signal(either switching or transition frequency)

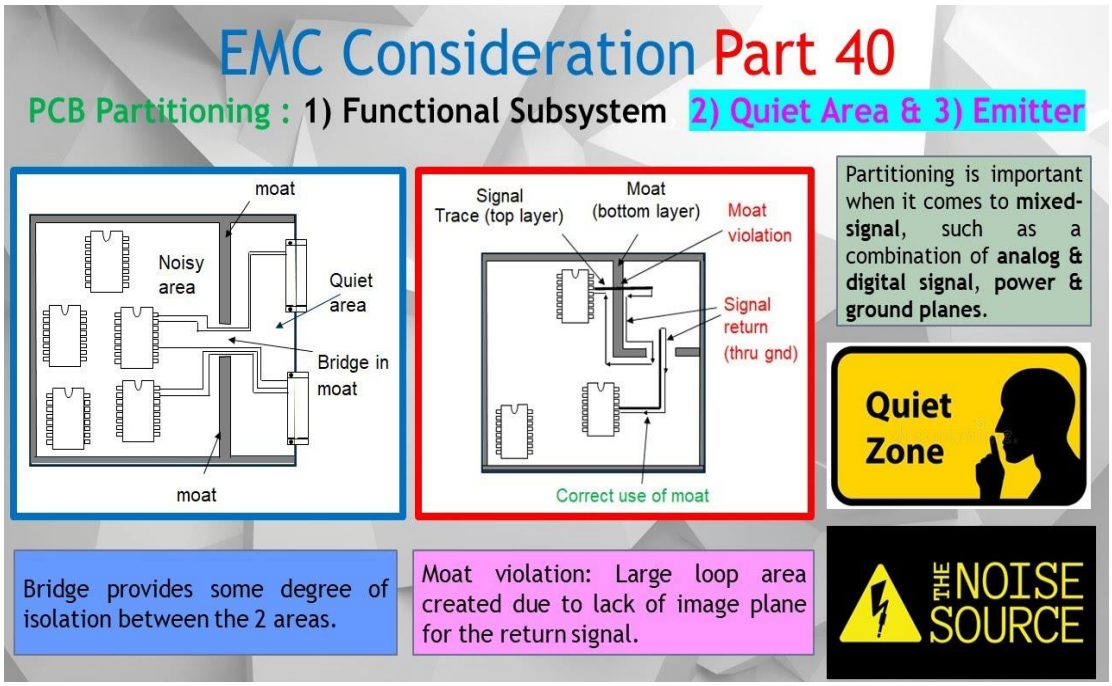
Capacitor Placement:

- Key idea is to reduce path inductance location of the components is limited by mechanical constrains.
- SMD parts can be closer than THT parts.
- Trace inductance will be 3-10X larger than plane inductance.
- Each via adds 1-3nH of Inductance.

Trace Routing:

- Keep signal traces AWAY from high frequency devices such as clocks, oscillators, etc.
- DO NOT use auto routers since they typically choose the worst possible layout for EMI/EMC concerns.
- Remember 3-W Rule, 20-H Rules.
- Use isolation (Moats) in conjunction with the portioning.

Isolation /Moating:



Intentionally/Accurately introducing breaks in power and /or ground planes.
It prevents capacitor coupling between along traces due to low frequency which means reducing the RF emissions.

Moat Violations:

Will virtually always generate loops of EMI, even if the violating trace is quiet.

Bridging Moats:

- Make the bridge wide enough for just required traces(observing 3W Rule)
- Use a ferrite to provide filtering in the power trace, but not to put once in the ground trace.
- If a violation must occur, place a bypass capacitor across the moat as close to the violation as

possible (capacitor is connected to ground to ground).

- Choose the proper filtering between the RF return currents.
- Peak Surge Voltage capability for ESD protection.

ESD Protection:

- Provide good shielding with the chassis and connectors.
- Provide good grounding connections; wire broad with 5:1 width : height aspect ratio is good (solder work nicely)
- Avoid pigtail wiring harnesses (they make good RF antennae).
- Filling unused signal plane with a ground fill help prevent ESD, not EMI.
- Guard Bands.

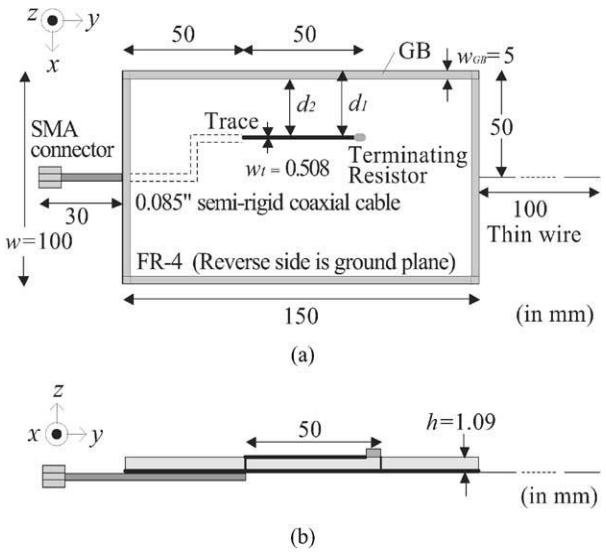
Guard Band:

Different from guard, shunt or ground traces.

Prevents ESD damage from handling of PCB

Non-Continuous traces around the edge of PCB on both Top and Bottom Layers. (Introduce some moats to prevent ground loops).

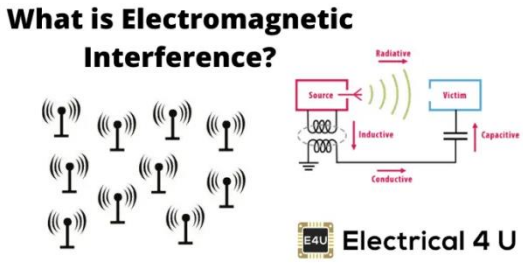
Should not be covered with the solder mask and frequently be connected to the ground reference with vias.



ELECTROMAGNETIC COMPATIBILITY TEST (EMC TEST):

EMC/EMI Testing is a critical step in design and manufacturing process of electronic device using various regulatory bodies, including the FDA, FCC and ISO will have set specific limits on the emissions that can be released from electronic device.

EMI or RFI: occurs when EM energy disrupts the operation of an electronic device.



The source can be manmade like SMPS, PC, or natural electrical storms, solar, or even cosmic noises.

EMC: ability of a device to operate an intended in an environment with other system or sources of EMI without affecting those other devices. A device is said to be an EMC compliment when it does not interface with an EM environment to extent that other device and system are negatively affected.

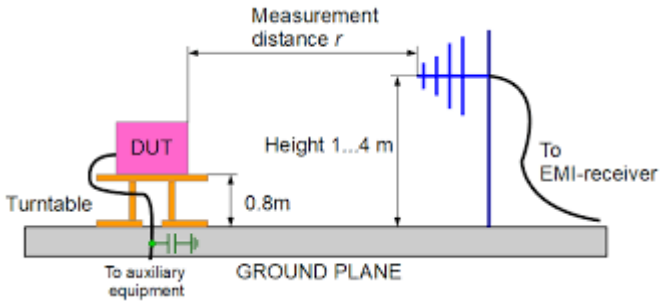
EMI and EMC Testing:

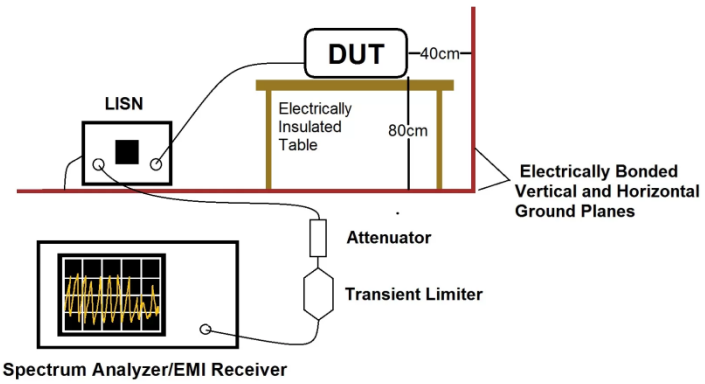
It is divided into two categories;

Immunity Testing: Process of transmitting the RF energy onto a device under test (DUT) {also known as Equipment under Test} to determine DUT operates correctly in environment.

Emission Testing: Process of measuring RF emissions both radiated and conducted of EUT or DUT. To determine if its emission levels do not exceed the limits defined by appropriate standard. It includes both radiated and conductive emission test too.

Radiated Emission: Intentional and unintentional release of EM energy from an electronic device. A radiated test is performed to ensure emission emanating from the DUT or EUT comply with applicable limits.



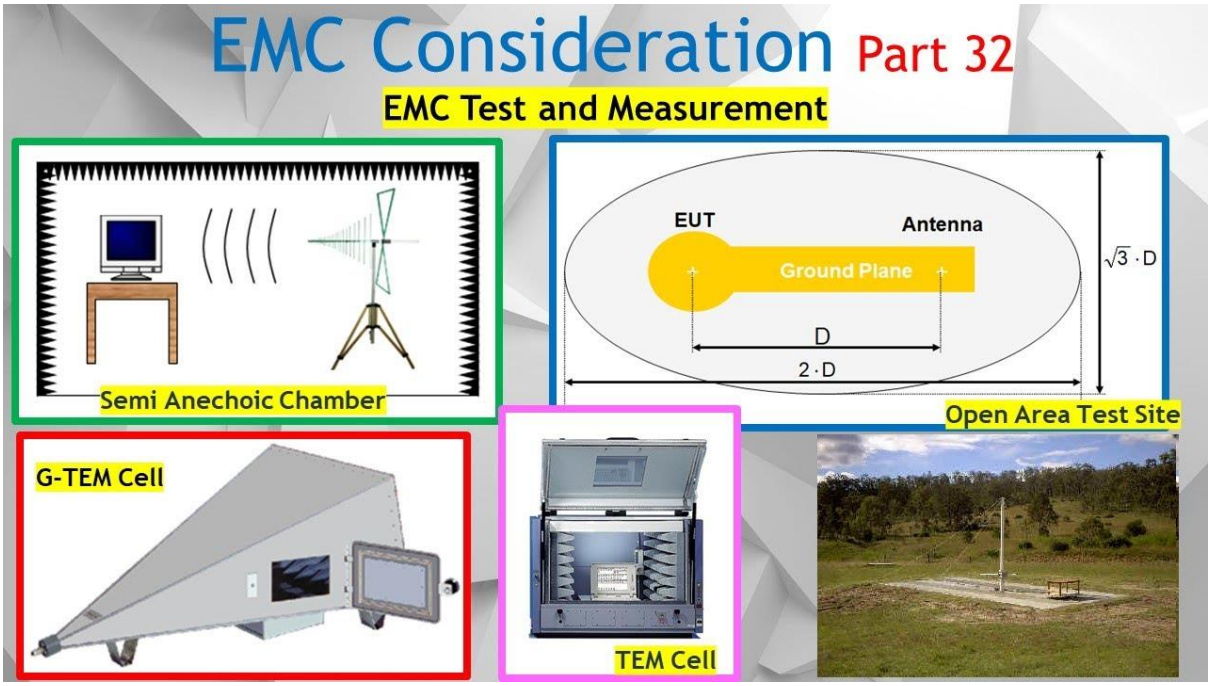


Conductive Emission: Coupling of EM energy from a device to its power chord. Like radiated emissions, the allowable conducted emissions from electronic device are controlled by different regulatory agencies and testing is preferred to ensure emission levels and below operative limits.

EMC TESTING LABS:

Open –air test site or OATS are reference sites used for most standards. They are especially used for emissions testing of large emissions/ equipment system. However, RF Testing of a physical prototype is more often called as carried out indoors in specified anechoic chambers.

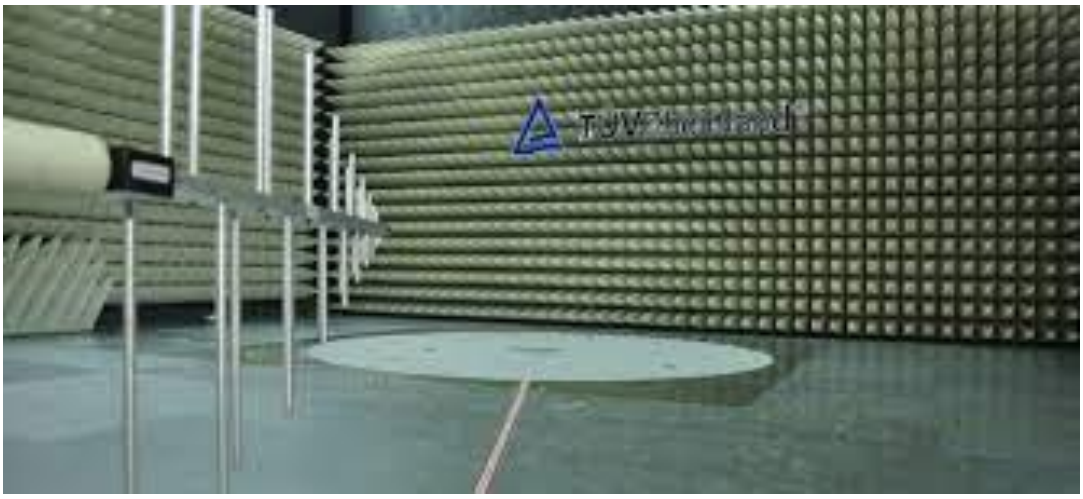
{Types of Chambers: Anechoic, Reverberation and Gigahertz transverse electromagnetic cell (GTEM)}



EMC Testing Process:

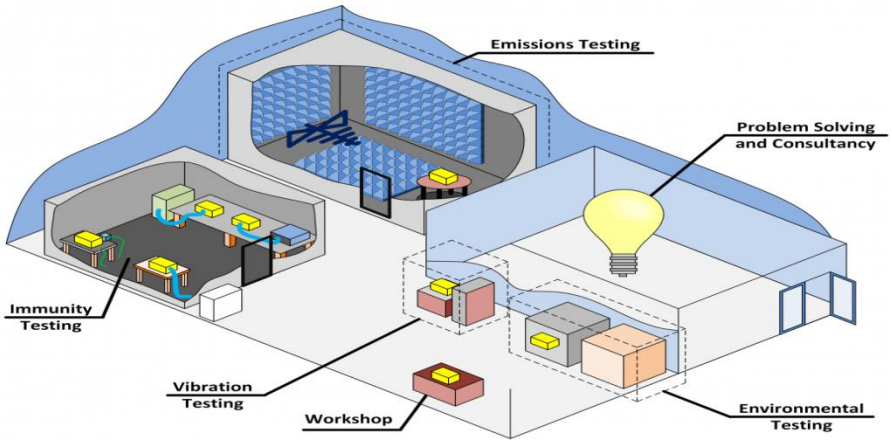
Roughly 50% of products pass their first EMC compliance Test when pre-compliance is not compared. So that is essential to understand the process and standards, a device are too tested to “n” order to increase your chances of success.

1. Know your standard: EMC Testing can be kept up to two weeks to complete, not including the time it takes to get your product into the test queue and cost up to $20,000 per submission.
2. Conduct pre-compliance EMC testing.
3. Find an EMC Testing lab.
   Once a product has gone through the Pre-Compliance testing and passed the test with a sufficient margin, it needs to be formally by an EMC Testing lab. Accredited labs are gold standard for EMC Testing and choosing an accredited lab is always for recommended through not necessary- to ensure a device ready to go to market.



How to pass EMC compatibility testing setting up a Pre-compliance testing lab:

- Spectrum Analyser with Quasi-Peak Detector.
- Pre-Amplifier(Amplifier)
- Antenna with non-metallic standard for radiated emission.
- Line Impedance Stabilization Network (LISN) for conduction testing.
- Power Limiter for conducted test.
- EMC near field probes for disposes (optional)
- Oscilloscope with frequency and time correlation capabilities to assists in debugging (optional).
- EMC Test Software.



Applications:

- ✓ Automation
- ✓ Telecommunication
- ✓ IT/AV
- ✓ Mutimedia etc.

ANTENNA TYPES:

Loop Antenna: (10 kHz to 30 MHz)

Bi-conical Antenna: (30 MHz to 300 MHz)

Long Periodic Antenna: (300 MHz to 1 GHz)

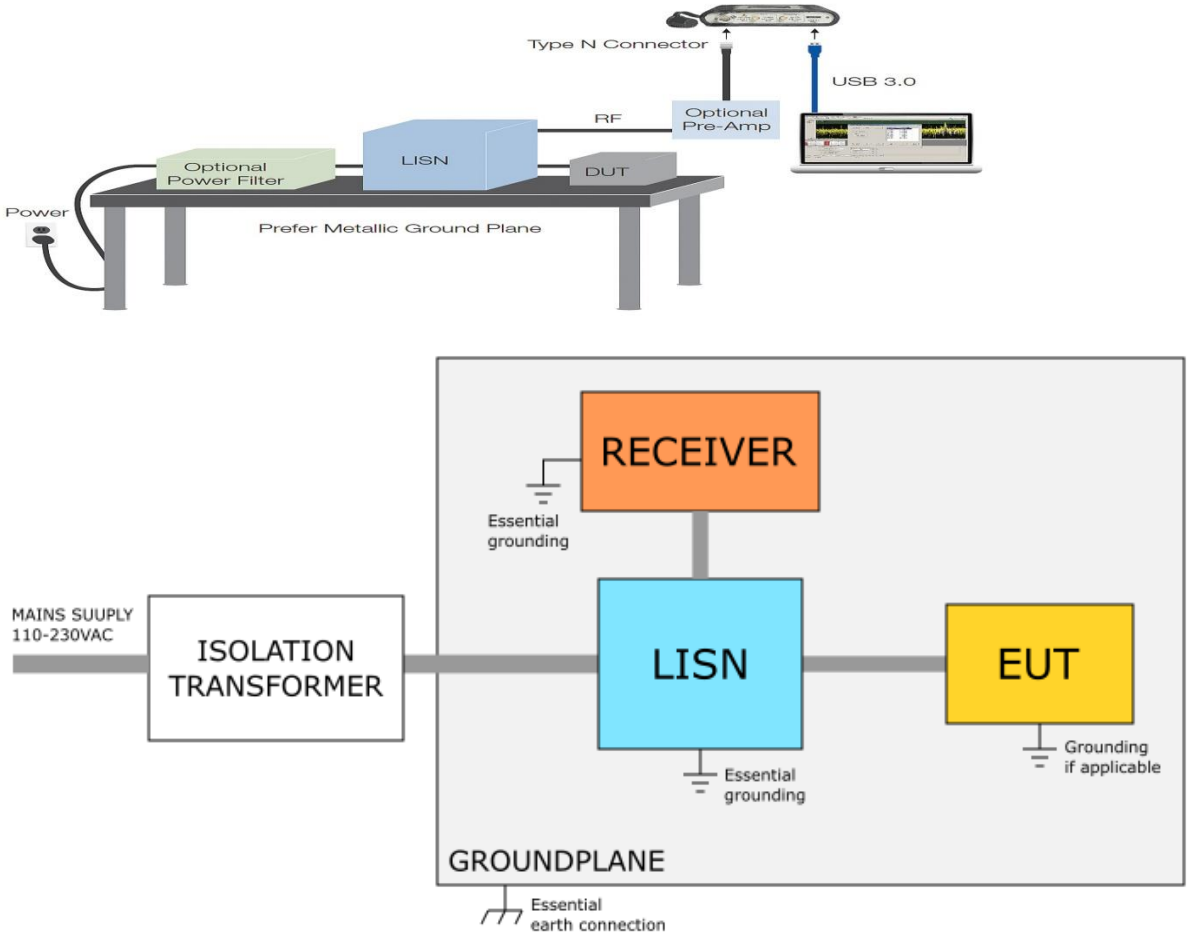
Horn Antenna: (1 GHz to 25 GHz)

CONDUCTIVE EMISSION: This interference in main supply, can affect several devices connected to same main supply. The devices generate EM or noise conducted through a power cord, interfacing with power source. This is called Conducted Emission.

Conducted Emission from frequency vary from 50 Hz to 300 MHz

Conduction emission testing is performed personally on device connected to AC Power supply.

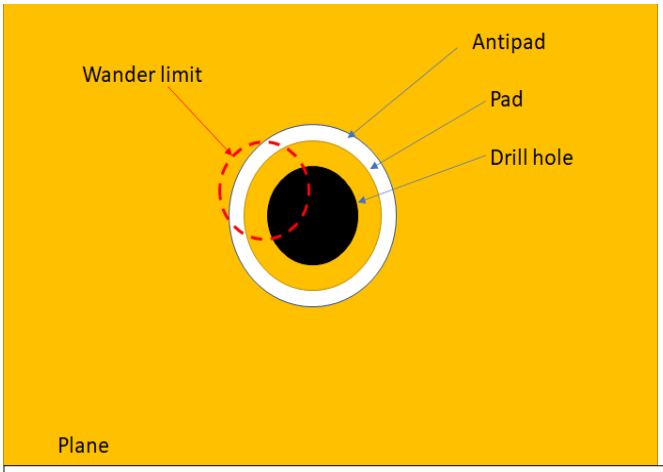
Conduction Emission Test Setup:

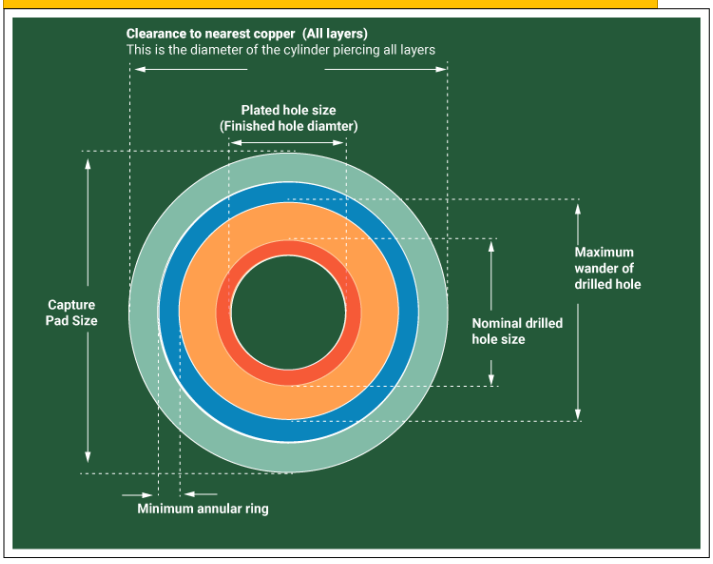


The LISN provides stabilization/standard impedance across the EUT measurement points. It couples the measurement point of EUT with the receiver. Also it prevents wanted interference signals from going to other device.

The receiver is a spectrum analyser that measures RF signal coming through LISN devices.

ANTIPAD: In PCB refers to void area around a via on internal plane layer, and which restricts other signal traces that should not be connected to the particular PTH.





A via - antipad is applied automatically by your design software based on the clearance rules. Anytime, you use a PTH to transition through a solid plane.

Inductance: A via taken in isolation is basically any inductor and the inductance of the via depends on the via aspect ratio.

Capacitance: The presence of the plane around creates some parasitic capacitance between the pads and ground.

DDR Routing: (Double-Data Rate)

Double-Data Rate or DDR memory is very common in printed circuit board design today. Many designs will use some version of this memory configuration which requires specific routing patterns in the layout. DDR gets its name from its ability to send and receive signals twice per clock cycle, which is double the rate of the original Single Data Rate (SDR) memory. Because of this doubled rate, the trace routing for DDR memory must hold tighter parameters in order to meet the performance specifications.

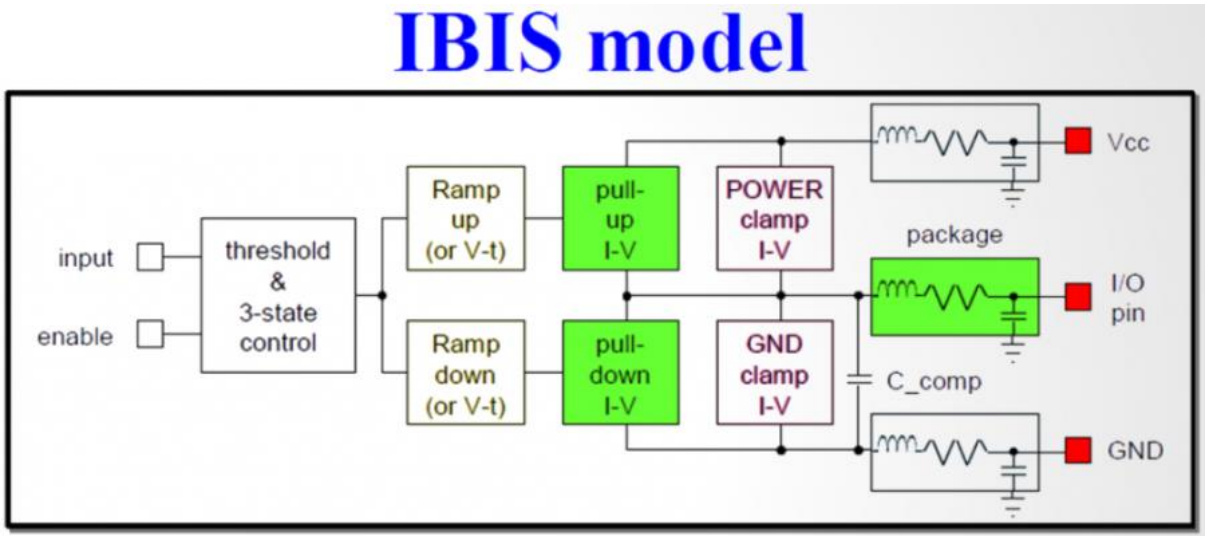
- Setting up the design with rule, constrains, footprints, and vias for DDR routing.
- Consideration for routing DDR Routing.
- How your PCB design tools can help you with DDR memory routing.
- Embedded system that uses double data rate memory (DDR) can realise increased performance over traditional single data rate (SDR) memories.

DDR Routing Types:

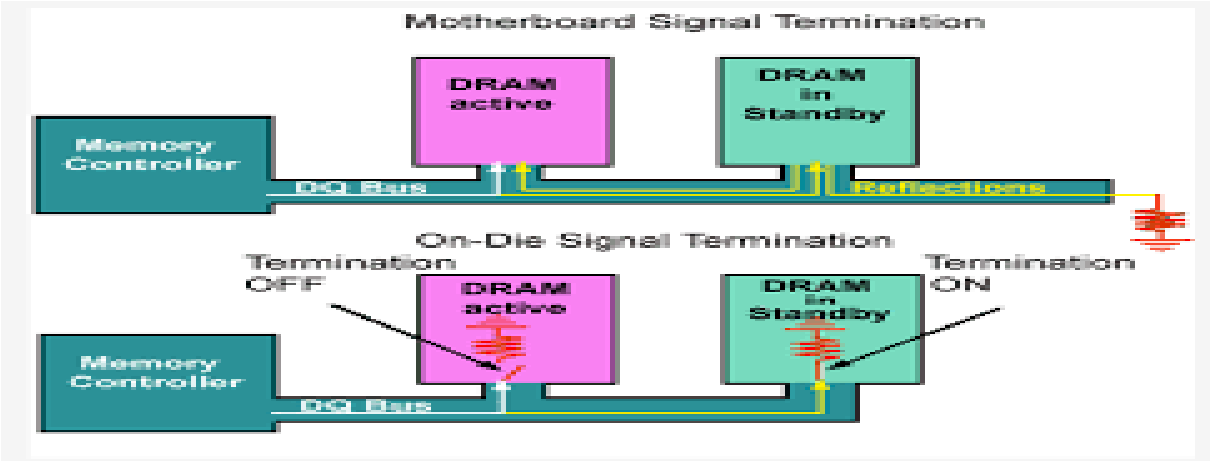
- ✓ Flyby-Topology
- ✓ T-Topology

IBIS (Input/output Buffer Inter Specification model):

Are intended to be used for the signal integrity analysis on system boards. These models allow system designers to stimulate and therefore foresee fundamental signal integrity concerns in the transmission line that connect different devices.



ODT (On-Die Termination): is the technology when termination resistor for impedance matching in transition lives is located inside a semiconductor chip instead of a PCB.



COPPER WEIGHTS:

Many designs require specific Cu Thickness to accommodate the current requirement of design.

Cu weight is defined as weight (in oz) of copper present in one square measured in oz/ft^2.

0.5 oz Cooper: (≈ 17.5 µm thick or 0.7 mils).

Available on inner layers if required as a part of a "Non-standard" constrain.

This also standard string copper weight for external layers of PCB with 1 oz finished copper weight selection.

1 oz Copper (≈ 35 µm thick or 1.4 mils):
Standard internal layer copper thickness for" Standard Construction" product of 1 oz and 2 oz finished copper weights selection. This is also the standard starting copper weight on external layers for PCB with 2 oz finished copper weight selection.

2 oz Copper (≈ 70 µm thick or 2.8 mils):
Standard internal layer copper thickness for the internal layers on 3 oz finished copper selection. This is standard starting copper thickness on external layer for PCB with 3 oz finished copper weight selection.

SURFACE FINISH:

ENIG (Electro less Nickel Immersion Gold):

Is a gold two- layer metallic surface finish that consists of a very thin layer of gold plated over a layer of Ni. Using electrodes, chemical reactions, a Nickel layer is first placed on copper pads.

An immersion method is used to apply gold on top of Nickel layer to copper the pads and traces.

Thickness Specifications:

IPC-4552.

Nickel – 2.54 to 6.35 µm (100 to 250 µin)

Immersion Gold- 0.0508 to 0.2032 µm (2 to 8 µin)

ENIG is now arguably the most used finish in the PCB industry due to growth and implementation of ROHS regulation.

BASIC UNIT CONVERSION TABLES USED IN PCB & SCHEMATICS:

1 mil – 0.0254mm

1 oz – 35 µm or 1.4 mils

0.1 inch – 2.54 mm

Note: Maximum Trace width (recommended) for all layer boards - 20 mil but for ground and power plane – 50 mils or 40 mils (approx.)

Copper Thickness for 4 or more layers (Recommended Stack-up):

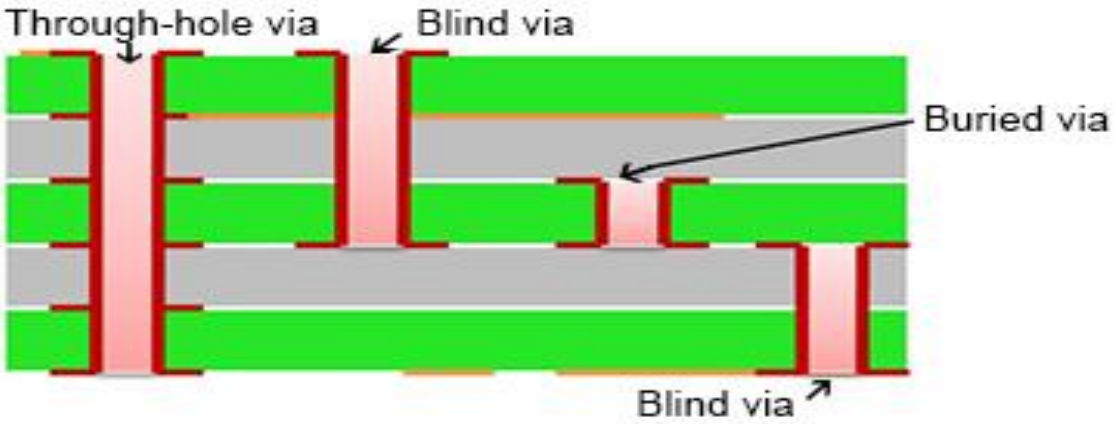
1 oz – Standard Usage

0.5 oz – EMI, SI, Twist {Cu Cladding}

Or

Thickness	Copper thick (outer/inner)	Layer No.	StackUp	Laminated chart Thickness
1.6mm±10%	1/1oz	L1		Copper 18 um--plating to 35um
				PP 0.11 mm dielectric constant 4.29
		L2		Core 1.2mm with 1/1 oz Cu
		L3		
				PP 0.11 mm dielectric constant 4.29
		L4		Copper 18 um--plating to 35um

VIA RECOMMENDATION LAYER:



LAYER1 – TOP LAYER

LAYER2 - POWER PLANE (VCC OR GND)

LAYER 3 - SIGNAL LAYER 1

LAYER 4 – SIGNAL LAYER 2

LAYER 5 – SIGNAL LAYER 3

LAYER 6 - SIGNAL LAYER 4

LAYER 7 – POWER PLANE (VCC OR GND)

LAYER 8 – BOTTOM LAYER

BEST OF LUCK