NATIONAL INSTITUTE OF TECHNOLOGY CALICUT

Department of Computer Science and Engineering

CS2091D-Logic Design Laboratory

S3:B.Tech(CSE)

Assignment-1

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Implement the following logic function using ***VerilogHDL*** with each of the three modeling techniques (**Gate-level modeling, Dataflow modeling, and Behavioral modeling**). Subsequently, Simulate and verify all the given logic functions using ***ModelSim*** integrated with ***Quartus Prime Lite Edition Software*.**

1. Inverter
2. 2-input AND gate
3. 2-input OR gate
4. 2-input NAND gate
5. 2-input NOR gate
6. 2-input XOR gate
7. 2-input XNOR gate
8. 8-input NOR gate
9. 8-input NAND gate
10. An array of 16 inverters
11. An array of 16 AND gates
12. An array of 16 OR gates
13. An array of 16 NAND gates
14. An array of 16 NOR gates
15. Boolean expression F(A, B, C) =(A’B)’+BC+A’B’
16. Implement NOT, AND, OR, XOR, XNOR using NAND and NOR gates.
17. 4bit Half adder
18. 4bit Full adder using respective Half adder

*******The End*******