NATIONAL INSTITUTE OF TECHNOLOGY CALICUT
Department of Computer Science and Engineering
CS2091D-Logic Design Laboratory
S3 B.Tech (CSE)
Assignment-III

Date of issue**: 17/10/2022** Date of submission**: 24/10/2022 23:59Hrs**

Design and Implement the following logic functions using ***Verilog with ModelSim*** integrated with ***Quartus Prime Lite Edition Software.*** Subsequently, Simulate and verify your design with an appropriate *test bench* and submit one file for each question (AIIIROLLNOQ1.***pdf,*** AIIIROLLNOQ.***pdf,*** AIIIROLLNOQ3.***pdf,*** and AIIIROLLNOQ4.***pdf***). Please note that Question 1 (Q1) and Questions 2 (Q2) must implement using all three modeling techniques (Gate level modeling, Dataflow modeling, and Behavioral modeling). However, Question 3 (Q3) and Question 4 (Q4) can implement with any of the three modeling techniques or a mix of them and encouraged to implement using hierarchical modeling wherever it is possible.

Q1.

a. 8 x 2 PROM using F1(X, Y, Z) =∑m (1,4,6,7); F2(X, Y, Z) = ∑m (0,3,4,5,7);
b. PAL(Programmable Array Logic) using F1(A,B,C,D)=∑ m(1,2,3,4,5,6,12,14,15),
   F2(A,B,C,D)=∑m(1,2,3,4,5,6,7,9,11,15), F3(A,B,C,D)=∑ m(1,3,4,5,9,10,11,13,15)
c. PLA with minimum additional logic using F1(A, B, C, D) =∑ m (0,3,4,5,6,12,14,15)
   F2(A, B, C, D) =∑m (1,3,4,5,6,7,9,11,13,15)

Q2.

a. Unclocked S-R latch.
b. Clocked S-R latch.

Q3.

a. Clocked D latch with asynchronous *preset* and *clear.*
b. Clocked D latch with synchronous *preset* and *clear.*
c. D flip-flop with asynchronous *preset* and *clear.*
d. D flip-flop with synchronous *preset* and *clear.*

Q4.

a. 8-bit register.
b. 16-bit register.
c. Register file consisting of four registers, each of which is 8-bits.
d. 4 x 2 SRAM.
e. 4 x 4 SRAM.

Instructions to submit Assignment-III:

- *Programs submitted after the due date are not validated, leading to securing **ZERO** marks in assignment III.*
- *Students should follow academic integrity at CSED, NIT Calicut to submit your work.*