NATIONAL INSTITUTE OF TECHNOLOGY CALICUT
Department of Computer Science and Engineering
CS2091D-Logic Design Laboratory
S3 B.Tech (CSE)
Assignment-IV

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Design and Implement the following logic functions using ***Verilog.*** All three questions can implement by any of the three modeling techniques or a mix of them. Subsequently, Simulate, verify, and submit (the one file (**ROLLNOQ1**.pdf, **ROLLNOQ2**.pdf, and **ROLLNOQ3**.pdf) for each question all the given logic functions using ***ModelSim*** integrated with ***Quartus Prime Lite Edition Software*** *with an appropriate full test bench***.**

Q1. Subtract two 4-bit binary numbers using a serial subtractor (or a sequential subtractor), in which bits have subtracted a pair at a time.

Q2. Multiply two 4-bit unsigned binary numbers using a combinational multiplier (without using a block multiplier, a combinational multiplier available in the FPGA and utilized when the multiplication operator * is used).

Q3. Multiply two 4-bit signed binary numbers using a combinational multiplier (without using a block multiplier, which is available in the FPGA and utilized when the multiplication operator * is used).

Instructions to submit Assignment-IV:

- *The **THREE** file names should contain Roll. No. and which modeling do the programs belong to? For instance, the file name for gate level, or data flow, or behavioral model are as follows forRol.No: **B210453CS** as **B210453CS_Gate.pdf**, or **B210453CS_Data.pdf,** or **B210453CS_Behavioral.pdf**.*
- *Programs submitted after the due date are not validated, leading to securing **ZERO** marks in **Assignment IV**.*
- *Students should follow academic integrity at a **HIGHER** level. Students should use their individual efforts to complete the assignments.*