NATIONAL INSTITUTE OF TECHNOLOGY CALICUT
Department of Computer Science and Engineering
CS2091D-Logic Design Laboratory
S3 B.Tech (CSE)
Assignment-1(b)

Date of issue**: 05/09/2022** Date of submission**: 12/09/2022 11:59 PM**

Implement the following essential combinational logic functions using ***Verilog HDL*** with the three modeling techniques (**Gate-level modeling, Dataflow modeling, and Behavioral modeling**). Subsequently, Simulate and verify all the given logic functions using ***ModelSim*** integrated with ***Quartus Prime Lite Edition Software*.**

(Note: All the inputs are taken using *repeat,* and *for looping*, statements and the student should use the previously generated files to produce the current logic functions.)

1. 4-bit Ripple carry adder
2. 8-bit Ripple carry adder
3. 4-bit Lookahead carry adder
4. BCD to Excess-3 code convertor.
5. 4-bit binary adder and subtractor.
6. 3-digit BCD cascading adder.
7. 4:1 Multiplexer
8. 16-bit Multiplexer
9. 16-bit / 4-way Multiplexer
10. 3:8 Decoder
11. 4-bit Comparator

Instructions to submit the Assignment-1(b):

- *Students should upload **SIX** independent files containing the files of Gate level, Data flow, and Behavioural modeling in .**pdf and .docx** formats (**Where .docx is a redundant copy of .pdf used at the time of evaluation purpose**).*
- *The **SIX** file names should contain Roll. No. and which modeling do the programs belong to? For instance, the file name for gate level, data flow, and behavioral model are as follows for Rol.No: **B210453CS** as **B210453CS_Gate.pdf**, **B210453CS_Data.pdf, B210453CS_Behavioral.pdf same for .docx as well**.*
- *Programs submitted after the submission date are not validated, leading to securing **ZERO** marks in assignment 1.*
- *Students should follow academic integrity at a HIGHER level. Students should use their efforts to complete the assignments.*

*******The End*******