```
module serial_subtractor(output reg [3:0]ans,output reg c,input [3:0]a,b,input clk);
reg [3:0]r1,r2;
reg a1,a2,q,s;
integer i;
initial begin
c=0;
a1=0;
a2=0;
i=0;
q=0;
s=1;
end
always@(posedge clk)begin
if(s)begin
r1=a;
r2=b;
s=0;
end
else if(i<4)begin
a1=r1[0];
a2=r2[0];
c=q;
{q,ans[i]}=a1-a2-c;
r1={1'b0,r1[3],r1[2],r1[1]};
r2={1'b0,r2[3],r2[2],r2[1]};
i=i+1;
end
end
endmodule
```

```
module tb;
reg [3:0]a,b;
reg clk;
wire c;
wire [3:0] ans;
serial_subtractor inst(ans,c,a,b,clk);
initial begin
a=$random();
b=$random();
end
initial begin
clk=1'b1;
repeat(10)
#10 clk=~clk;
end
endmodule
```