Overview of Lab Experiments

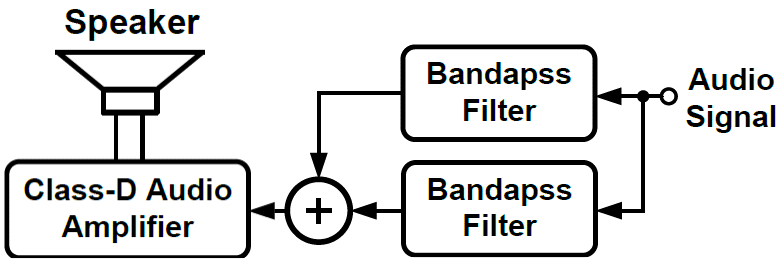

Figure A. Top-level block diagram of the lab experiment.

Objective

Design an analog system for driving a speaker.

Learning Outcome

At the end of this lab, students should be able to understand following topics with their application in real world.

- Feedback theory
- Open and closed loop system
- Opamp-RC Integrator
- Schmitt Trigger and Oscillator
- Active-RC Filters
- Summing Amplifier (Adder)
- Audio Amplifier

Brief Description

Typically, heart beat and lung sound are used as inputs and processed in electronic stethoscope module. This lab experiment aims to realize the electronic system for the stethoscope as shown in Fig. A. However, an alternate audio signal such as fixed frequency tone from audio source or functional generator are used as inputs to the experiment. We realize different blocks required for the electronic system in each experiment and finally integrate all blocks to implement the full system.

Important Instructions

- Pre-lab exercise and simulation results must be done before starting the lab experiment.
- Use LTSpice for pre-lab simulations. Information about cad tools can be found at http://www.ee.iitm.ac.in/~nagendra/cadinfo.html

LIST OF EXPERIMENTS

1. **RAMP GENERATOR**
2. **SINGLE ENDED-TO-DIFFERENTIAL INPUT CONVERTER AND PWM MODULATOR**
3. **H-BRIDGE DRIVER AND INTEGRATION**
4. **BANDPASS FILTER**
5. **ADDER**
6. **TOP LEVEL INTEGRATION**

LIST OF FIGURES

EXPERIMENT-1: RAMP GENERATOR

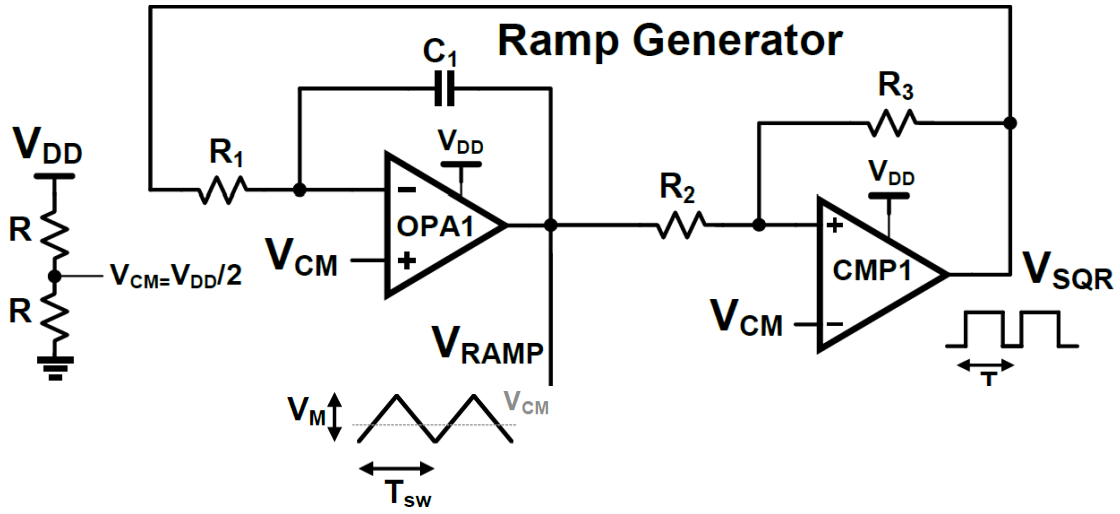

Figure 1 Schematic diagram of a ramp generator.

Ramp or triangle wave generator is actually an oscillator which is designed using opamp-RC integrator and Schmitt trigger. Figure 1 shows schematic diagram of a ramp generator.

The peak-peak amplitude of the ramp is defined by the equation:

$$V_M = 2\left(\frac{R_2}{R_3}\right)V_{CM} \quad (1)$$

The oscillation frequency of the ramp is given by equation:

$$F_{SW} = \frac{1}{T_{SW}} = \frac{R_3}{4R_2R_1C_1} \quad (2)$$

Specifications

- Supply voltage (V_{DD}) = 5V
- Frequency ($1/T_{SW}$) = 5kHz
- Peak-peak ramp amplitude (V_M) = 1V

List of Components

- OPA1: MCP6004 or equivalent alternate part
- CMP1: LM339 (open collector – requires a pullup resistor between V_{DD} and V_{OUT})

List of Measurements

1. Set V_{DD}=5V, V_{CM} = V_{DD}/2
2. Capture integrator output (V_{RAMP}) and Schmitt trigger output (square wave)
3. Measure and record frequency of V_{RAMP} and square wave V_{SQR}
4. Measure amplitude of V_{RAMP}

Pre-Lab Exercises

1. For the ramp generator circuit in Figure 1, derive the expression for ramp amplitude (Equation (1)) and frequency (Equation (2)).
2. Simulate the ramp generator circuit shown in Figure 1 and verify the expressions in Equation (1) and Equation (2). Observe the effect of variation in R_1, R_2, R_3 and C_1 on ramp amplitude and frequency.
3. Plot the waveforms and perform measurements 1-4 using simulation.

EXPERIMENT-2: SINGLE ENDED-TO-DIFFERENTIAL INPUT CONVERTER AND PWM MODULATOR

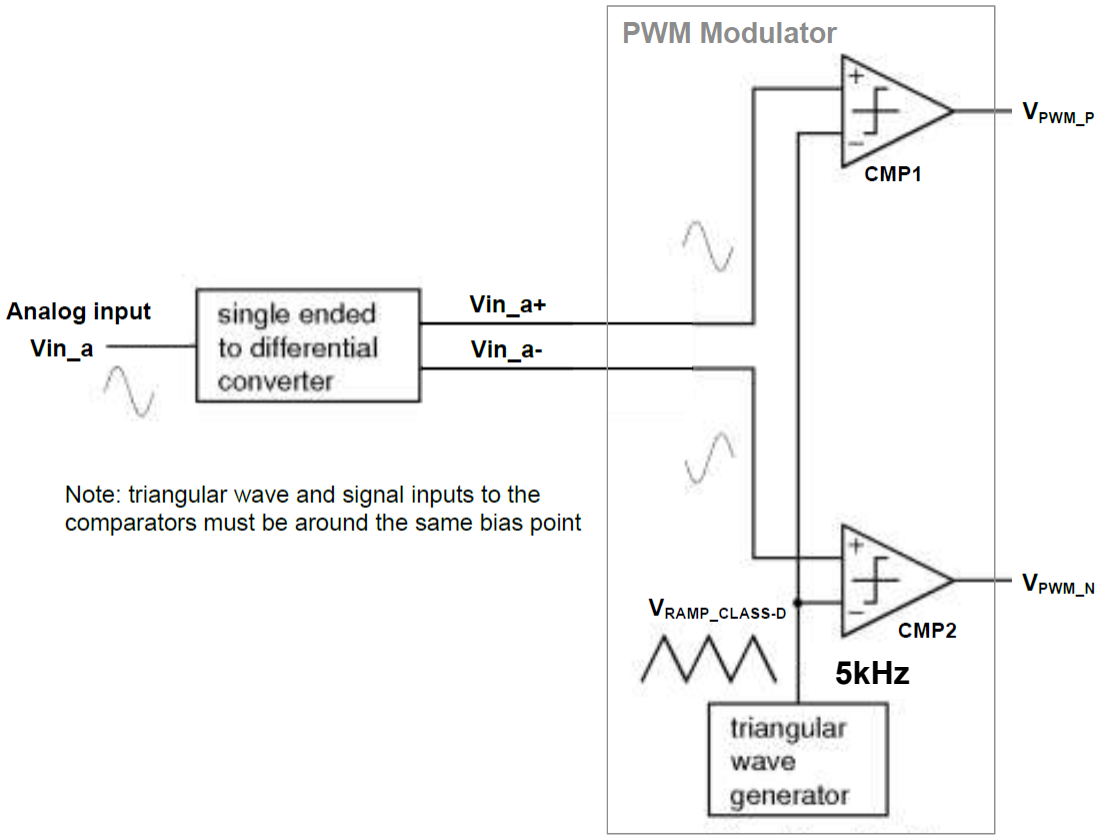

Figure 2 Schematic diagram of single-to-differential input converter and PWM modulator.

Single ended-to-differential converter can be designed using op-amp based inverting amplifier as shown in Figure 2.

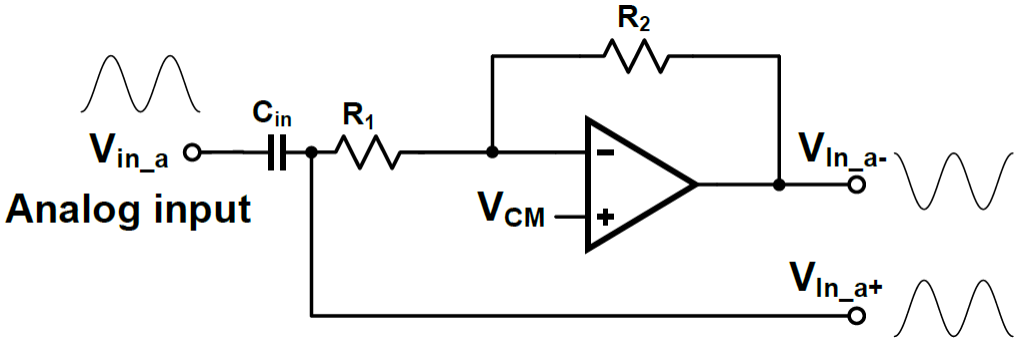

Figure 3 Schematic diagram of single-to-differential converter.

Input capacitor C_{in} should be large enough to make sure input audio signal is not attenuated.
For R_1=R_2:

$$V_{in\_a^+} = V_{in\_a(ac)} + V_{CM}$$
$$V_{in\_a-} = -V_{in\_a(ac)} + V_{CM}$$

Since outputs (V_{in_a+} and V_{in_a-}) and V_{RAMP} are biased around V_{CM}, common mode shifting of V_{RAMP} is not needed. Therefore $V_{RAMP\_CLASS-D}$ can be directly connected to V_{RAMP}. In case common mode of V_{RAMP} is not V_{CM} then it must be shifted to V_{CM} by using a coupling capacitor and resistor (Figure 3) to generate V_{RAMP_B}.

Specifications

• Supply voltage (V_{IN}=V_{DD}) = 5V
• PWM Frequency = 5KHz

List of Components

• CMP1 and CMP2: LM339 (open collector – requires a pullup resistor between V_{DD} and V_{OUT})
• INV1, INV2 and INV3: MC14069

List of Measurements

1. Set V_{DD}=V_{IN}=5V
2. From function generator, set sinusoid wave of 312.5Hz and use as input to single ended-to differential converter. Peak-to-peak amplitude of the sinusoid should be same as peak-to-peak amplitude of the triangular wave.
3. Measure amplitude and frequency of waveforms at input, V_{in+} and V_{in-}. Capture oscilloscope waveform and verify that V_{in+} and V_{in-} are 180 degrees out of phase and have same amplitude as input.
4. Measure and capture duty cycle at V_{PWM_P} and V_{PWM_N}. Duty cycle should follow the same pattern as V_{in_a+} and V_{in_a-}. Verify that V_{PWM_N} has inverter duty cycle (1-D) of V_{PWM_P} (D).
5. Add an RC filter at V_{PWM_P} and V_{PWM_N} with 3dB cut-off frequency of 1-2KHz and observe the output. Verify that output has the same shape as V_{in_a+} and V_{in_a-}.

Pre-Lab Exercise

1. Derive the expression for V_{in+} and V_{in-} in terms of input and prove that V_{in+} and V_{in-} have same amplitude but of opposite polarity.
2. Find the expression for differential PWM signal, V_{PWM_P}-V_{PWM_N} and prove that average output is amplified version of analog input to single ended to differential converter. Find the gain of amplifier.
3. Build the complete circuit shown in Figure 3. Verify the functionality in simulation with measurements 1-5.

EXPERIMENT-3: H-BRIDGE DRIVER AND INTEGRATION

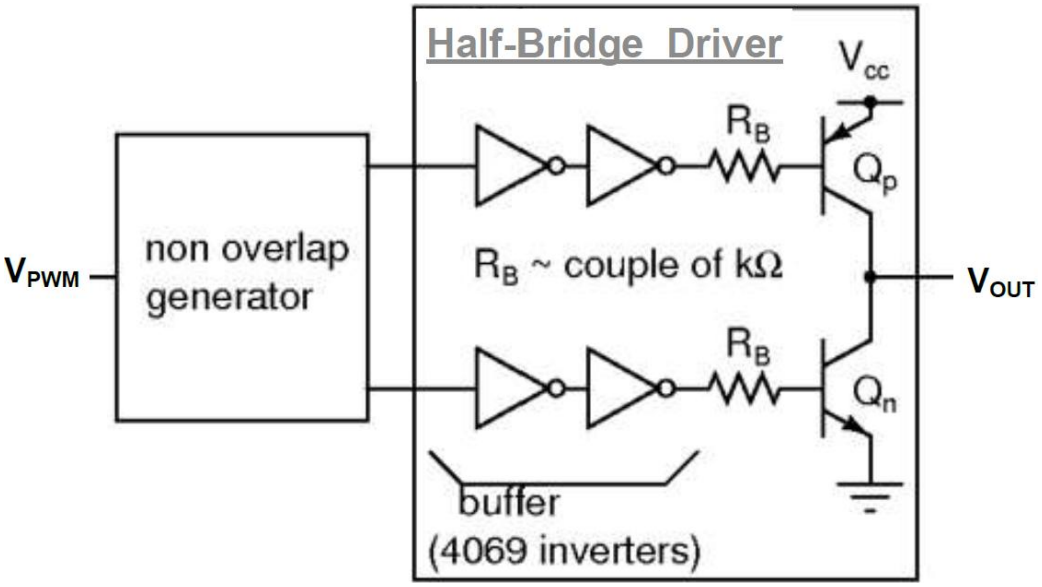

Figure 4 Schematic diagram of a half-bridge driver.

Figure 4 shows the circuit diagram of half-bridge driver. The driver is the output stage of class-D amplifier and is the key to obtaining good efficiency. The switches (Qp and Qn) of the half-bridge driver are implemented using NPN and PNP transistors and driven with CMOS inverter buffers. Use a base resistance (bases of Qp and Qn) of a few kΩ to limit the base current. If you find that the drive is insufficient (i.e. the transistors don't saturate with a heavy load), reduce the base resistances so that they saturate. If you find that the drive is still not sufficient, you can omit the base resistor, and connect two inverters in parallel to drive the base of the transistors. The non-overlap generator can be designed using the circuit shown in Figure 5.

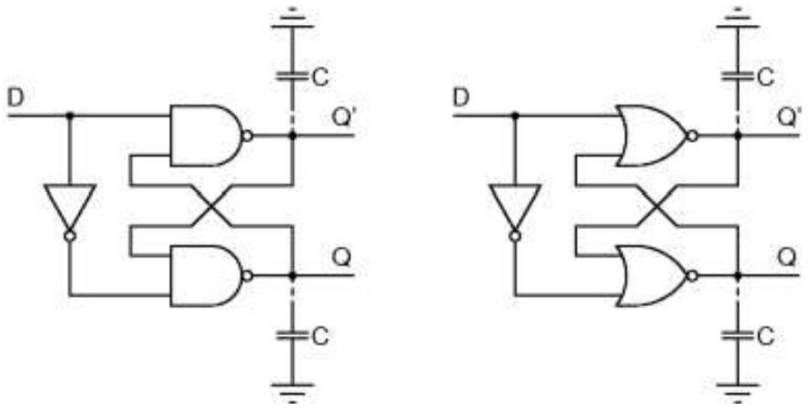

Figure 5 Schematic diagram of a non-overlapping clock generator.

In order to test the half-bridge circuit, V_{PWM} from one of the PWM modulators (V_{PWM_P} or V_{PWM_N}) of experiment-4 can be used as input. V_{OUT} can be initially tested without load and then 32Ω

resistive load is applied. For simulation, actual electrical model of speaker can be used as shown in Figure 6. L is the coil inductance which is usually within the range of few 100s to a 1000 µH depending upon the size of coil. R_L is coil resistance which depends upon power rating of the speaker.

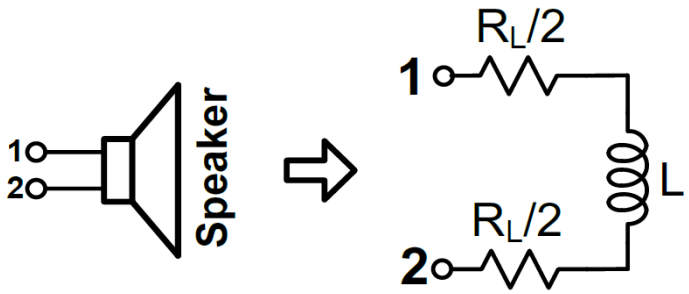

Figure 6 Electrical model of a speaker.

Figure 7 shows the circuit diagram of complete class-D amplifier. The PWM output from single ended to differential converter and PWM modulator designed in experiment-2 is fed to H-Bridge driver which drives the speaker load. H-bridge driver consist of two identical half-bridge drivers. The complete class-D amplifier should be tested with resistive load first and then actual speaker.

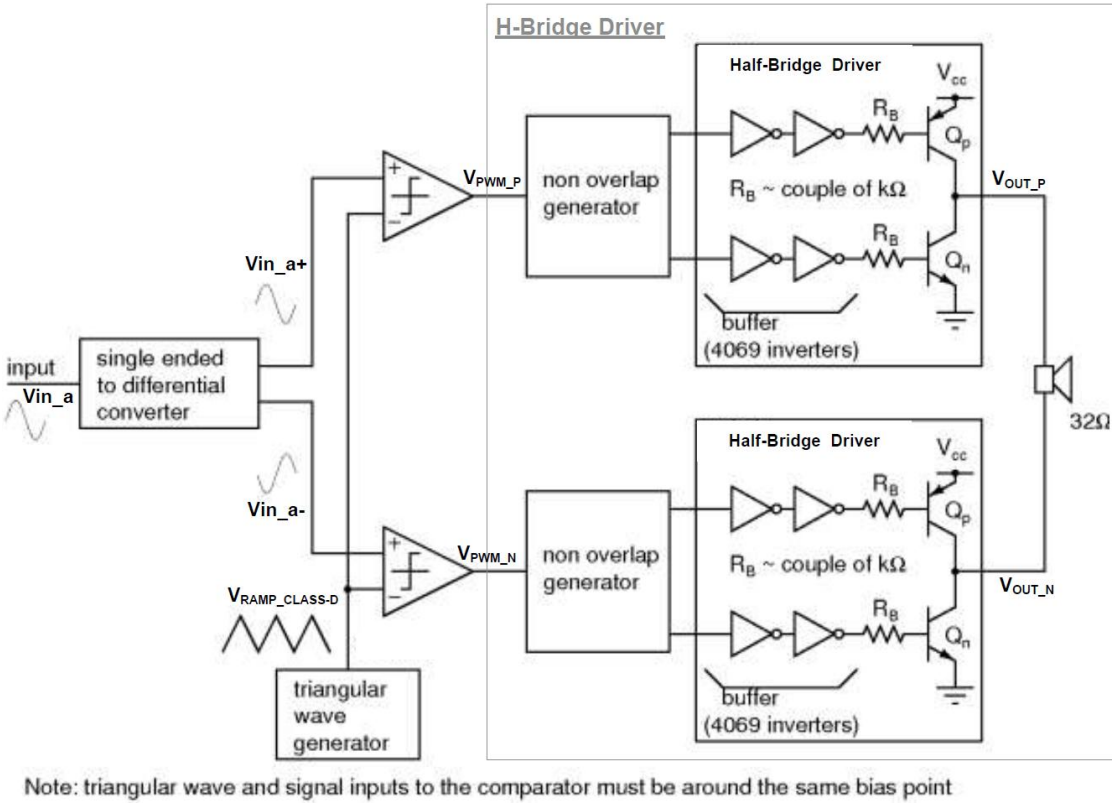

Figure 7 Circuit diagram of a complete class-D amplifier.

Specifications

• Supply voltage (V_{IN}=V_{DD}) = 5V

• PWM Frequency = 5KHz
• Load Resistance (R_L) = 32Ω

List of Components

• CMP1 and CMP2: LM339 (open collector – requires a pullup resistor between VDD and VOUT)
• Inverters: MC14069 or CD4069
• NAND Gates: SN74AHC00N
• BJTs: 2NXXXX series or alternate parts

List of Measurements

1. Set V_{DD}=V_{IN}=5V, RL=32 Ω
2. From function generator, set sinusoid wave of 312.5Hz and use as input to single ended-to differential converter. Peak-to-peak amplitude of the sinusoid should be same as peak-to-peak amplitude of the triangular wave.
3. Measure and capture duty cycle at V_{OUT_P} and V_{OUT_N}. Duty cycle should follow the same pattern as V_{in_a+} and V_{in_a-}. Verify that V_{OUT_N} has inverter duty cycle (1-D) of V_{OUT_P} (D).
4. Add an RC filter at V_{OUT_N} and V_{OUT_P} with 3dB cut-off frequency of 1-2KHz and observe the output. Verify that output has the same shape as V_{in_a+} and V_{in_a-}. RC filter is only to observe the average value of output hence should not be in the load path (i.e. load should be connected directly between V_{OUT_P} and V_{OUT_N}).
5. Verify 2-4 with speaker and do hearing test. Reduce the amplitude of input sinusoid and observe the change in sound level. Repeat hearing test for 5 different frequency tones between 156.25Hz to 1.25KHz and observe the sound.

NOTE: capture oscilloscope waveform only for one condition to show the functionality of circuit.

Pre-Lab Exercise

1. Build the complete circuit shown in Figure 7 in LTSpice. Verify the functionality by simulation with measurements 1-5. Use speaker model from Figure 6 as load and plot current through inductor. Inductor current should be average of differential output voltage (V_{OUT_P}-V_{OUT_N}) divided by R_L.

EXPERIMENT-4: BANDPASS FILTER

The objective of experiment-4 is to design two different bandpass filters in Figure 8. Audio input (V_{in_audio}), which is a fixed frequency sinusoid tone, is used as input to the bandpass filter. Each bandpass filter is designed to respond to a desired frequency tone and reject other frequencies.

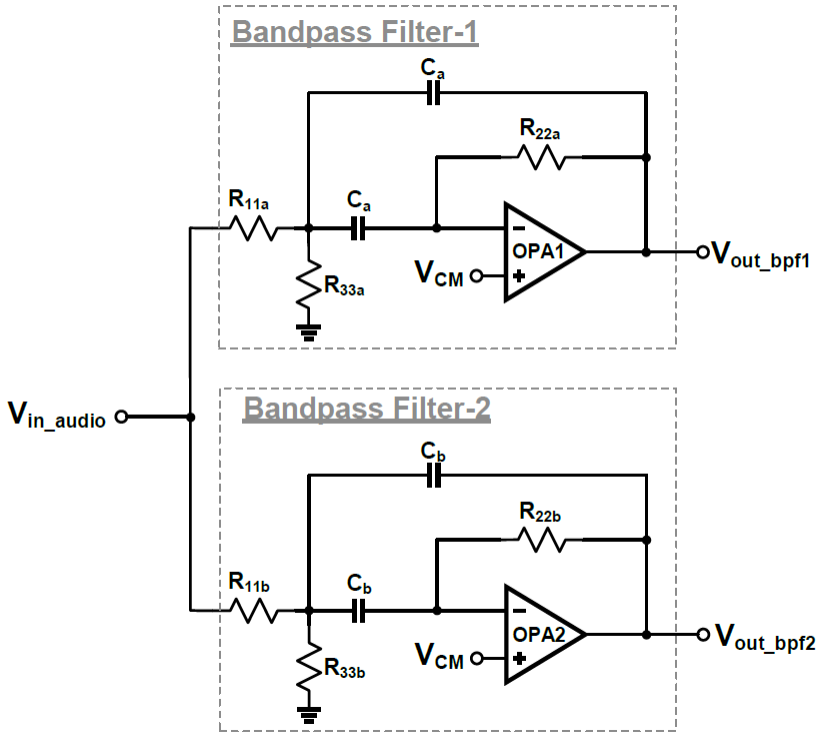

Figure 8 Schematic diagram of a bandpass filter.

Specifications

- Supply voltage: V_{DD}=5V
- V_{CM}=V_{DD}/2=2.5V
- Bandpass filter Gain (A_{o1}=A_{o2})=1 (0 dB)
- Bandpass filter Q-factor (Q_{o1}=Q_{o2}) = 10
- Bandpass Filter-1 center frequency (f_{o1}) = 156.25Hz, Bandpass Filter-2 center frequency (f_{o2}) = 625Hz

List of Components

- OPA1 and OPA2: MCP6004 (Op Amps Quad 1.8V 1MHz)

List of Measurements

1. Set V_{DD}=5V, V_{CM}=2.5V
2. Tune Bandpass Filter-1 center frequency (f_{o1}) = 156.25Hz, Bandpass Filter-2 center frequency (f_{o2}) = 625Hz, gain (A_{o1}=A_{o2})=1 and Q_{o1}=Q_{o2}=10.

3. From function generator, set sinusoid wave of 156.25Hz and use as input to bandapss filters (V_{in_audio}). Peak-to-peak amplitude of the sinusoid should be 0.9 times of peak-to-peak amplitude of the ramp signal of experiment-1.
4. Measure and capture the output of bandpass filters (V_{out_bpf1} and V_{out_bpf2}) and verify the amplitude as per the filter response. Reduce the amplitude of V_{in_audio} and verify that V_{out_bpf1} follow the change in amplitude. Set the amplitude back to its maximum value (0.9xVm)
5. Change the frequency of V_{in_audio} to 625Hz and repeat 4.
6. Now sweep the frequency of V_{in_audio} from 100Hz to 1.25kHz and verify that V_{out_bpf1} and V_{out_bpf2} do not respond to any other frequencies except their respective center frequencies (f_{o1}=156.25Hz and f_{o2}=625Hz)

Pre-Lab Exercise

1. Derive the transfer function of bandpass filter shown in Figure 8 and prove that it is a second order bandpass filter having transfer function equivalent to:

$$H(s) = \frac{A_0 \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}$$

2. Find the values of resistors and capacitors for BPF-1 and BPF-2 based on values (A_o, f_o and Q_o) provided in the Specifications.
3. Simulate and perform measurement 3-6. Capture all the plots and mark values.

NOTE:

• Center frequencies (f_{o1} and f_{o2}) may be slightly off from simulation results when implemented on breadboard. This is mainly due to the tolerance in resistors and capacitors. In that case, you can tune the frequency of V_{in_audio} to match the center frequency of the bandpass filter. Exact center frequency of BPF-1 (f_{o1}) can be found by sweeping the frequency of V_{in_audio} around 156.25Hz and look for the maximum amplitude of V_{out_bpf1}. Similarly, Exact center frequency of BPF-2 (f_{o2}) can be found by sweeping the frequency of V_{in_audio} around 625Hz and look for the maximum amplitude of V_{out_bpf2}.

EXPERIMENT-5: ADDER

The objective of experiment-5 is to add the band pass filtered signals (V_{out_bpf1} and V_{out_bpf2}) from experiment-4. The schematic diagram of an adder is given below.

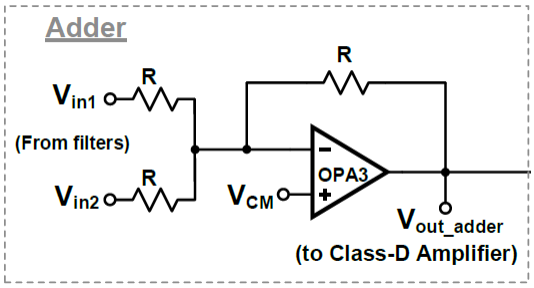

Figure 9 Schematic diagram of an adder.

Specifications

• Maximum peak to peak amplitude of V_{in1} and V_{in2} = 0.9xVm (Vm is the peak-to-peak amplitude of the ramp signal obtained from experiment-1 at VDD=5V)

List of Components

• OPA3: MCP6004 (Op Amps Quad 1.8V 1MHz)

List of Measurements

1. Set V_{DD}=5V, V_{CM}=2.5V
2. From function generator, apply sinusoid wave of amplitude=0.9xVm, frequency=156.25Hz at V_{in1} and V_{in2} with common mode (dc offset) set at 2.5V.
3. Measure and capture the output of adder (V_{out_adder}) and verify that: $V_{out\_adder} = (V_{in1} + V_{in2})$
4. Reduce the amplitude of Vin1 and Vin2 and verify that V_{out_adder} follows the change in amplitude.
5. Now connect V_{in1} to the output of Bandpass Filter-1 (V_{out_bpf1}) and V_{in2} to Bandpass Filter-2 output (V_{out_bpf2}). From function generator, apply sinusoid wave of 156.25Hz as input to bandapss filters (V_{in_audio}). Peak-to-peak amplitude of the sinusoid should be 0.9 times of peak-to-peak amplitude of the ramp signal of experiment-1.
6. Change the frequency of input sinusoid to 625Hz and repeat 5.
7. Now sweep the frequency of V_{in_audio} from 100Hz to 1kHz and verify that V_{out_adder} amplitude is 0.9xVm.

Pre-Lab Exercise

1. Calculate the values of R for the frequency provided in the Specifications.
2. Design and simulate the entire circuit shown in Figure 9 with above calculated values. Verify the operation with measurements 1 to 7.

EXPERIMENT 6: TOP LEVEL INTEGRATION

Top level integration combines all the four modules (Class-D Amplifier, Filters and Adder designed during experiments 1-5) to build the complete system. Figure 10 shows the block diagram of the complete system after integrating all the modules.

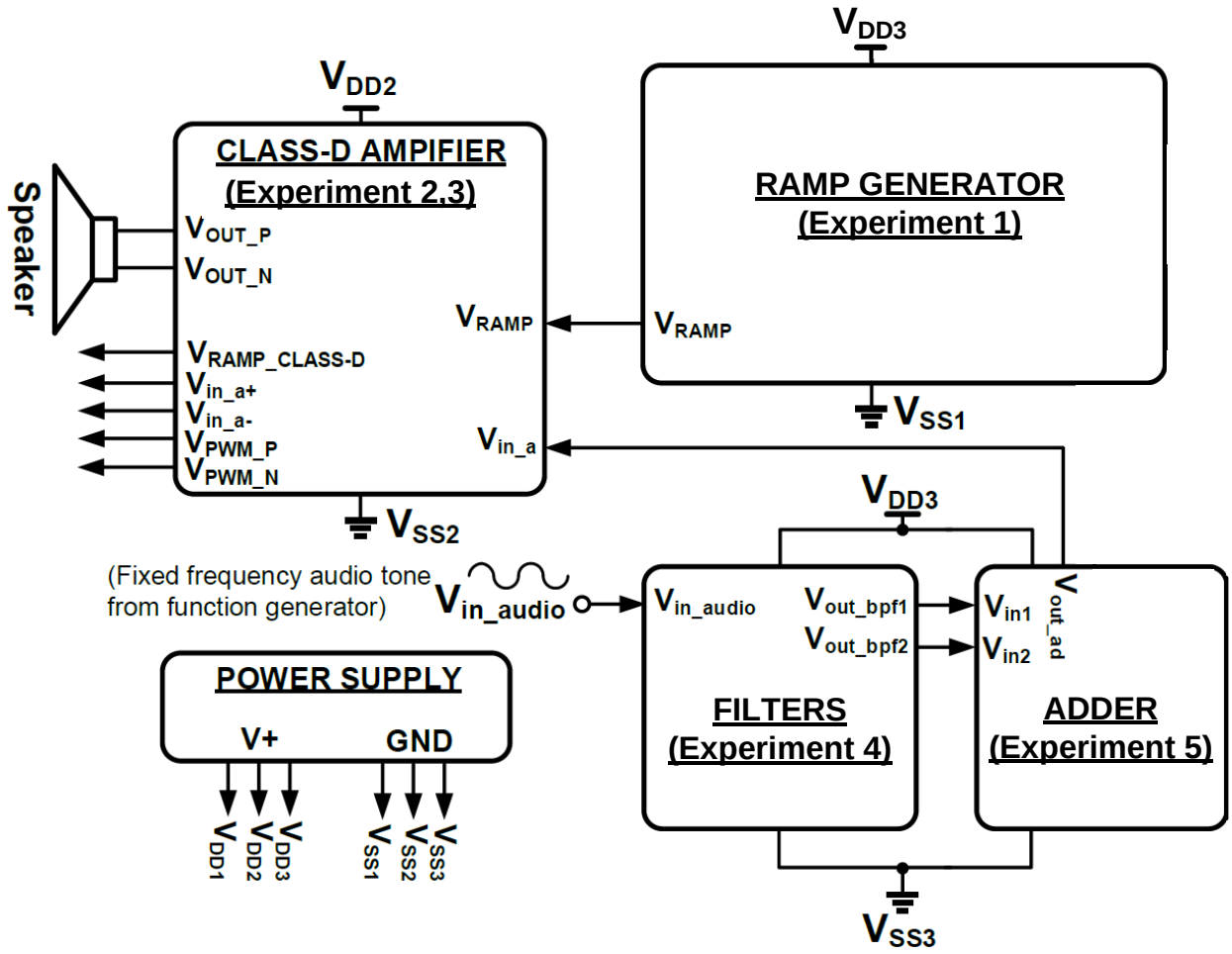

Figure 10 Block diagram of top-level integration.

V_{in_audio} is a fixed frequency audio tone generated from function generated as it was used in experiment-4 and 5. All the interface signals going from one module to other should be connected properly. In order to prevent noise coupling from one module to other, V_{DD} and GND (V_{SS}) of each module should be connected directly to power supply and not shorted locally on the breadboard. If required, decoupling capacitors of few µF can be connected locally between V_{DD} and GND of each module. If analog modules (non-switching) within the modules are affected from switching noise then V_{DD} and GND of each analog module can be separated as well and connected directly to the power supply.

Integration Guidelines

1. Makes sure all the individual modules are working before integrating them together.
2. Before starting board level integration, integrate all the modules together on LTSpice and verify the functionality.
3. Label all the signals shown in the block diagram of Figure 10 using a small piece of paper and tape. Wires connecting to these labelled signals should be brought to for measurement. Rest of the signals can be left inside the board.
4. Try to use different color wires for VDD, GND and signals. For example, red can be used for VDD, black from GND and other colors for signals.
5. Putting tape around the circuits may help in keeping the connections intact. Signal wires which are brought out for measurement can also be fastened locally on board using tape to protect from popping out of the holes.
6. VDD and GND (VSS) of each module should be connected directly to power supply and not shorted locally on the breadboard. If required, decoupling capacitors of few μF can be connected locally between VDD and GND of each module.
7. Check the short between VDD, GND and signals before turning the power supply ON.
8. Limit the power supply current to prevent the circuit from damaging in case of accidental short. Usually, current limit is set slightly higher (1.5x or so) than the maximum total current drawn by the circuits.

Final Demo

Final demo will be based on both LTSpice and board level design. Students will be asked to demonstrate following:

1. LTSpice simulation results. Must be implemented individually by each person.
2. Hardware functionality demo.
3. Probe signals listed in Figure 10.