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**Evaluation of Variability using Schmitt
Trigger on Full Adders Layout**

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ABSTRACT

The aggressive technology and voltage scaling which CMOS-based modern digital circuits are facing introduce challenges as short-channel effects, higher radiation and variability impact. As CMOS technology approaches its scaling limit, novel technology nodes, as FinFET, emerged to address such challenges. Although, even when short-channel and radiation effects are mitigated due to technology intrinsic characteristics, the variability impact escalates with technology scaling and the lack of manufacturing precision. To mitigate that, novel techniques are proposed and tested in the literature. This work analyzes the impact on variability robustness using a technique based on the replacement of full adders internal inverters by Schmitt Triggers. Some works point that the given technique helps to improve the variability robustness at the electrical level. Therefore, analysis has been performed at layout level using the 7nm FinFET technology node from ASAP7 library and the technique was applied on four full adder designs. Performance, energy and area are taken into account. Results show up to 65% improvement on average delay and energy variability robustness, being necessary a trade-off analysis between robustness improvements and the impact on delays, power consumption and area.

Keywords: Nanotechnology. FinFET devices. Process Variability. ASAP7 PDK. Schmitt Trigger. Full Adder.

Análise da Variabilidade utilizando Schmitt Triggers em Leiautes de Somadores Completos

RESUMO

A miniaturização da tecnologia e diminuição das tensões de alimentação ao qual os circuitos digitais baseados na tecnologia CMOS estão enfrentando introduzem desafios como os efeitos de canal-curto e o maior impacto da radiação e da variabilidade. Como a tecnologia CMOS se aproxima de seus limites, novos nodos tecnológicos, como o FinFET, emergem para enfrentar esses desafios. Contudo, mesmo quando efeitos de canal-curto e efeitos de radiação são mitigados devido à características intrínsecas do nodo, o impacto da variabilidade escala com a miniaturização da tecnologia e a falta de precisão de fabricação. Para mitigar esta variabilidade, novas técnicas são propostas e testadas na literatura. Este trabalho analiza o impacto na robustez à variabilidade de uma técnica baseada na substituição dos inversores internos de somadores completos por Schmitt Triggers. Alguns trabalhos apontam que esta técnica ajuda a melhorar a robustez à variabilidade no nível elétrico. Portanto, a análise foi efetuada em nível de leiaute utilizando o nodo tecnológico de 7nm FinFET da biblioteca ASAP7 e a técnica foi aplicada em quatro somadores completos diferentes. Desempenho, consumo de energia e área foram levados em conta. Resultados mostram melhorias de até 65% na robustez à variabilidade no atraso de propagação médio e energia. Contudo, é necessário realizar uma análise de custo-benefício entre as melhorias e o seu impacto nos atrasos de propagação, energia e área.

Palavras-chave: Nanotecnologia, Dispositivos FinFET, Variabilidade de Processo, ASAP7 PDK, Schmitt Trigger, Somador Completo.

LIST OF ABBREVIATIONS AND ACRONYMS

BTI	Bias Temperature Instability
CMOS	Complementary-Metal-Oxide-Semiconductor
CNFET	Carbon Nanotube Field Effect Transistor
CPL	Complementary Pass-transistor Logic
ECC	Error Correcting Code
EDA	Electronic Design Automation
EDP	Energy-Delay-Product
FA	Full Adder
FDSOI	Fully Depleted Silicon On Insulator
FinFET	Fin Field Effect Transistor
GOBD	Gate Oxide BreakDown
HCI	Hot Carrier Injection
HFIN	Fin Height
IOFF	Off-Current
ION	On-Current
LG	Gate Length
M2	Metal 2
MC	Monte Carlo
NBTI	Negative Bias Temperature Instability
NMOS	N-channel Metal-Oxide-Semiconductor
NT	Near-Threshold
OTS	Optimized Transistor Sizing
PBTI	Positive Bias Temperature Instability
PDK	Process Design Kit

PDP	Power-Delay-Product
PMOS	P-channel Metal-Oxide-Semiconductor
PTM	Predictive Technology Model
PVT	Process, Voltage and Temperature
RDP	Random Dopant Fluctuation
SCE	Short-Channel Effect
SOI	Silicon On Insulator
SRAM	Static Random-Access Memory
ST	Schmitt Trigger
TFA	Transmission Function Adder
TGA	Transmission Gate Adder
TOX	Oxide Thickness
TSI	Fin Thickness
VTH	Threshold Voltage
WF	Work Function
WFF	Work Function Fluctuation

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1 INTRODUCTION

The technology scaling over the years have significantly increased the density of transistors present on chips. Alongside, with the advance over transistor technology, new challenges were introduced due to the scale down, as aging effects, high power consumption due to leakage current and an increase in the sensibility to transient faults due to radiation and process variability (ABBAS et al., 2015).

The same technology scaling that allowed the increase in transistor density also allowed a voltage scaling due to the shortening of gate dimensions, internal capacitances and resistances. These two combined events contributed to the emergence, growth and current dominance of mobile applications over its counterpart. This new context introduced a concern for battery lifespan which these applications are dependent (ISLAM et al., 2010).

The ascending number of mobile applications that depends on highly sophisticated processing schemes with a limited power-supply capability of today's batteries brings conflicting needs. The need to explore high-performance designs and implementations to meet the speed constraints for real-time applications and, simultaneously, consider low-power design approaches to extend the battery life of portable devices (SHOARINEJAD; UNG; BADAWY, 2003).

Due to the new power consumption concern, novel types of logic blocks for chips started being designed for low power. One of the most present logic blocks in computer systems is the Full Adder (FA). It plays a central role in performing general arithmetic operations such as addition, subtraction, division, shift and so on. The full adder operation adds two bits considering the Carry Out value from a less significant stage. It follows the equations 1.1 and 1.2 with the Truth Table 1.1.

$$\text{Sum} = (A \oplus B) \oplus Cin \quad (1.1)$$

$$\text{Cout} = (A \wedge B) \vee Cin \wedge (A \oplus B) \quad (1.2)$$

Table 1.1: Truth Table of Full Adders

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Adder cells define the throughput and are employed in the processor's executive, floating-point, and memory address generation units. Due to its absolute numbers in microprocessors and their part on the critical path of electronic systems, any improvements over adding blocks generates a considerable improvement in the whole system because of the huge influence of power, timing and area characteristics on the system design (SHOARINEJAD; UNG; BADAWY, 2003).

Moore's law predicts that the number of transistors per square on integrated circuits will double every year and it has been guiding the industry trending for decades. However, continue with scaling in the bulk Complementary metal-oxide-semiconductor (CMOS) technology has been no straightforward task. At deep nanotechnology nodes, each chip may show different behavior due to process variations during the manufacturing steps. Variations that influence the circuits metrics such as performance and power consumption, hastening the circuit degradation and making it deviate from its correct operation (ABBAS et al., 2015) (NASSIF, 2008).

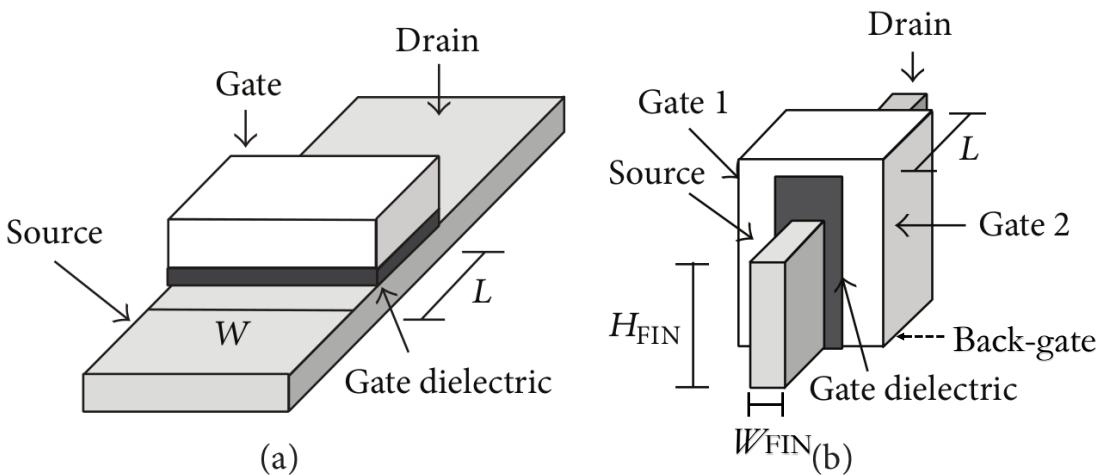
Few works present techniques at circuit level for variability mitigation. Among these works, there is (DOKANIA; ISLAM, 2015) and (TOLEDO; ZIMPECK; MEINHARDT, 2016) which introduce and investigate, respectively, the impact of a novel technique for variability robustness improvement. In this context, this work employs such novel technique which consist of using Schmitt Trigger (ST) inverters for process variability mitigation on different Full Adder topologies with priority on power consumption variations. Performance, power, and area penalty were analyzed alongside variability robustness.

This work is divided into five further sections: FinFET Technology where its characteristics and major variability impact are explained, Variability Effects and Mitigation Techniques, with a theoretical foundation about variability. Motivation and Objectives, explaining in more details this work's objective. Methodology, presenting how results were achieved with its experimental setup. The Results and Discussion presenting the simulation results and its analysis. And, lastly, the Conclusions.

2 FINFET TECHNOLOGY

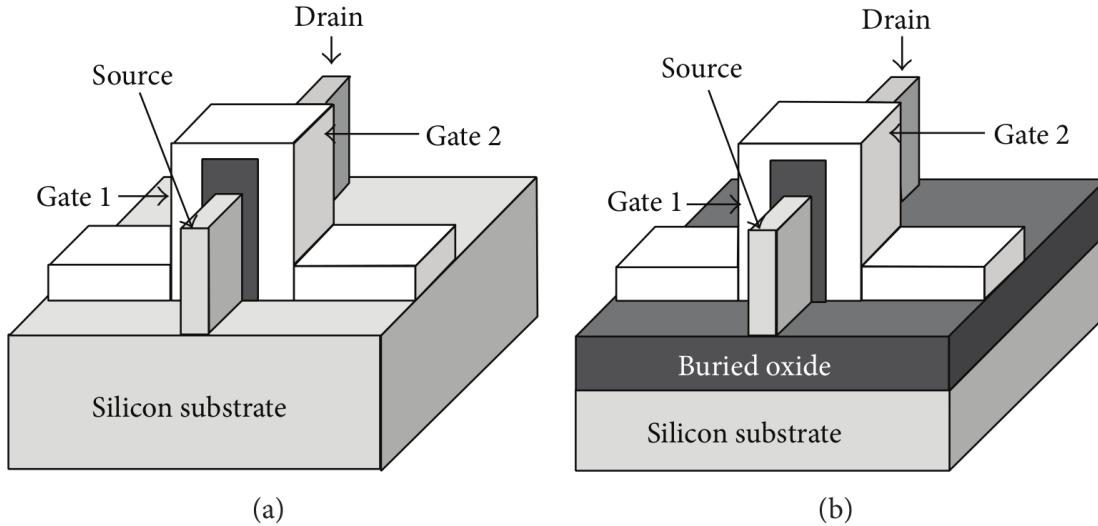
Promising new commercial technologies based on the Fin Field Effect Transistor (FinFET) devices have been introduced to maintain the technology scaling. The FinFET main geometric parameters are the gate length (L or LG), fin width (W_{FIN} , T_{FIN} or TSI), fin height (H_{FIN}) and Oxide Thickness (TOX). FinFET technology can be built on a traditional bulk or Silicon on Insulator (SOI) substrate with a conducting channel that rises above the level of the insulator, creating a thin silicon structure, the gate as shown in Figure 2.1 and 2.2. FinFET devices can be shorted-gate (3 gate nodes) or independent-gate (4 gate nodes). The shorted gate model is similar to the traditional MOSFET given that the front-gate and back-gate are connected and controlled by the gate signal. The independent gate has 4 nodes, making possible to connect the front and back gate to different voltage values.

Figure 2.1: Structural comparison between (a) planar MOSFET and (b) FinFET.



Source: Bhattacharya and Jha (2014)

Figure 2.2: Structural comparison between (a) bulk and (b) SOI FinFETs.



Source: Bhattacharya and Jha (2014)

The channel being surrounded from three dimensions by the gate results in a superior control, reduced short-channel effect (SCE) and eliminated random dopant fluctuation (RDF) effect due to the fully depleted channel that causes less sensitivity to process variations (TAUR; NING, 2013). FinFETs also present relative immunity to gate line-edge roughness, a major source of variability in planar nanoscale FETs (KING, 2005). The disadvantage over MOSFETs is the harder manufacturing process due to difficulty in the lithography steps as it is increasingly difficult to print small patterns, the increased variability impact due to the further minituarization of dimensions, in comparison to MOSFET and more constly manufacturing process due to the need of techniques to address the manufacturing imprecision and, in the case of SOI FinFET, to change the CMOS substrate process to support a SOI substrate manufacturing process (KING, 2005) (MANOJ et al., 2007).

Several works analyze the FinFET reliability. In (HARRINGTON et al., 2018) it is shown, at 14/16nm fabricated bulk FinFET technology, that for high energy charged particles, the drive current is the dominant factor to the transient fault pulse width and cross-section. And low energy particles have a grater dependence on secondary transistor and circuit design factors (number of fins, transistor arrangement, etc).

In (REN et al., 2018) the hot carrier injection (HCI) effect is analyzed in pass-gate FinFET transistors. The tests were executed using commercial FinFET technology showing a 50% chance of errors due to HCI in pass-gate transistors. In (XIONG; BOKOR, 2003) a analysis of the sensitivity of double-gate and FinFET devices to process vari-

ations is shown. It is concluded that for 20nm FinFET devices large channel doping concentration is necessary to obtain suitable values of threshold voltage if heavily doped polysilicon gates are used. Due to the small volume of the channel the channel doping will bring unacceptable V_{TH} fluctuations. Given that, heavily doped polysilicon may not be a viable choice with the work function adjustment being a better approach.

In (ZHANG et al., 2017) the modeling of the reliability degradation of a FinFET-based Static Random Access Memory (SRAM) is shown. It is concluded that the probability of failure due to Bias Temperature Instability (BTI) and Gate Oxide BreakDown (GOBD) is relatively lower in comparison to HCI-induced failures. They also show the improvement of lifetime due to Error-Correcting Code (ECC) memory. In (LIAO et al., 2008) a investigation on reliability characteristics of NMOS and PMOS FinFETs is conducted. Based on fabricated FinFETs transistor with 17-27 nm width, it was shown that the life time of FinFET is very dependable of its dimensions. The predicted lifetime for a 50nm gate length NMOS FinFET was 133 years, for the first HCI event. While a 27nm fin-width PMOS FinFET showed 26.84 years of lifetime which is reduced to 2.76 years when reducing its fin-width from 27 to 17 nm for a NBTI event, showing the huge reliability challenge introduced by technology scaling.

Given the majority of papers exploring the reliability factors and its effects but the few that actually study mitigation techniques, this paper aims to bring a layout level analysis of a novel technique for robustness improvement. There is no evaluation in the literature of the impact of the ST technique at layout level as well as in FinFET technology.

3 VARIABILITY EFFECTS AND MITIGATION TECHNIQUES

Standard CMOS devices have been optimized for high-speed and low-power consumption through its lifetime being the backbone of almost all modern digital circuits. The periodic process of technology scaling has resulted in faster and more energy efficient transistor than the previous generation. As channel lengths shrank below 50nm, the ratio of device size to atom-size becomes smaller, hence, a variable structure at the atomic scale has an increased effect on device behavior. There have been advances to reduce the loss of precision due to the manufacturing process. However, the intrinsic quantum-mechanical limitations cannot be overcome, with their impact increasing as the technology shrinks further (ASENOV, 1999).

Variability can occur in both spatial and temporal domains with deterministic and stochastic fluctuations (WALKER et al., 2010). In summary, variability consists of deviation of characteristics, internal or external, to the circuit, which can determine its operational features such as power and delay. These characteristics, or factors, as we addressed them for the rest of this work, can be divided into three types:

Environmental Factors: Caused by temperature fluctuations and voltage drops. Voltage drops occurs due to abrupt changes in the switching activity, causing large current transients in the system, which can occur locally as well globally across the die (NASSIF, 2008).

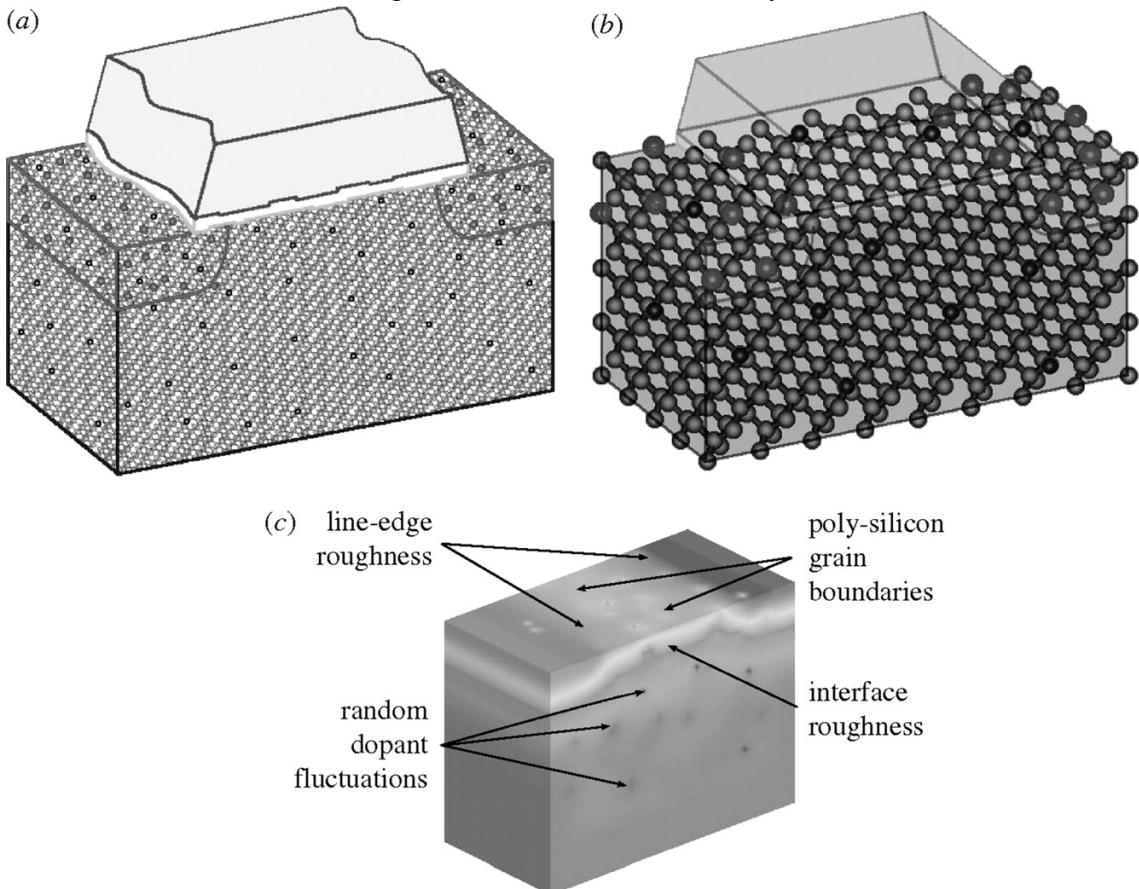
Reliability Factors: Related to the aging process of the circuit, it is introduced by negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), electromigration, time dependent dielectric breakdown, gate oxide integrity, thermal cycling and hot carrier injection (NASSIF, 2008).

Physical Factors: It is related to variations caused by the manufacturing process, due to imprecisions in lithography stage, which results in deviations in the electrical parameters defining the behavior of active and passive devices. Those variations can be divided in three types of mechanisms: Systematic, they repeat over many chips or wafers. Design dependent, being particular to each circuit design. And Random, which depends on the random aspects of process manufacturing, as shown in Figure 3.1 (NASSIF, 2008).

Additionally, the technology scaling and manufacturing tolerances are not correspondingly moving side by side. For instance, the pace at which the effective channel length is reduced is faster than the improvement of mask fabrication error and mask overlay control (NASSIF, 2008) (AGHABABA; AFZALI-KUSHA; FOROUZANDEH,

2009).

Figure 3.1: Transistor Variability



Source: Walker et al. (2010)

These three types of variabilities, in conjunction, may prevent circuits from meeting their performance and power goals. Table 3.1 demonstrates the design impact of performance and power due to different types of variability.

Table 3.1: Design impact on performance and power due to different types of variability

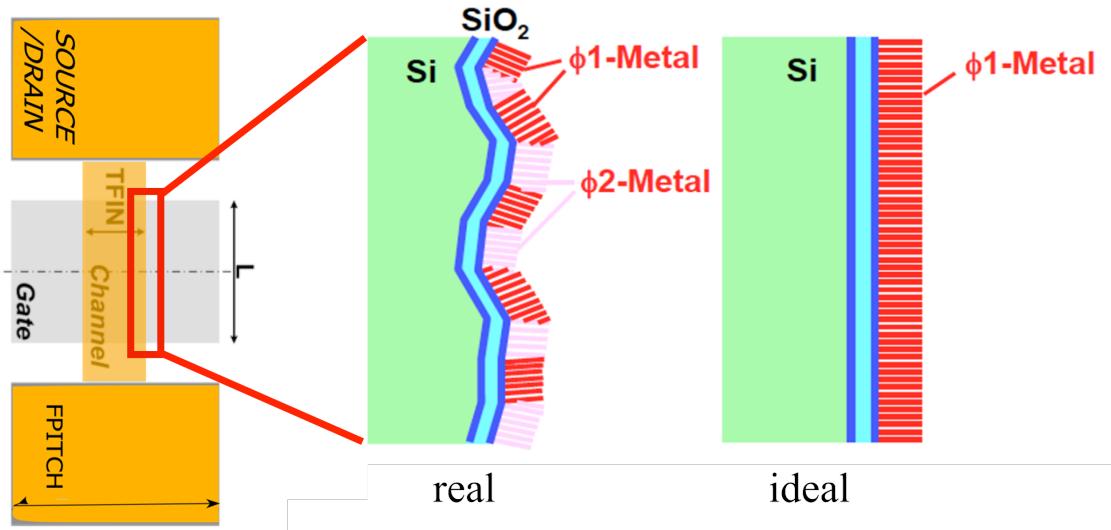
Property	Ease of measuring	Variability	Effects of Variability	Effect of missing specification
Performance	Medium	Medium: up to 60%	L, W, R, C, V _{th} , μ	Slower product, yield, timing error
Leakage Power	Easy	Large: up to 148%	L, V _{th} , μ , tox	Shorter battery life, yield, heat
Dynamic Power	Difficult	Workload dependent	C, α	Shorter battery life, heat

Source: Rahimi, Benini and Gupta (2016)

This work evaluates the effects caused by the physical variability. In FinFET, the physical variations are responsible for deviations in the device work function (WF), gate length (LG), fin height (HFIN), fin thickness (TSI) and parasitic resistances. It is shown in (MEINHARDT; ZIMPECK; REIS, 2014) that work function fluctuation (WFF) is the main cause of threshold voltage (V_{TH}) variations. Alongside, in (WANG et al., 2011) is

shown the high correlation between the variability in the on (ION) and off (IOFF) currents and VTH fluctuation in the presence of granularity of the metal gate. The main cause of WFF is due to its dependency over the orientation of its metal grains. In the real fabrication process, metal gate devices are generally produced using multiple types of metal with different work functions randomly aligned as depicted in Figure 3.2. In the ideal fabrication process, metal gate devices have the gates manufactured with uniformly aligned metal and then, they have very low WFF deviation (DADGOUR et al., 2010).

Figure 3.2: Metal gate fabrication ideal and real aspects.



Source: Meinhardt, Zimpeck and Reis (2014)

3.1 Related Works

At circuit level there is multiple techniques to predict and prevent errors: Tuning CMOS knobs, circuit topology optimizations, self-timed circuits, temporal and logical error masking, relaxed retiming and graceful degradation, and inexact circuits. Although, there are few approaches to decrease the process variability at its core. It is due to the technology dependency present in this problem (RAHIMI; BENINI; GUPTA, 2016).

It can be observed that many works try to indicate the most robust design for a given type of circuit. For example, in (DOKANIA; IMRAN; ISLAM, 2013) twelve different Full Adder topologies are analyzed considering delay, power and Power-Delay-Product (PDP) variability. It is used a 16nm bulk CMOS technology node in SPICE simulations with Process, Voltage and Temperature (PVT) variability being considered and Monte Carlo simulations performed. The authors concluded that Cell A, CLRCL and

Cell B full adders presented the best results for all three metrics (Delay, Power and PDP).

In (AMES et al., 2016) the effects of PVT variability in different full adder designs are investigated. The simulations are performed in HSPICE with the bulk CMOS 32nm node technology. With Transmission Gate Full Adder (TGA) and Transmission Function Adder (TFA) architectures showing acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested full adders - 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) Full Adder.

In (ISLAM; HASAN, 2011) various popular 1-bit digital summing circuits functionality and robustness are analyzed in light of PVT variations with the best full adder being simulated in Carbon Nanotube Field Effect Transistor (CNFET) technology for comparison with the bulk CMOS version. The simulations are carried at the 22nm bulk CMOS and CNFET technology node in HSPICE. Its results show that the TGA has the strongest PVT variability robustness and its CNFET version provides over 3x, 1.14x and 1.1x less propagation delay, power dissipation and energy delay product (EDP) variations, respectively. This work does not consider the total power consumption of each full adder separately.

Some articles analyze the adoption of new technologies: (GUDURI; ISLAM, 2015) proposes a hybrid of bulk CMOS and CNFET Full Adder at 16nm in deep sub-threshold operation region for ultralow-power applications simulated in SPICE which showed some improvement over its bulk CMOS Full Adder counterpart achieving 5% and 1% improvement in power, power-delay and energy-delay products and their variability, respectively.

In (ISLAM; AKRAM; HASAN, 2011) a new subthreshold-FinFET Full Adder is proposed and compared over multiple full adders showing huge metric improvements provided by the FinFET technology up to 2.22x improvement in power variability. It was simulated in 32nm predictive technology model on HSPICE.

It is notable that none of these works consider a layout approach for its simulations and do not address any novel general technique which can be applied to a range of different types of circuits. Although, some works introduce novel designs.

(FEDERSPIEL et al., 2012) presents reliability comparison between 28nm bulk CMOS and Fully Depleted Silicon On Insulator (FDSOI) technologies at layout level, with FDSOI showing 32% improved performance, 40% reduced power consumption and improved matching, with its intrinsic reliability behavior similar to 28nm bulk at the device level. (ALIOTO; PALUMBO, 2007) presents a study about the delay variability

caused by supply variations in the TGA. The experiments were performed at 90nm and 180nm bulk CMOS Technology in Spectre at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TGA presenting worse results 15% (25%) for the 90 nm (180 nm) in comparison to static logic.

Some works focus on evaluating techniques: In (ZIMPECK et al., 2016) three transistor sizing techniques are applied on a set of cells and their impact on variability robustness is analyzed. The simulations were performed considering a 14nm FinFET technology using HSPICE tool. The authors concluded that the Optimized Transistor Sizing (OTS) technique has the best ratio between nominal PDP and PDP under process variability.

(AHMADI; ALIZADEH; FOROUZANDEH, 2017) introduces a new technique to improve the performance of digital circuits in the presence of variations. It consists of a hybrid of two former methods to prevent errors due to delay variations. The simulations were performed with a 45nm predictive technology using HSPICE and applied on ITC'99 and ISCAS'89 benchmarks circuits. The results show that this hybrid technique can tolerate process variations up to 27.3% better than state-of-the-art techniques.

Among these works there is (DOKANIA; ISLAM, 2015) on which a novel technique based on the replacement of Full Adder's internal inverters with low voltage Schmitt Triggers for PVT variability robustness improvement is originally introduced and applied on seven different full adder designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in PDP. Although, the improvements occur at the cost of an increase in the area and power dissipation of each design.

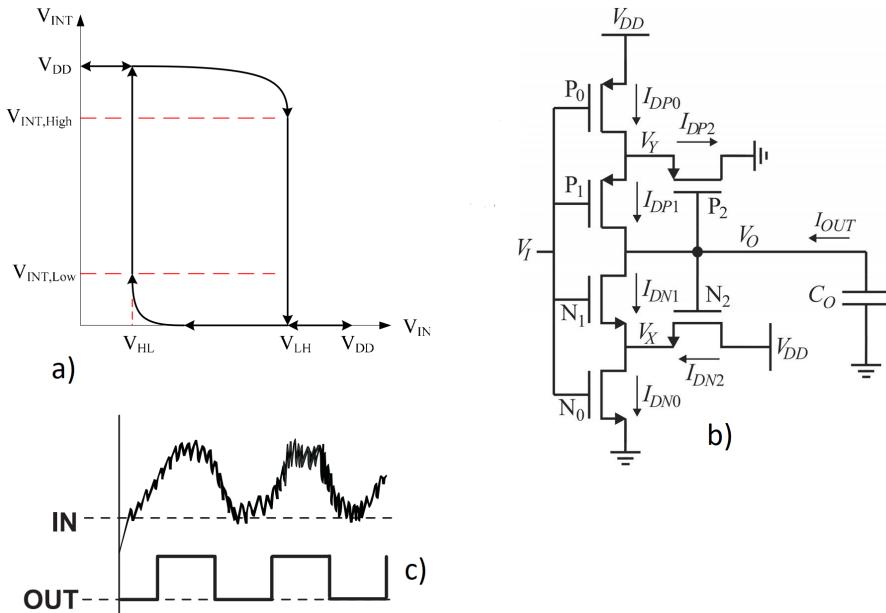
Alongside, in (TOLEDO; ZIMPECK; MEINHARDT, 2016) the ST technique is applied on four Full Adders. It presented promising results regarding the power deviation due to the process variability with a decrease up to 79% with a drawback of a significant increase in average energy consumption. The simulations were performed with the 16nm technology predictive technology model in NGSPICE.

Schmitt triggers are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. On a typical input (non-Schmitt trigger), its binary value will switch at the same point on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit

causing a shift in the threshold voltage.

If the threshold shifts, it will cross the input causing it to switch again. It can go indefinitely causing oscillation. The same thing can happen if there is noise on the input. Schmitt Triggers are applied in these cases to filter noise introducing superior and inferior threshold voltages, as shown in Figure 3.3.c. The difference between the thresholds is called Hysteresis (COCKRILL, 2011), its curve is shown at 3.3.a. According to the Schmitt Trigger behavior, it can mitigate the influence of variations in the inputs product of PVT variability. In figure 3.3.c is shown a classical CMOS Schmitt Trigger design.

Figure 3.3: a) General ST hysteresis curve b) Classical CMOS ST Topology c) Typical signal filtering with ST.



Source: Cockrill (2011)

This technique is tested in several works: In (AHMAD et al., 2016) it is presented a novel Schmitt-trigger-based single-ended 11 Transistor SRAM cell. It analyses its performance against seven different SRAM topologies. The novel cell showed the least energy consumption per operation with the smallest leakage power and a 6.9x higher Ion/Ioff ratio. Further PVT variability simulations confirmed the robustness of the design regarding read and write operation. The simulations were carried in 22nm predictive technology using HSPICE.

(MOGHADDAM; MOAIYERI; ESHGHI, 2017) presents a Schmitt trigger (ST) buffer using CNFET. It was evaluated against other two buffers and showed, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain consider-

ing PVT variability robustness. The simulations were carried in 16nm Stanford CNFET model using HSPICE.

4 METHODOLOGY

For the experiments, there were considered four different types of Full Adders topologies to evaluate their robustness to process variability with their internal inverters replaced by Schmitt Triggers. The Full Adders listed below have been chosen due to their promising results in related works (AMES et al., 2016) (DOKANIA; ISLAM, 2015) (DOKANIA; IMRAN; ISLAM, 2013):

1. Complementary MOSFET Adder (CMOS)
2. Transmission Gate Adder (TGA)
3. Transmission Function Adder (TFA)
4. Hybrid Full Adder

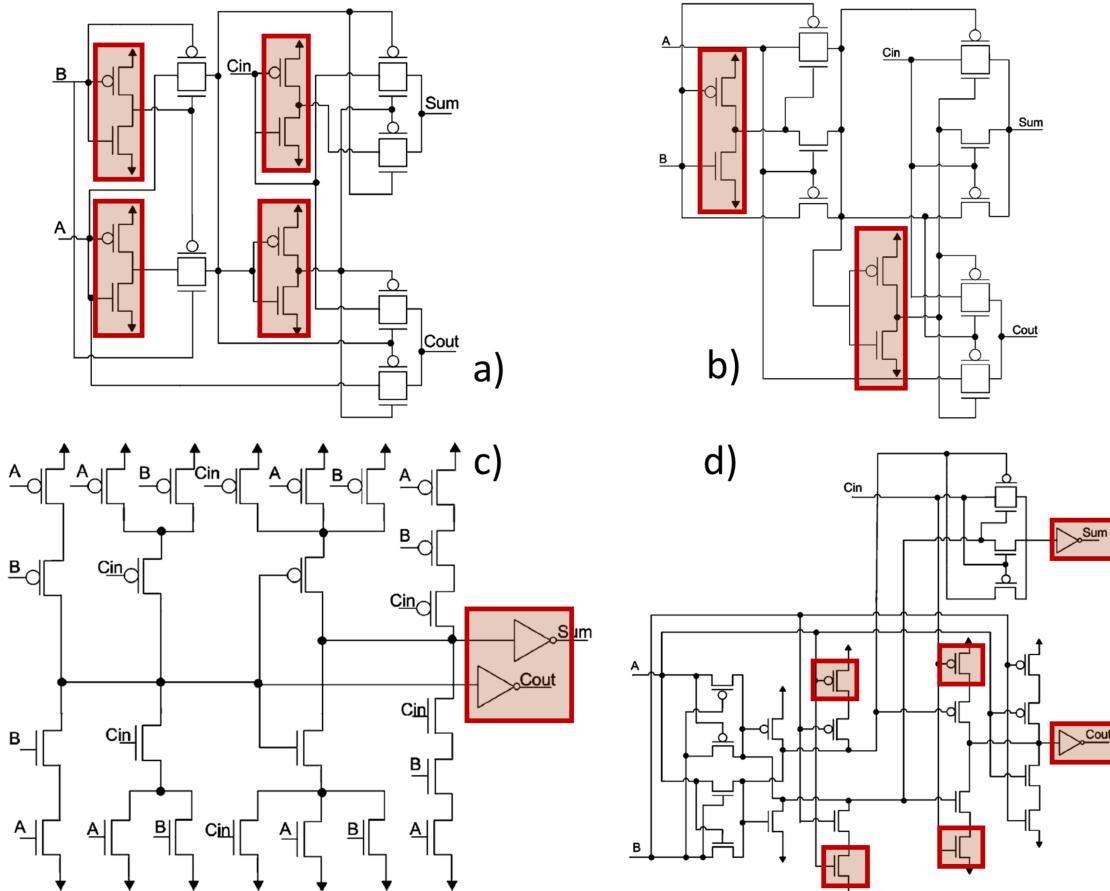
The CMOS Full Adder is considered the most traditional Full Adder topology containing 28 Transistors arranged in a pull-up and pull-down networks, which are logically complementary. It has a full voltage swing and buffered Sum and Cout signal and the advantages of good conductibility and robustness when working with novel technologies and low voltages. However, it has high capacitance because each input is connected to the gate of at least a p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) device additionally, it shows the impact of the pull-up network that makes the circuit slower due to the low mobility of its holes (BECKETT, 2002) (DEVADAS; KISHORE, 2017) (ISLAM; HASAN, 2011).

Transmission Gate Full Adder (WESTE; ESHRAGHIAN, 1985) contains 16 transistors, and is a high speed and low power design. However, shows low driving capability which may be unacceptable in some cases where there is a long chain of full adders due to the increase in delay (ISLAM; HASAN, 2011). The Transmission Function Adder is based on transmission gates as well, containing 20 transistors, working satisfactorily with low voltages but losing performance when cascaded due to the lack of supply/ground contacts and, consequently, driving capability (NAVI et al., 2009). Both TFA and TGA generate the XOR function ($H = A \text{ XOR } B$) followed by an inverter which produces the XNOR function (H'). H and H' are used to control the transmission gates generating the Sum and Cout outputs. The inverter generates delay between H and H' , which will cause the transmission gates to behave as pass transistors, that may introduce glitches and consequently, increase the power consumption of these cells. Additionally, TGA contains three inverters, one more than TFA. The inverters switching introduce more short-circuit

power (SHAMS; BAYOUMI, 2000).

Inspired by CMOS and CPL Full Adders architectures, the Hybrid Full Adder (NAVI et al., 2009) contains 26 transistors, with the main advantage of a high output signal and low power properties. Although, the design shows high input capacitance for specific input vectors. The Full Adder designs are shown in Figure 4.1.

Figure 4.1: Full Adders with internal inverters to be replaced highlighted.

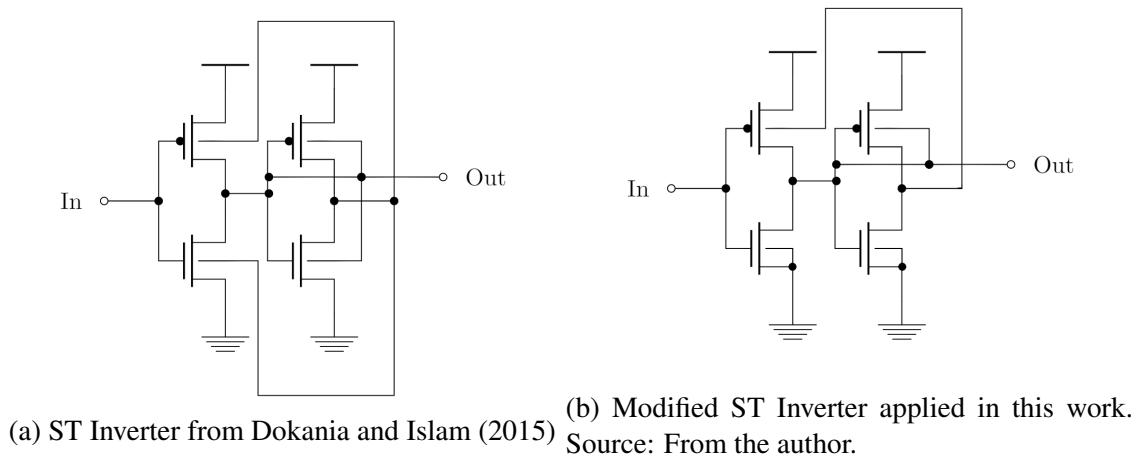


Transmission Gate Adder (a), Transmission Function Adder (b), Mirror CMOS Adder (c) and Hybrid Full Adder (d). Source: Toledo, Zimpeck and Meinhardt (2016)

A variety of CMOS Schmitt Trigger designs have been proposed and implemented over the years, with the conventional 6T-CMOS Schmitt Trigger proposed in (DOKI, 1984) exhibiting the wanted characteristics of different high-to-low and low-to-high transition threshold voltages, giving rise to hysteresis. The ST inverter circuit used in this work was inspired by (ZHANG; SRIVASTAVA; AJMERA, 2003) and modified in (DOKANIA; ISLAM, 2015) to achieve the desired inverting characteristic, as shown in Figure 4.2a. It is designed for operation at a supply voltage of 0.4V in order to achieve low power consumption, and consists of the junction of two inverters where the output from the second one will be the bulk for the first one.

In this design a dynamic body-bias technique is applied through a feedback mechanism to a standard CMOS inverter circuit, thus allowing a change in the threshold voltages of two MOSFETs, implying a change in the switching voltage.

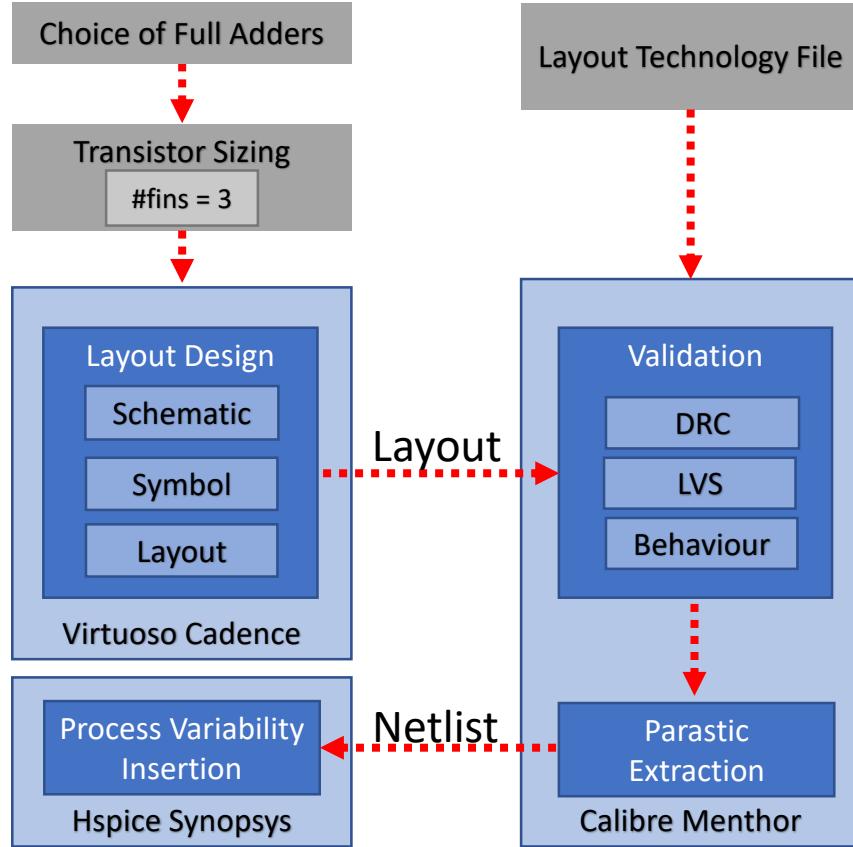
Figure 4.2: Original and modified STs side-by-side



(a) ST Inverter from Dokania and Islam (2015) (b) Modified ST Inverter applied in this work.
Source: From the author.

The project was divided into two main steps: The layouts design and the electrical simulations. Before the layouts design the Full Adders were chosen, based on (DOKANIA; ISLAM, 2015) and the transistors were sized (it was chosen 3 fins for each transistor). At Layout Design, each Full Adder schematic, symbol and Layout was designed. After finishing the layout design, each layout passed through validation which consisted from a Design Rule Checking (DRC) to detect if the layout obeys the technology geometry restrictions and layer rules, Layout Versus Schematic (LVS) where layout and schematic are compared to detect if they are equals (same nodes and nets) and a Behavior test. After validation the layout netlist is generated with parasitics extracted. And, finally, the netlist is instantiated in a spice file with the technology WF variation inserted to simulate process variability. The design flow is shown at Figure 4.3. In the end there was chosen 4 Full Adders. Each one was designed with and without the ST technique resulting in 8 layouts.

Figure 4.3: Design flow of the experiments.



Source: From the author.

4.1 Layout Design

All Full Adders layouts were designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence® with the process design kit (PDK) of 7-nm FinFET or Arizona State Predictive PDK (ASAP7) from the Arizona State University in partnership with ARM (CLARK et al., 2016). It is the only available 7nm PDK for academic use, resulting in a very realistic estimative. This PDK was chosen due to realistic design conjecture regarding the current design competencies. Due to limitations of ASAP7 technology, it is not possible to connect the NMOS bulks separately due to the shared substrate. Given that, the Schmitt Trigger behavior is preserved with only minor changes between charging and discharging delays due to the difference between PMOS and NMOS threshold voltages. The ST applied in this work is shown at Figure 4.2b.

The main PDK rules and lithography assumptions considered in this work are shown in Table 4.1. To exemplify the PDK layers, the traditional CMOS Full Adder

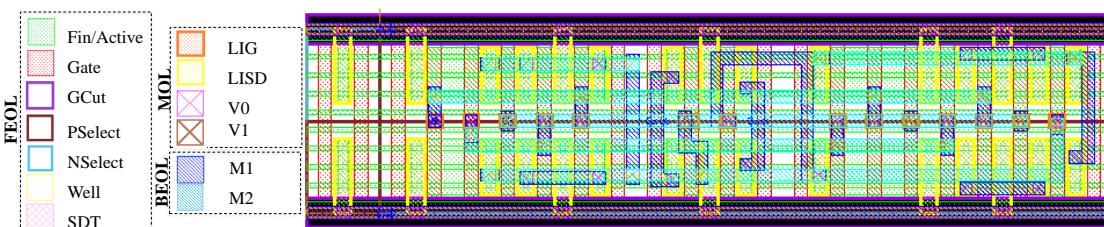
layout is shown in Fig. 4.4. For all layouts it was used a dense 7.5 M2 (Metal 2) track cell, baseline resulting in a 270nm cell height. This corresponds to three fins for each transistor as shown in Figure 4.5. To make the back-gate connections it is necessary a TAP-Cell. It is responsible to connect the NMOS and PMOS back-gates to supply/ground, respectively, being possible to connect the PMOS back-gates to another node. It is a PDK restriction needed for the proper function of the circuit. Its layout has a length of 108nm resulting in an area of $0.02916 \mu\text{m}^2$ as shown in Figure 4.6.

Table 4.1: Key layer lithography assumptions, widths and pitches

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

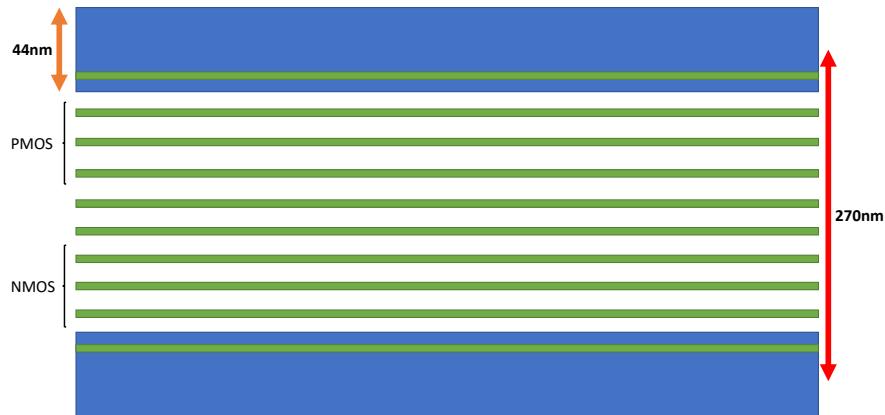
Source: Clark et al. (2016)

Figure 4.4: Technology layers and original Mirror CMOS Layout



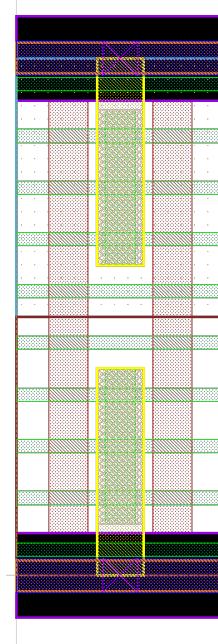
Source: From the author.

Figure 4.5: Transistor height and number of fins.



Source: From the author.

Figure 4.6: TAP-Cell Layout.



Source: From the author.

4.2 Electrical Simulation

The simulations were carried out in HSPICE considering the new netlist obtained after the physical verification flow and the parasitic capacitances extraction. Each full adder was designed with and without the Schmitt Triggers replacement to consider the penalties due to the adoption of the ST technique in terms of area, energy and per-

formance. There was performed simulations at nominal supply level (0.7V) and near-threshold level (0.4V) with a frequency of 1GHz for the signals.

The process variability evaluation was taken, after the layout parasitic extraction through Calibre® from Mentor Graphics, through 2000 Monte Carlo (MC) simulations (ALIOTO; CONSOLI; PALUMBO, 2015) varying the threshold voltage of the PMOS and NMOS devices according to a Gaussian distribution considering a 3σ deviation of 5% variation from the WFF nominal values. For all experiments, it was observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: delay, power and energy, where σ/μ represents the sensibility of the cell to process variability.

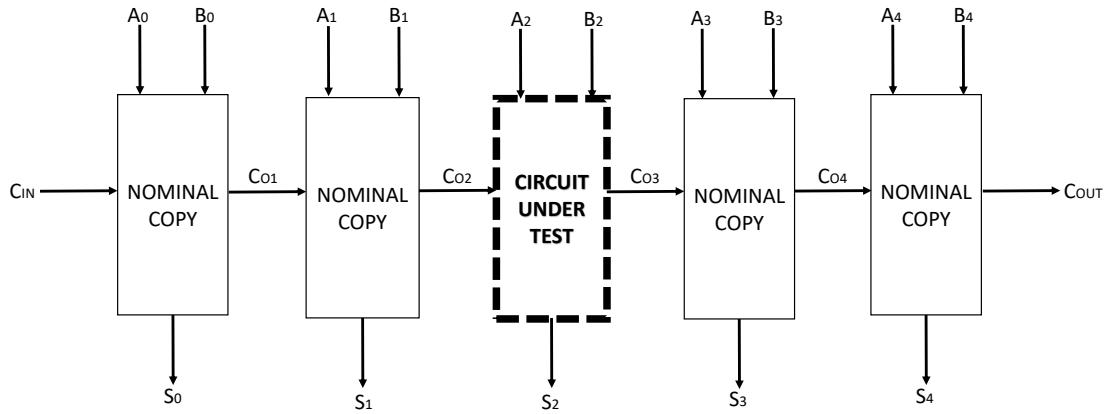
The reference values from ASAP7 technology for electrical simulations are shown in Table 4.2. To avoid underestimating effects of realistic input waveforms on design metrics, the simulations were carried under a 5-bit ripple carry adder using copies of the 1-bit full adder cell with design metrics being calculated for the middle cell as shown in Figure 4.7.

Table 4.2: Parameters applied in the electrical simulations

Parameter	7nm
Nominal Supply Voltage	0.7 V
Gate Length (LG)	21nm
Fin Width (WFIN)	6.5nm
Fin Height (HFIN)	32nm
Oxide Thickness (TOX)	2.1nm
Channel Doping	$1 \times 10^{22} m^{-3}$
Source/Drain Doping	$2 \times 10^{22} m^{-3}$
Work Function	NFET 4.372
	PFET 4.8108

Source: Clark et al. (2016)

Figure 4.7: Test Bench.



Source: Dokania and Islam (2015)

5 RESULTS AND DISCUSSION

The results are organized into two main analysis: the set of full adders were evaluated at nominal voltage conditions and operating at a near-threshold (Nt) region with supply voltage equal to 0.4V. In both cases, the process variability is considered and simulations with and without the ST technique is performed. To highlight the improvements and drawbacks of the ST technique for each FA, results also show the relation (Δ) between the deviation of traditional and ST circuits. For each output (Sum and Carry Out) delays and energy measures were considered. All analysis was made at layout level with the 7nm ASAP technology node, with all parasitics considered.

5.1 Nominal Voltage Operation

At nominal supply voltage, carry-out generation is always the critical path, considering or not the variability effects. According to the Table 5.1 and Table 5.2, it is possible to observe an increase on the mean of delay and energy for all circuits when the ST technique is inserted in the design compared to traditional one.

TFA presented the best performance and the lowest energy consumption for nominal voltage operation. However, TFA presented high maximum values and large standard deviation that are essential points to be considered. These points are a consequence of the heavy signal degradation on the TFA outputs, leaving the TFA for high-performance applications more indicated to technology nodes with low process variability sensibility. The CMOS adder showed the smallest standard deviations being the most recommended for technology nodes with high variability.

The TGA showed the lowest maximum delays, resulting from the lowest average absolute standard deviations. Although, not presenting the lowest normalized deviation. The Hybrid showed high values for maximum delays (only after the TFA maximum) and the highest mean delays.

For delays, there was improvement over the Sum (Carry Out) output for the TFA (TGA) with a 37.43% (15.77%) higher variability robustness. The CMOS and Hybrid FAs did not show any considerable improvement/worsening. Although, the Carry Out (Sum) output for the TFA (TGA) showed a 25.64% (11.65%) robustness worsening.

The results obtained in this work are in the face of the results found to 16nm Predictive Technology Model (PTM) High-Performance technology (CAO, 2018) in (TOLEDO;

ZIMPECK; MEINHARDT, 2016). 7nm layout with ASAP7 technology shows significant improvement on the energy robustness (over 18%) at nominal voltage and in some cases also in the delay robustness to process variability.

According to Table 5.2, ST circuits increased the mean energy about close two times considering the energy necessary to cover all timing arches to the SUM output. The effect is lighter on the Carry-Out total energy. But, although this penalty, the benefits of ST technique on the cell robustness against process variability are considerable. All the ST FA circuits have the deviation reduced. Hybrid presented the best improvement on energy robustness, with 30% more stability. Fig. 5.1 resumes the improvement reached with the ST technique on Delay and Energy.

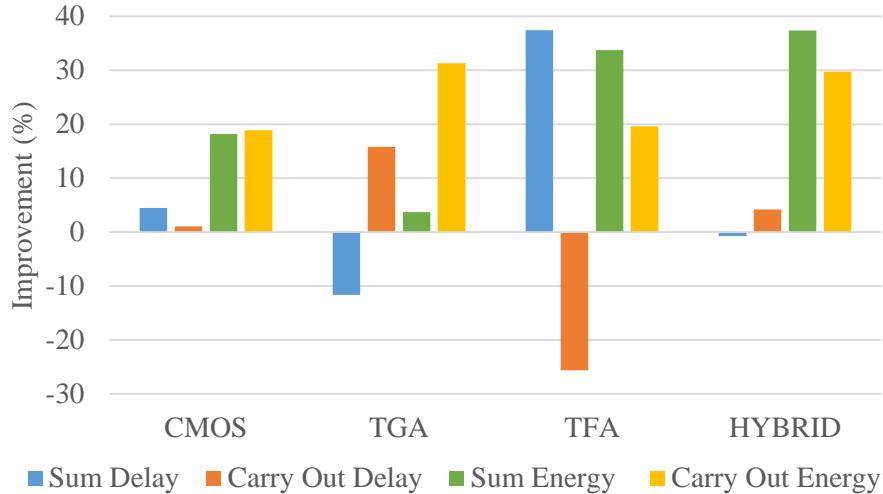
Table 5.1: Delay measures for nominal voltage operation.

@Nominal Voltage	Delay									
	SUM					CARRY OUT				
	Max (ps)	μ (ps)	σ (ps)	σ/μ (%)	Δ (%)	Max (ps)	μ (ps)	σ (ps)	σ/μ (%)	Δ (%)
CMOS	93.19	16.11	3.83	23.31	4.46	104.48	27.38	5.92	21.60	1.05
CMOS ST	117.19	21.98	4.98	22.27		120.01	33.09	7.08	21.38	
TGA	63.13	14.51	3.28	27.94		60.11	16.32	4.28	28.54	
TGA ST	77.71	17.63	3.80	31.20	-11.65	71.82	21.19	4.77	24.04	15.77
TFA	1016.90	12.63	10.62	58.94		2010.20	14.74	13.77	77.59	
TFA ST	83.52	15.39	4.16	36.88	37.43	2030.50	22.72	37.42	97.48	-25.64
HYBRID	117.57	18.15	4.42	23.72		65.29	17.30	4.18	25.57	
HYBRID ST	192.48	25.92	6.55	23.90	-0.75	96.40	23.27	5.64	24.50	4.20

Table 5.2: Energy measures for nominal voltage operation.

@Nominal Voltage	Energy									
	SUM					CARRY OUT				
	Max (fJ)	μ (fJ)	σ (fJ)	σ/μ (%)	Δ (%)	Max (fJ)	μ (fJ)	σ (fJ)	σ/μ (%)	Δ (%)
CMOS	69.07	12.89	2.97	23.00		83.43	20.88	3.52	16.87	
CMOS ST	93.07	20.26	3.81	18.81	18.21	98.66	30.69	4.20	13.68	18.91
TGA	60.36	11.78	2.36	20.04		92.71	13.54	4.15	30.61	
TGA ST	90.61	22.99	4.44	19.30	3.71	93.03	24.79	5.21	21.03	31.32
TFA	21.94	4.45	0.92	20.67		29.74	4.96	1.14	22.99	
TFA ST	29.28	10.59	1.45	13.70	33.73	53.74	10.58	1.96	18.48	19.62
HYBRID	86.45	12.99	3.63	27.97		93.88	19.99	3.89	19.48	
HYBRID ST	87.13	23.67	4.15	17.52	37.38	98.85	35.58	4.87	13.69	29.74

Figure 5.1: Robustness improvements for each Full Adder at nominal voltage operation.



Source: From the author.

5.2 Near-Threshold Operation

At near-threshold, variability compromises the FA circuits on some cases making the SUM output the critical path instead of the Carry-out generation, observing the maximum values found. Table 5.3 presents the delay results of the near-threshold operation.

The energy results to near-threshold operation are presented in Table 5.4. Operating at low voltage reduces the mean energy over 30% for CMOS, TFA and Hybrid FAs and at least 15% of TGA compared to nominal voltage operation. As stated on (DOKANIA; ISLAM, 2015), the ST technique at NT operation reduces the delay and energy deviation for all circuits. However, the lag of the circuits is considerably higher at NT operation, emphasizing the need of circuit strategies to deal with variability.

TFA and TGA showed the highest deviations and high maximum delays, which is expected due to their pass-transistor logic and inherent signal degradation. The Hybrid adder showed higher deviations, delays and similar energy consumption in comparison to the CMOS Adder. Given that, the CMOS adder remains as a good choice for low power applications.

Results make clear the advantage of the technique when considering energy variability robustness. Fig. 5.2 shows the comparative evaluation of the improvement reached by ST technique at NT operation. Even when there was a worsening on delay robustness, the energy robustness presented improvements. The technique can introduce more delay variability given that variability determines the ST behavior as well, influencing its

delays, which stacks with the impact of multiple transistors in a series arrangement.

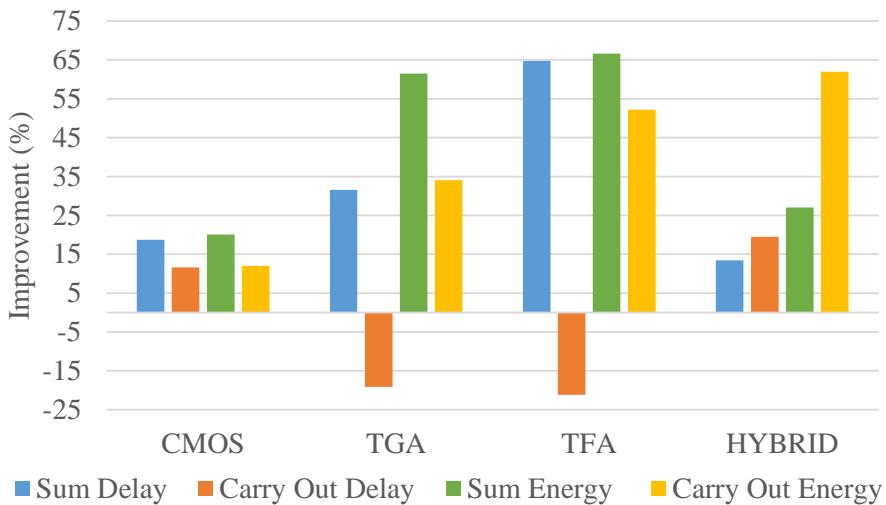
Table 5.3: Delay measures for near-threshold operation.

@NT	Delay									
	SUM					CARRY OUT				
	Max (ps)	μ (ps)	σ (ps)	σ/μ (%)	Δ (%)	Max (ps)	μ (ps)	σ (ps)	σ/μ (%)	Δ (%)
CMOS	873.41	73.22	56.38	77.47	18.70	794.87	128.65	86.67	67.39	
CMOS ST	430.85	95.85	60.57	62.99		539.77	143.77	85.67	59.57	11.61
TGA	7328.30	62.90	92.17	133.30		6396.90	325.25	138.02	173.54	
TGA ST	2386.40	127.54	106.22	91.26	31.53	6265.10	181.01	373.37	206.76	-19.14
TFA	1024.90	67.28	93.48	289.41		5734.20	151.02	286.55	227.50	
TFA ST	4202.20	84.34	79.51	102.05	64.74	6705.80	94.87	233.09	275.63	-21.16
HYBRID	830.64	95.23	77.95	79.00		695.28	78.00	56.73	73.90	
HYBRID ST	1212.00	120.92	86.26	68.39	13.43	2755.30	168.92	100.34	59.51	19.48

Table 5.4: Energy measures for near-threshold operation.

@NT	Energy									
	SUM					CARRY OUT				
	Max (fJ)	μ (fJ)	σ (fJ)	σ/μ (%)	Δ (%)	Max (fJ)	μ (fJ)	σ (fJ)	σ/μ (%)	Δ (%)
CMOS	45.37	6.29	2.00	31.81		20.07	51.91	9.97	2.09	20.97
CMOS ST	60.64	10.22	2.60	25.43		70.97	15.16	2.80	18.45	12.02
TGA	53.90	6.06	2.01	33.17		61.28	6.40	1.85	28.90	
TGA ST	34.33	11.30	1.44	12.79	61.45	85.49	11.67	2.22	19.06	34.04
TFA	16.26	2.40	0.65	27.05		23.03	2.58	0.64	24.66	
TFA ST	18.85	5.45	0.49	9.04	66.59	22.21	5.61	0.66	11.79	52.18
HYBRID	56.96	6.02	2.29	38.04		59.99	9.46	2.00	21.19	
HYBRID ST	81.05	11.65	3.23	27.75	27.06	26.22	15.03	1.21	8.07	61.91

Figure 5.2: Robustness improvements for each Full Adder at near-threshold operation.



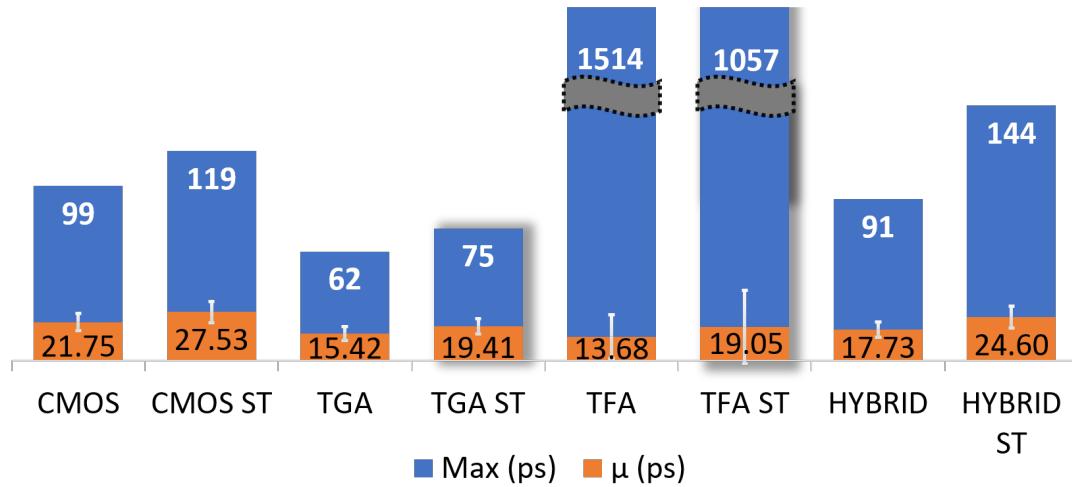
Source: From the author.

5.3 Penalties

It is expected that a technique which replaces a 2-transistor sub-circuit to a 4-transistor one should bring an impact over metrics. Given so, the average impact at nom-

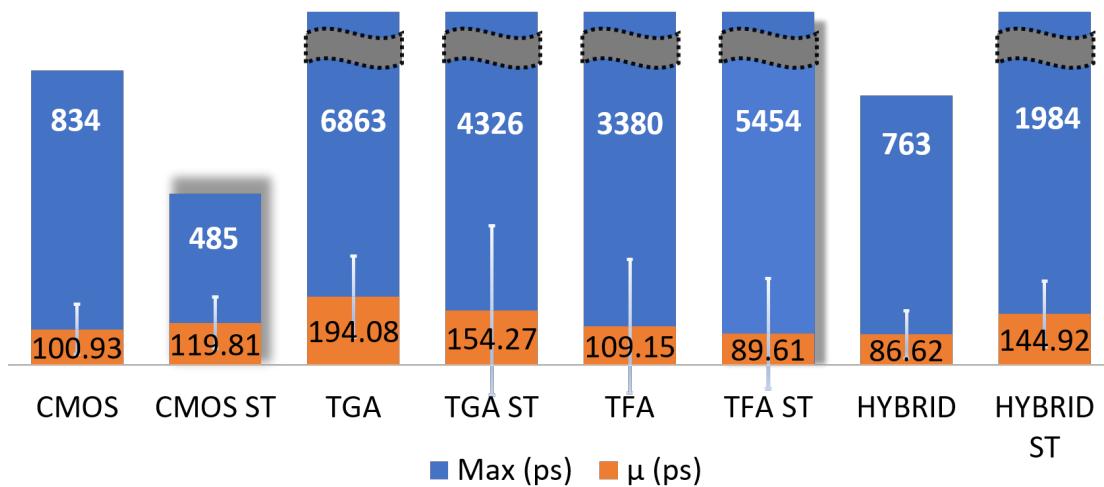
inal voltage operation was 30% over the delay and their absolute deviation values for nominal voltage and near-threshold operations. For nominal voltage operation, both outputs had similar penalties (35% increase in delays). For near-threshold operation the Sum output had a considerable higher penalty (47%) in comparison to the Carry Out output (12%). For delay deviation both operation regimes had similar results with an 8% increase for the Sum output and a 60% increase for the Carry Out output, which is expected since Carry Out is the critical path. Delay penalties are plotted in Figures 5.3 and 5.4.

Figure 5.3: Delay penalties at nominal operation due to technique application.



Source: From the author.

Figure 5.4: Delay penalties at near-threshold operation due to technique application.



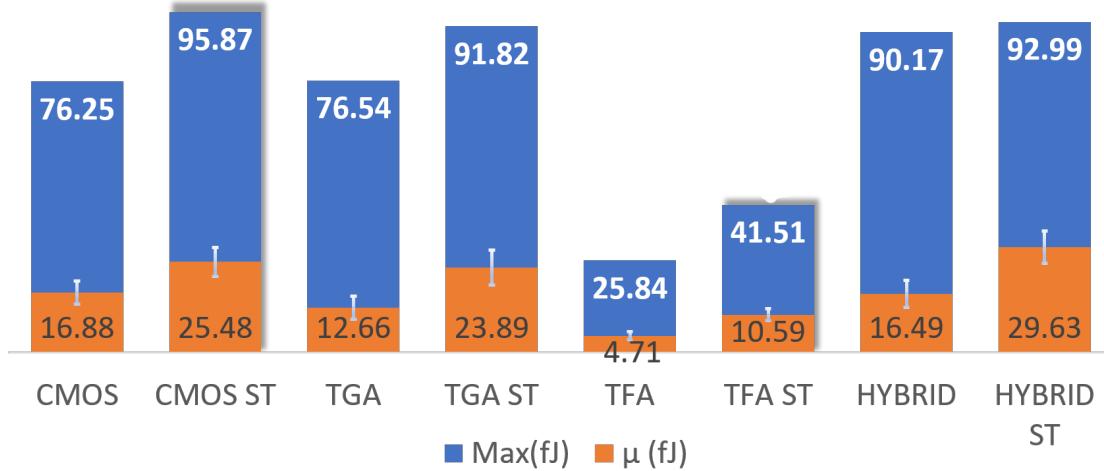
Source: From the author.

For energy, the impact is considerable, being on average over 85% percent higher. For energy standard deviations there was a 40% increase at nominal voltage and a minor

4% increase at near-threshold level. At both operation regimes and at both outputs the penalty for energy was similar, with a 93% increase for the Sum output and 80% increase for the Carry Out output. For the energy deviation, at nominal voltage operation there was a higher penalty for the Sum output (47%) in comparison to the Carry Out output (35%). At near-threshold operation both outputs had the same minor penalty of 4% on deviations.

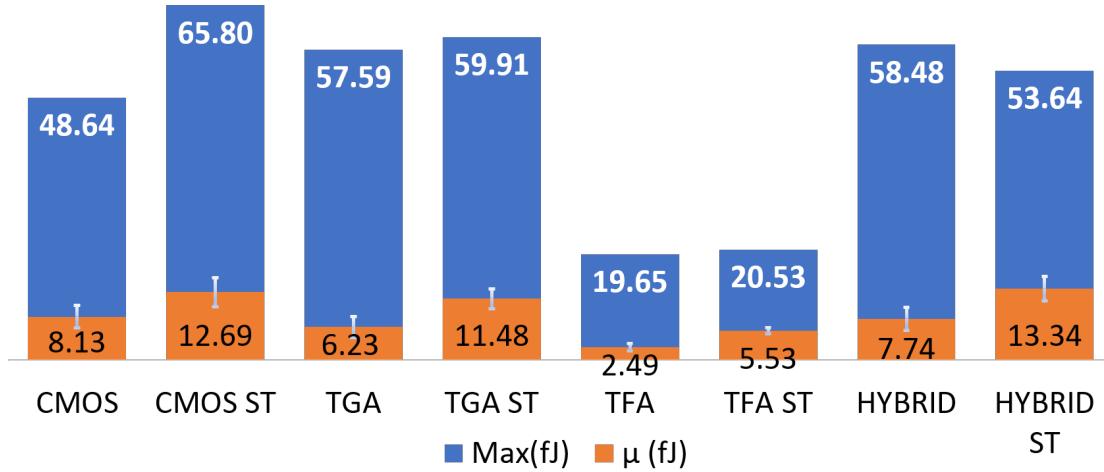
Overall, the worst penalties were the 47% increase in delays in Sum output at near-threshold operation, 59% increase on delay deviation in the Carry Out output at nominal operation, 93% increase at energy consumption for Sum output at both operation regimes and its 47% increase in energy deviation at nominal operation. Energy penalties are plotted at Figures 5.5 to 5.6.

Figure 5.5: Energy penalties at nominal operation due to the technique application.



Source: From the author.

Figure 5.6: Energy penalties at near-threshold operation due to the technique application.



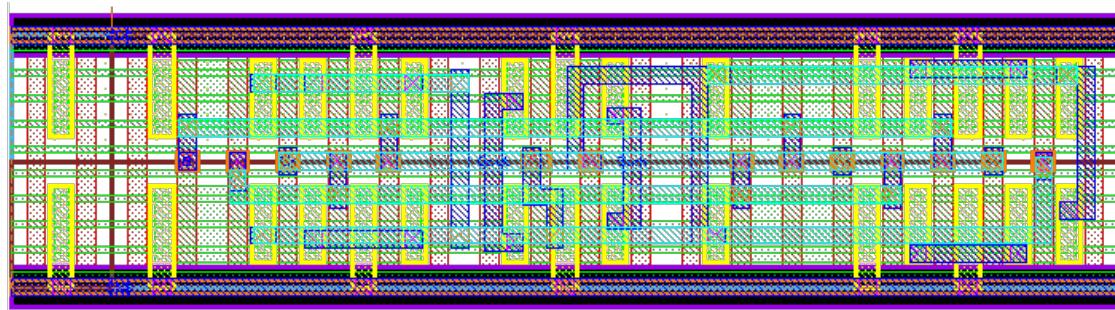
Source: From the author.

For area penalties there was 136%, 188%, 100% and 213% increase for the CMOS, TGA, TFA and Hybrid Full Adders, respectively. Their respective areas are shown in Table 5.5. Such high area penalties are mainly due to technology rules such as the 108nm well-spacing and the necessity to use TAP-Cells to explicitly connect the transistors back-gates to specific parts of the circuits or the supply/ground making the ST cell more prominent than expected. The FA layouts are shown from Figure 5.7 to 5.10.

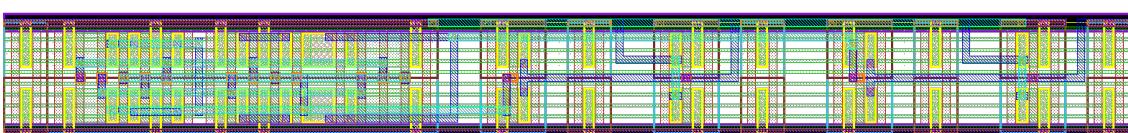
Table 5.5: Full Adders areas and respective technique area impact.

Full Adder	# of Transistors	Area (μm^2)	Ratio
CMOS	28	0.32	
CMOS ST	32	0.76	2.36
TGA	20	0.50	
TGA ST	28	1.43	2.88
TFA	16	0.44	
TFA ST	20	0.87	2.00
HYBRID	26	0.47	
HYBRID ST	34	1.46	3.13

Figure 5.7: Mirror CMOS Full Adder layouts (The cells have the same height, although the scaling is not maintained).



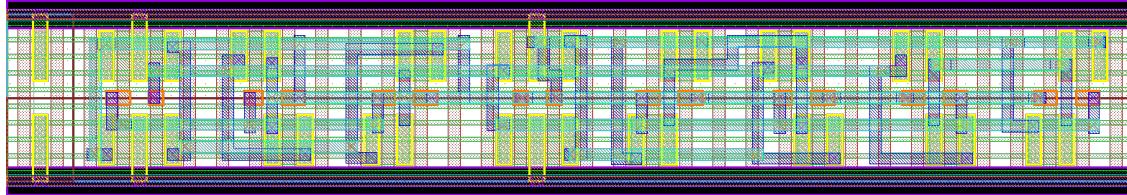
(a) Original Mirror CMOS Full Adder layout.



(b) Mirror CMOS Full Adder layout with the applied technique.

Source: From the author.

Figure 5.8: TGA Full Adder layouts (The cells have the same height, although the scaling is not maintained).



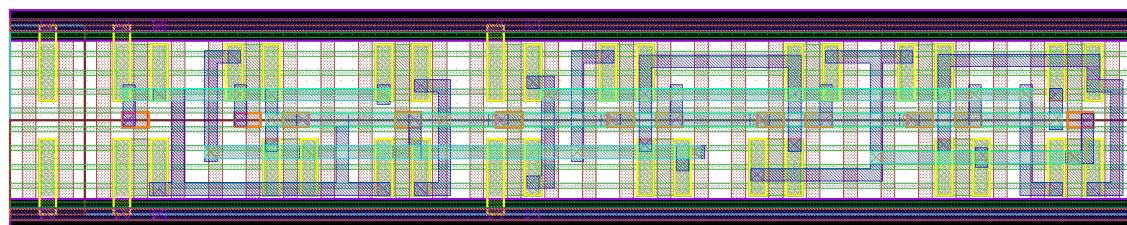
(a) Original TGA Full Adder layout.



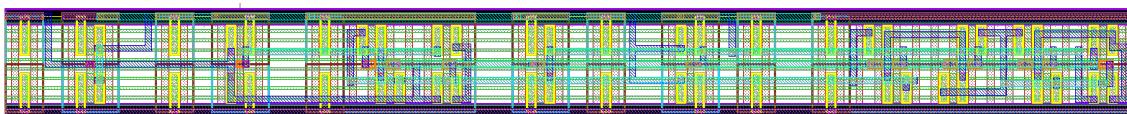
(b) TGA Full Adder layout with the applied technique.

Source: From the author.

Figure 5.9: TFA Full Adder layouts (The cells have the same height, although the scaling is not maintained).



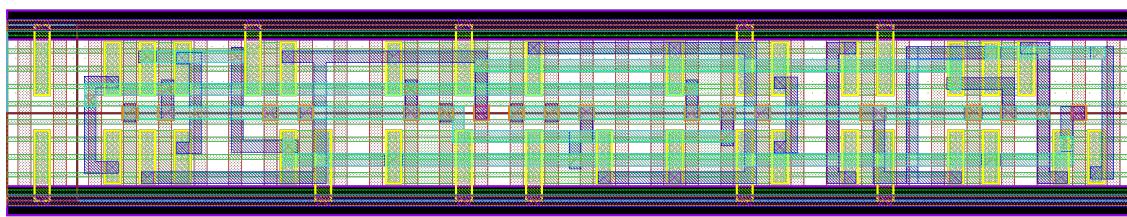
(a) Original TFA Full Adder layout.



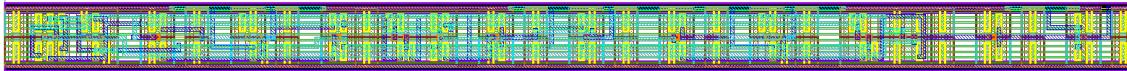
(b) TFA Full Adder layout with the applied technique.

Source: From the author.

Figure 5.10: Hybrid Full Adder layouts (The cells have the same height, although the scaling is not maintained).



(a) Original Hybrid Full Adder layout.



(b) Hybrid Full Adder layout with the applied technique.

Source: From the author.

6 CONCLUSIONS

Variability has been a critical challenge in emerging technology nodes because it can deviate from the correct circuit's behavior and affects the manufacturing yield. All current work in developing and validating techniques have been done at electrical and transistor level. There is a need for novel techniques which to improve variability robustness at the layout level.

Given that, a novel technique was tested. The method consists of replacing internal inverters with Schmitt Trigger inverters to increase the circuit's noise-immunity. The ST technique presents considerable robustness improvements over all full adders. For nominal voltage and near-threshold operation, TFA and Hybrid adders showed the highest accumulated improvements, respectively. As results show, the technique improves, sometimes drastically, the energy variability robustness for each Full Adder considered. For delay robustness, in some cases, there was a worsening in robustness mainly caused by area penalty and the pass-transistor logic.

Resuming, considering average variability robustness improvements with no worsenings, the Hybrid FA showed the best results for nominal voltage operation (17.64%) and near-threshold operation (30.47%). Considering only delay robustness there is no definitive best case at nominal voltage operation given that there was no considerable improvement at CMOS and Hybrid FAs and there was considerable worsening over one of the inputs at TGA and TFA. At near-threshold level the Hybrid FA brings the best average delay improvement (16.45%). Considering only energy robustness improvements, the Hybrid FA showed the best average improvement (33.56%) at nominal voltage operation. At near-threshold level, the TFA showed the best energy robustness improvement (61.88%). An overview is shown at Table 6.1.

Table 6.1: General most and less sensible Full Adder over variability

	Nominal	NT
Highest Accumulated Robustness Improvement	Hybrid (70%)	Hybrid (122%)
Highest Accumulated Robustness Improvement	TGA (39.15%)	CMOS (62.38%)
Lowest Variability Sensitivity without the ST technique	Delay	CMOS (22.46%)
	Energy	CMOS (20%)
Lowest Variability Sensitivity with the ST technique	Delay	CMOS (21.82%)
	Energy	Hybrid (15.6%)
Highest Variability Sensitivity without the ST technique	Delay	TFA (68.27%)
	Energy	TGA (25.33%)
Highest Variability Sensitivity with the ST technique	Delay	TFA (67.18%)
	Energy	TGA (20.16%)
		CMOS (22%)

Considering penalties, the FA that suffered less penalty, at nominal voltage level, was the TGA, with 26% increase on delays and 14% increase in absolute delay deviations. At near-threshold level, the TFA showed improvements, with a 7% decrease on delays and 17% decrease on absolute deviations. Those improvements are due to the pass-transistor logic present on the TFA in a way that the extra path to supply/ground, comparing a inverter with the ST, aids the signal restoring. Alongside that, the TFA was the FA that presented the lowest area penalty. For energy penalties, the CMOS showed the lowest penalties, with 52% increase in energy consumption and 24% increase in absolute deviations. For near-threshold operation, the CMOS Adder shows again the lowest increase in energy consumption with the TFA showing a 10% decrease in energy absolute deviation. A penalty overview is shown at Table 6.2.

Table 6.2: General technique penalty.

(%)	Metrics	Nominal	NT
Area			TFA (100%)
Average Lowest Penalty	Delay	TGA (19.63%)	TFA (-11.35%)
	Energy	CMOS (38%)	HYBRID (38.45%)
Area			Hybrid (213%)
Average Highest Penalty	Delay	TFA (46.71%)	TGA (61%)
	Energy	TFA (95.17%)	TFA (56.18%)

With the technique penalties in mind, it should only be utilized in applications that can bear the delays, energy consumption and area increase with variability robustness as a priority. These works demonstrate the need for new techniques at layout level to address variability for high performance/low power applications with low area penalties. It is

important to note that, according to the state-of-art research, this is the first analysis of this technique made at layout level. For future works, a supply voltage calibration shall be made to find the best cost-benefit supply voltage.

6.1 Future Works

As future works it is proposed: a near-threshold voltage calibration to find the best cost-benefit supply voltage, to explore different full adder topologies and investigate other techniques to mitigate the impact of process variability.

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**ANNEX A — EXEMPLO DE ARQUIVO UTILIZADO NA SIMULAÇÃO
ELÉTRICA SEM A TÉCNICA ST**

```
* test file for extracted cmos full adder layout with asap7
finfet tech
.include "CMOSFA.pex.netlist"
.include "/home/ic/leonardo.moraes/Desktop/FAEXT/hspice/7
nm_TT.pm"

*.OPTION POST = 2
.define gauss(nom, rvar, sig) (nom + (nom*rvar)/sig *
sgauss(0))

.param VCC = 0.7

.param p_phig = gauss(4.8108, 0.05, 3)
.param n_phig = gauss(4.3720, 0.05, 3)

VCIN CIN GND PWL (0n 0 18n 0)

VA1 A1 GND PWL (0n VCC 18n VCC)
VA2 A2 GND PWL (0n VCC 18n VCC)
VA4 A4 GND PWL (0n 0 18n 0)
VA5 A5 GND PWL (0n 0 18n 0)

VB2 B2 GND PWL (0n 0 18n 0)
VB4 B4 GND PWL (0n 0 18n 0)
VB5 B5 GND PWL (0n 0 18n 0)

VA3 A3 GND PWL (0n 0 3n 0 3.01n VCC 6n VCC 6.01n 0 7n 0
7.01n VCC 8n VCC 8.01n 0 10n 0 10.01n VCC 11n VCC 11.01n
0 15n 0 15.01n VCC 18n VCC)
VB3 B3 GND PWL (0n 0 3n 0 3.01n VCC 6n VCC 6.01n 0 9n 0
9.01n VCC 12n VCC 12.01n 0 13n 0 13.01n VCC 14n VCC
```

```

14.01n 0 16n 0 16.01n VCC 17n VCC 17.01n 0 18n 0)
VB1 B1 GND PWL (0n 0 1n 0 1.01n VCC 2n VCC 2.01n 0 3n 0 4n
0 4.01n VCC 5n VCC 5.01n 0 6n 0 9n 0 9.01n VCC 10n VCC
12n VCC 12.01n 0 13n 0 15n 0 15.01n VCC 16n VCC 18n VCC)

VVDD0 VDD0 GND VCC
VVDD1 VDD1 GND VCC
VGND GND GND 0

XCMOSFA1 GND VDD0 B1 A1 CIN    COUT1 SUM1 CMOSFA
XCMOSFA2 GND VDD0 B2 A2 COUT1 COUT2 SUM2 CMOSFA
XCMOSFA3 GND VDD1 B3 A3 COUT2 COUT3 SUM3 CMOSFA
XCMOSFA4 GND VDD0 B4 A4 COUT3 COUT4 SUM4 CMOSFA
XCMOSFA5 GND VDD0 B5 A5 COUT4 COUT5 SUM5 CMOSFA

.tran 1p 18n sweep Monte = 2000

*---Atrasos de Propagacao---
.measure tran TP_LH_Cin_0_1 trig v(COUT2) val=0.35 rise
=1 targ v(SUM3) val=0.35 rise=1
.measure tran TP_HL_Cin_0_1 trig v(COUT2) val=0.35 fall
=1 targ v(SUM3) val=0.35 fall=1
.measure tran TP_LH_Cin_1_0 trig v(COUT2) val=0.35 rise
=2 targ v(SUM3) val=0.35 rise=2
.measure tran TP_HL_Cin_1_0 trig v(COUT2) val=0.35 fall
=2 targ v(SUM3) val=0.35 fall=2

.measure tran TP_LH_0_A_1 trig v(A3) val=0.35 rise=2
targ v(SUM3) val=0.35 rise=3
.measure tran TP_HL_0_A_1 trig v(A3) val=0.35 fall=2
targ v(SUM3) val=0.35 fall=3
.measure tran TP_LH_1_A_0 trig v(A3) val=0.35 rise=3

```

```
targ v(SUM3) val=0.35 rise=5
.measure tran TP_HL_1_A_0 trig v(A3) val=0.35 fall=3
targ v(SUM3) val=0.35 fall=5

.measure tran TP_LH_0_1_B trig v(B3) val=0.35 rise=3
targ v(SUM3) val=0.35 rise=7
.measure tran TP_HL_0_1_B trig v(B3) val=0.35 fall=3
targ v(SUM3) val=0.35 fall=7
.measure tran TP_LH_1_0_B trig v(B3) val=0.35 rise=4
targ v(SUM3) val=0.35 rise=9
.measure tran TP_HL_1_0_B trig v(B3) val=0.35 fall=4
targ v(SUM3) val=0.35 fall=9

*---Medidas de energia---
.measure tran energy integ i(VVDD1) from=0n to=18n

.end
```

**ANNEX B — EXEMPLO DE ARQUIVO UTILIZADO NA SIMULAÇÃO
ELÉTRICA COM A TÉCNICA ST**

```
* test file for extracted cmos full adder layout with asap7
finfet tech

.include "CMOSFAST.pex.netlist"
.include "/home/ic/leonardo.moraes/Desktop/FAEXT/hspice/7
nm_TT.pm"

*.OPTION POST = 2
.define gauss(nom, rvar, sig) (nom + (nom*rvar)/sig *
sgauss(0))

.param VCC = 0.7

.param p_phig = gauss(4.8108, 0.05, 3)
.param n_phig = gauss(4.3720, 0.05, 3)

VCIN CIN GND PWL (0n 0 18n 0)

VA1 A1 GND PWL (0n VCC 18n VCC)
VA2 A2 GND PWL (0n VCC 18n VCC)
VA4 A4 GND PWL (0n 0 18n 0)
VA5 A5 GND PWL (0n 0 18n 0)

VB2 B2 GND PWL (0n 0 18n 0)
VB4 B4 GND PWL (0n 0 18n 0)
VB5 B5 GND PWL (0n 0 18n 0)

VA3 A3 GND PWL (0n 0 3n 0 3.01n VCC 6n VCC 6.01n 0 7n 0
7.01n VCC 8n VCC 8.01n 0 10n 0 10.01n VCC 11n VCC 11.01n
0 15n 0 15.01n VCC 18n VCC)
VB3 B3 GND PWL (0n 0 3n 0 3.01n VCC 6n VCC 6.01n 0 9n 0
9.01n VCC 12n VCC 12.01n 0 13n 0 13.01n VCC 14n VCC
```

```

14.01n 0 16n 0 16.01n VCC 17n VCC 17.01n 0 18n 0)
VB1 B1 GND PWL (0n 0 1n 0 1.01n VCC 2n VCC 2.01n 0 3n 0 4n
0 4.01n VCC 5n VCC 5.01n 0 6n 0 9n 0 9.01n VCC 10n VCC
12n VCC 12.01n 0 13n 0 15n 0 15.01n VCC 16n VCC 18n VCC)

VVDD0 VDD0 GND VCC
VVDD1 VDD1 GND VCC
VGND GND GND 0

XCMOSFAST1 GND VDD0 B1 A1 CIN    COUT1 SUM1 CMOSFAST
XCMOSFAST2 GND VDD0 B2 A2 COUT1 COUT2 SUM2 CMOSFAST
XCMOSFAST3 GND VDD1 B3 A3 COUT2 COUT3 SUM3 CMOSFAST
XCMOSFAST4 GND VDD0 B4 A4 COUT3 COUT4 SUM4 CMOSFAST
XCMOSFAST5 GND VDD0 B5 A5 COUT4 COUT5 SUM5 CMOSFAST

.tran 1p 18n sweep Monte = 2000

*---Atrasos de Propagacao---
.measure tran TP_LH_Cin_0_1 trig v(COUT2) val=0.35 rise
=1 targ v(SUM3) val=0.35 rise=1

.measure tran TP_HL_Cin_0_1 trig v(COUT2) val=0.35 fall
=1 targ v(SUM3) val=0.35 fall=1

.measure tran TP_LH_Cin_1_0 trig v(COUT2) val=0.35 rise
=2 targ v(SUM3) val=0.35 rise=2

.measure tran TP_HL_Cin_1_0 trig v(COUT2) val=0.35 fall
=2 targ v(SUM3) val=0.35 fall=2

.measure tran TP_LH_0_A_1 trig v(A3) val=0.35 rise=2
targ v(SUM3) val=0.35 rise=3

```

```
.measure tran TP_HL_0_A_1 trig v(A3) val=0.35 fall=2
targ v(SUM3) val=0.35 fall=3

.measure tran TP_LH_1_A_0 trig v(A3) val=0.35 rise=3
targ v(SUM3) val=0.35 rise=5

.measure tran TP_HL_1_A_0 trig v(A3) val=0.35 fall=3
targ v(SUM3) val=0.35 fall=5

.measure tran TP_LH_0_1_B trig v(B3) val=0.35 rise=3
targ v(SUM3) val=0.35 rise=7

.measure tran TP_HL_0_1_B trig v(B3) val=0.35 fall=3
targ v(SUM3) val=0.35 fall=7

.measure tran TP_LH_1_0_B trig v(B3) val=0.35 rise=4
targ v(SUM3) val=0.35 rise=9

.measure tran TP_HL_1_0_B trig v(B3) val=0.35 fall=4
targ v(SUM3) val=0.35 fall=9

*---Medidas de energia---
.measure tran energy integ i(VVDD1) from=0n to=18n

.end
```

Evaluation of Variability using Schmitt Trigger on Full Adders Layout

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Abstract. The aggressive technology and voltage scaling which modern digital circuits are facing introduces a higher influence in metrics due to variability. To mitigate that, novel techniques are proposed and tested. This work aims to analyze the impact on variability robustness of a novel technique of Schmitt Trigger-based replacement of full adders internal inverters. Several works points that the given technique helps improve the variability robustness, although, at the electrical level. Therefore, analysis will be performed at layout level using the 28nm library from STMicroelectronics and applied on four full adder designs. Performance, power and area will be taken into account.

1. Introduction

The technology scaling over the years have significantly increased the density of transistors present on chips. Alongside, with the advance over transistor technology, new challenges were introduced due to the scale down, as aging effects, high power consumption due to leakage current and an increase in the sensibility to transient faults due to radiation and process variability [Abbas et al. 2015].

The same technology scaling that allowed the increase in transistor density also allowed a voltage scaling due to the shortening of gate dimensions, internal capacitances and resistances. These two combined events contributed to the emergence, growth and current dominance of mobile applications over its counterpart. This new context, introduced a concern for battery lifespan which these applications are dependent [Islam et al. 2010].

The ascending number of mobile applications that depends on highly sophisticated processing schemes with a limited power-supply capability of today's batteries brings conflicting needs. The need to explore high-performance designs and implementations to meet the speed constraints for real-time applications and, simultaneously, consider low-power design approaches to extend the battery life of portable devices [Shoarinejad et al. 2003].

Due to the new power consumption concern, novel types of logic blocks for chips started being designed for low power. One of the most present logic blocks in computer systems is the Full Adder. It plays a central role in performing general arithmetic operations such as addition, subtraction, division, shift and so on. The full adder operation

adds two bits considering the Carry Out value from a less significant stage. It follows the equations 1 and 2 with the Truth Table 1.

$$Sum = (A \oplus B) \oplus Cin \quad (1)$$

$$Cout = (A \wedge B) \vee Cin \wedge (A \oplus B) \quad (2)$$

Table 1. Truth Table of Full Adders

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Adder cells define the throughput and are employed in the processor's executive, floating-point, and memory address generation units. Due to its absolute numbers in microprocessors and their part on the critical path of electronic systems, any improvements over adding blocks generates a considerable improvement in the whole system because of the huge influence of power, timing and area characteristics on the system design [Shoarinejad et al. 2003].

Moore's law predicts that the number of transistors per square on integrated circuits will double every year and it has been guiding the industry trending for decades. However, continue with scaling in the bulk CMOS technology has been no straightforward task. At deep nanotechnology nodes, each chip may show different behavior due to process variations during the manufacturing steps. Variations that influence the circuits metrics such as performance and power consumption, hastening the circuit degradation and making it deviate from its correct operation [Abbas et al. 2015] [Nassif 2008].

In this context, this work employs a technique using Schmitt Trigger (ST) inverters for process variability mitigation on different Full Adder topologies with priority on power consumption variations. Performance, power, and area penalty will be analyzed alongside variability robustness.

Promising new commercial technologies based on the FD-SOI (Full Depleted Silicon On Insulator) devices have been introduced to maintain the technology scaling. The process variability impact on those technologies have shown to be less present, although it can not be ignored, being necessary more research concerning the characterization of process variability effect on emerging technologies.

FD-SOI technology consists of a planar process technology with two primary innovations in comparison to the standard bulk-CMOS. First, an ultra-thin layer of buried oxide is positioned on top of the base silicon reducing the parasitic capacitance between

the source and drain and confining the charge carriers in the channel itself significantly reducing performance and power degrading leakage currents. Secondly, a very thin silicon film implements the transistor channel. The silicon film is so thin, it does not require doping the channel, resulting in a fully depleted device [Karel et al. 2016], as shown in Figure 1. These two characteristics introduce some advantages as better control of short channel effects, a decrease of junction capacitance (alongside an improved isolation of neighboring devices), better mobility due to the undoped channel and better threshold voltage (V_t) variability in comparison to previous bulk MOSFET technology. [Federspiel et al. 2012] [Weber et al. 2008]

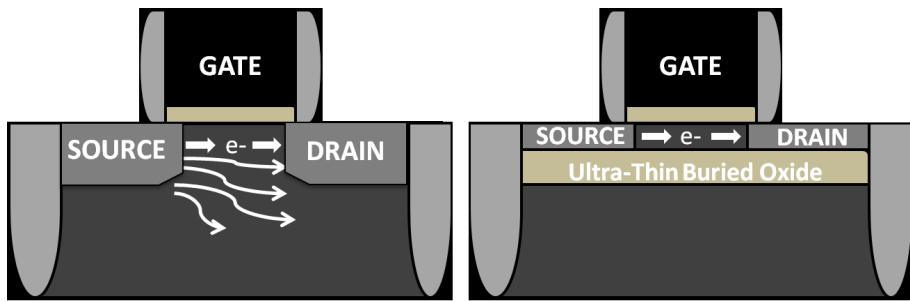


Figure 1. Comparison between Bulk CMOS (left) and FD-SOI (right) transistors.
[Karel et al. 2016]

This work is divided into six further sections: Variability Effects and Mitigation Techniques, with a theoretical foundation about variability. Motivation and Objectives, explaining in more details this work's objective. Methodology, presenting how results will be achieved with its experimental setup. Schedule, giving a prospect about next semester plans on future work.

2. Variability Effects and Mitigation Techniques

Standard CMOS devices have been optimized for high-speed and low-power consumption through its lifetime is the backbone of almost all modern digital circuits. The periodic process of technology scaling has resulted in faster and more energy efficient transistor than the previous generation. As channel lengths shrank below 50nm, the ratio of device size to atom-size becomes smaller, hence, a variable structure at the atomic scale has an increased effect on device behavior. There have been advances to reduce the loss of precision due to the manufacturing process. However, the intrinsic quantum-mechanical limitations cannot be overcome, with their impact increasing as the technology shrinks further.

Variability can occur in both spatial and temporal domains with deterministic and stochastic fluctuations [Walker et al. 2010]. In summary, variability consists of deviation of characteristics, internal or external, to the circuit, which can determine its operational features such as power and delay. These characteristics, or factors, as we will address them for the rest of this work, can be divided into three types:

Environmental Factors: Caused by temperature fluctuations and voltage drops. Voltage drops occurs due to abrupt changes in the switching activity, causing large current transients in the system, which can occur locally as well globally across the die [Nassif 2008].

Reliability Factors: Related to the aging process of the circuit, it is introduced by negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), electromigration, time dependent dielectric breakdown, gate oxide integrity, thermal cycling and hot carrier injection [Nassif 2008].

Physical Factors: It is related to variations caused by the manufacturing process, which results in deviations in the electrical parameters defining the behavior of active and passive devices. Those variations can be divided in three types of mechanisms: Systematic, they repeat over many chips or wafers. Design dependent, being particular to each circuit design. And Random, which depends on the random aspects of process manufacturing, as shown in Figure 2 [Nassif 2008].

Additionally, the technology scaling and manufacturing tolerances are not correspondingly moving side by side. For instance, the pace at which the effective channel length is reduced is faster than the improvement of mask fabrication error and mask overlay control [Nassif 2008] [Aghababa et al. 2009].

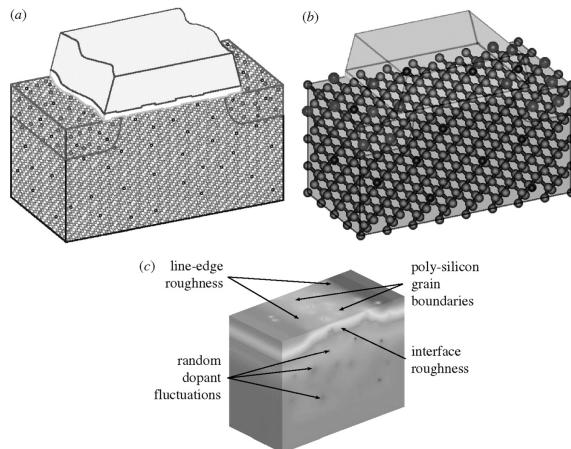


Figure 2. Transistor Variability [Walker et al. 2010]

These three types of variabilities, in conjunction, may prevent circuits from meeting their performance and power goals. Table 2 demonstrates the design impact of performance and power due to different types of variability.

Table 2. Design impact on performance and power due to different types of variability [Rahimi et al. 2016]

Property	Ease of measuring	Variability	Effects of Variability	Effect of missing specification
Performance	Medium	Medium: up to 60%	L, W, R, C, V _{th} , μ	Slower product, yield, timing error
Leakage Power	Easy	Large: up to 148%	L, V _{th} , μ , tox	Shorter battery life, yield, heat
Dynamic Power	Difficult	Workload dependent	C, α	Shorter battery life, heat

At circuit level there is multiple techniques to predict and prevent errors: Tuning CMOS knobs, circuit topology optimizations, self-timed circuits, temporal and logical error masking, relaxed retiming and graceful degradation, and inexact circuits. Although, there are few approaches to decrease the process variability at its core. It is due to the technology dependency present in this problem [Rahimi et al. 2016].

It can be observed that many works try to indicate the most robust design for a given type of circuit. For example, in [Dokania et al. 2013] twelve different Full Adder topologies are analyzed considering delay, power and Power-Delay-Product (PDP) variability. It is used a 16nm bulk CMOS technology node in SPICE simulations with Process, Voltage and Temperature (PVT) variability being considered and Monte Carlo simulations performed. The authors concluded that Cell A, CLRCL and Cell B full adders presented the best results for all three metrics (Delay, Power and PDP).

In [Ames et al. 2016] the effects of PVT variability in different full adder designs are investigated. The simulations are performed in HSPICE with the bulk CMOS 32nm node technology. With TGA and TFA architectures showing acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested full adders - 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) Full Adder.

In [Islam and Hasan 2011] various popular 1-bit digital summing circuits functionality and robustness are analyzed in light of PVT variations with the best full adder being simulated in CNFET technology for comparison with the bulk CMOS version. The simulations are carried at the 22nm bulk CMOS and CNFET technology node in HSPICE. Its results show that the TGA has the strongest PVT variability robustness and its CNFET version provides over 3x, 1.14x and 1.1x less propagation delay, power dissipation and energy delay product (EDP) variations, respectively. This work does not consider the total power consumption of each full adder separately.

Some articles analyze the adoption of new technologies: [Guduri and Islam 2015] proposes a hybrid of bulk CMOS and CNFET (Carbon Nanotube Field Effect Transistor) Full Adder at 16nm in deep subthreshold operation region for ultralow-power applications simulated in SPICE which showed some improvement over its bulk CMOS Full Adder counterpart achieving 5% and 1% improvement in power, power-delay and energy-delay products and their variability, respectively.

In [Islam et al. 2011] a new subthreshold-FinFET (Fin Field-Effect Transistor) Full Adder is proposed and compared over multiple full adders showing huge metric improvements provided by the FinFET technology up to 2.22x improvement in power variability. It was simulated in 32nm predictive technology model on HSPICE.

It is notable that none of these works consider a layout approach for its simulations and do not address any novel general technique which can be applied to a range of different types of circuits. Although, some works introduce novel designs.

[Federspiel et al. 2012] presents reliability comparison between 28nm bulk CMOS and FDSOI technologies at layout level, with FDSOI showing 32% improved performance, 40% reduced power consumption and improved matching, with its intrinsic reliability behavior similar to 28nm bulk at the device level. [Alioto and Palumbo 2007] presents a study about the delay variability caused by supply variations in the Transmission Gate Full Adder (TGA). The experiments were performed at 90nm and 180nm bulk CMOS Technology in Spectre at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TG FA presenting worse results 15% (25%) for the 90 nm (180 nm) in comparison to static logic.

Some works focus on evaluating techniques: In [Zimpeck et al. 2016] three di-

mensioning methods are applied on multiple circuits and their impact on variability robustness is analyzed. The simulations were performed considering a 14nm FinFET technology using HSPICE tool. The authors concluded that the Optimized Transistor Sizing (OTS) technique has the best ratio between nominal PDP and PDP under process variability.

[Ahmadi et al. 2017] introduces a new technique to improve the performance of digital circuits in the presence of variations. It consists of a hybrid of two former methods to prevent errors due to delay variations. The simulations were performed with a 45nm predictive technology using HSPICE and applied on ITC'99 and ISCAS'89 benchmarks circuits. The results show that this hybrid technique can tolerate process variations up to 27.3% better than state-of-the-art techniques.

Among these works there is [Dokania and Islam 2015] on which a novel technique based on the replacement of Full Adder's internal inverters with low voltage Schmitt Triggers for PVT variability robustness improvement is originally introduced and applied on seven different full adder designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in PDP. Although, the improvements occur at the cost of an increase in the area and power dissipation of each design.

Schmitt triggers are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. On a typical input (non-Schmitt trigger), its binary value will switch at the same point on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit causing a shift in the threshold voltage.

If the threshold shifts, it will cross the input causing it to switch again. It can go indefinitely causing oscillation. The same thing can happen if there is noise on the input. Schmitt Triggers are applied in these cases to filter noise introducing superior and inferior threshold voltages, as shown in Figure 3.c. The difference between the thresholds is called Hysteresis [Cockrill 2011], its curve is shown at 3.a. According to the Schmitt Trigger behavior, it can mitigate the influence of variations in the inputs product of PVT variability. In figure 3.c is shown a classical CMOS Schmitt Trigger design.

This technique is tested in several works: In [Ahmad et al. 2016] it is presented a novel Schmitt-trigger-based single-ended 11T SRAM cell. It analyses its performance against seven different SRAM topologies. The novel cell showed the least energy consumption per operation with the smallest leakage power and a 6.9x higher Ion/Ioff ratio. Further PVT variability simulations confirmed the robustness of the design regarding read and write operation. The simulations were carried in 22nm predictive technology using HSPICE.

[Moghaddam et al. 2017] presents a Schmitt trigger (ST) buffer using carbon nanotube FET (CNTFET). It was evaluated against other two buffers and showed, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain considering PVT variability robustness. The simulations were carried in 16nm Stanford CNTFET model using HSPICE.

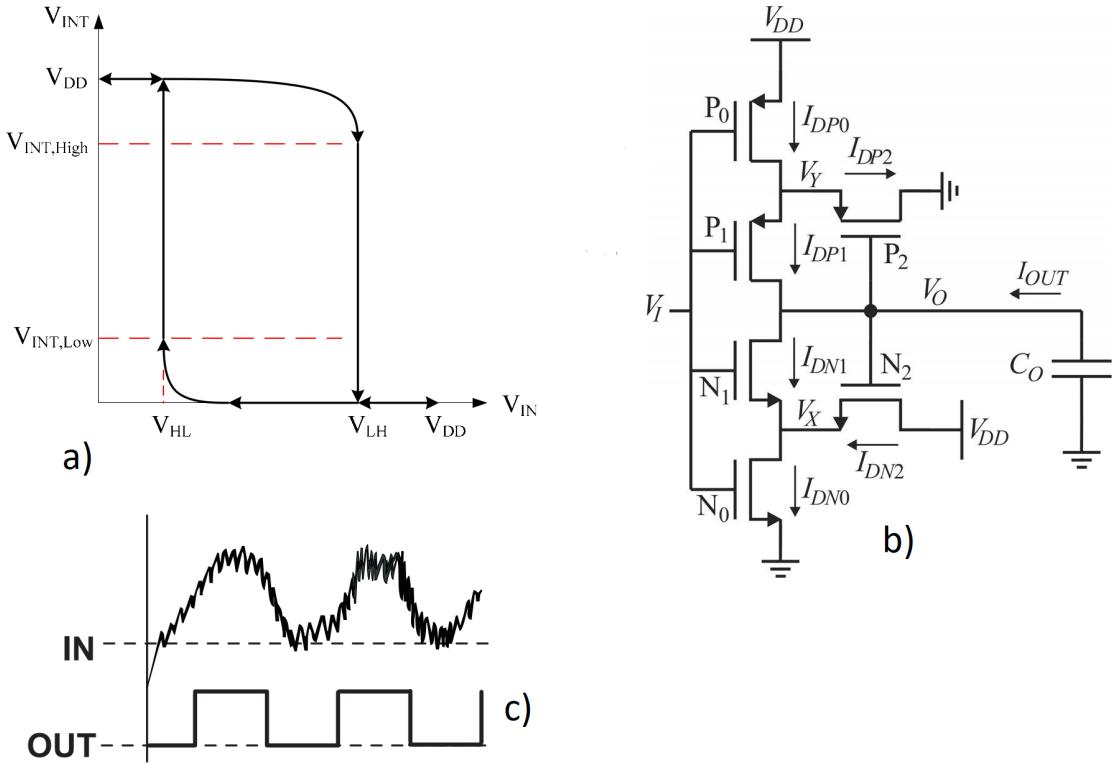


Figure 3. a) General Schmitt Trigger's hysteresis curve b) Classical CMOS Schmitt Trigger Topology c) Typical signal filtering with Schmitt Trigger [Cockrill 2011].

Alongside, in [Toledo et al. 2016] the ST technique is applied on four Full Adders. It presented promising results regarding the power deviation due to the process variability with a decrease up to 79% with a drawback of a significant increase in average energy consumption. The simulations were performed with the 16nm technology predictive technology model in NGSPICE.

3. Motivation and Objectives

Reviewing the works which have explored ST technique, it is evident that there is a lack of tests on layout level. These works have demonstrated the technique strengths at electrical level, with the circuits tested showing improved PVT variability robustness characteristics. Although, it is essential to shed light on multiple levels of abstraction simulation to give a more precise notion of the technique efficiency. Given that, the main goal of this work is to apply on four different full adder topologies at layout level designed on the 28nm FD-SOI technology the technique introduced at [Dokania and Islam 2015] of changing traditional inverters by Schmitt Triggers Inverters to mitigate variability effects, to measure the impact of such technique on power, timing and area.

4. Methodology

For the experiments, there will be considered four different types of Full Adders topologies to evaluate their robustness to process variability with their internal inverters replaced by Schmitt Triggers. The Full Adders listed below have been chosen due to

their promising results in related works [Ames et al. 2016] [Dokania and Islam 2015] [Dokania et al. 2013]:

1. Complementary MOSFET Adder (CMOS)
2. Transmission Gate Adder (TGA)
3. Transmission Function Adder (TFA)
4. Hybrid Full Adder

The CMOS Full Adder is considered the most traditional Full Adder topology containing 28 Transistors arranged in a pull-up and pull-down networks, which are logically complementary. It has a full voltage swing and buffered Sum and Cout signal and the advantages of good conductibility and robustness when working with novel technologies and low voltages. However, it has high capacitance because each input is connected to the gate of at least a PMOS and NMOS device additionally, it shows the impact of the pull-up network that makes the circuit slower due to the low mobility of its holes [Beckett 2002] [Devadas and Kishore 2017] [Islam and Hasan 2011].

Transmission Gate Full Adder [Weste and Eshraghian 1985] contains 16 transistors, and is a high speed and low power design. However, shows low driving capability which may be unacceptable in some cases where there is a long chain of full adders due to the increase in delay [Islam and Hasan 2011]. The Transmission Function Adder is based on transmission gates as well, containing 20 transistors, working satisfactorily with low voltages but losing performance when cascaded due to the lack of supply/ground contacts and, consequently, driving capability [Navi et al. 2009]. Both TFA and TGA generate the XOR function ($H = A \text{ XOR } B$) followed by an inverter which produces the XNOR function (H'). H and H' are used to control the transmission gates generating the Sum and Cout outputs. The inverter generates delay between H and H' , which will cause the transmission gates to behave as pass transistors, that may introduce glitches and consequently, increase the power consumption of these cells. Additionally, TGA contains three inverters, one more than TFA. The inverters switching introduce more short-circuit power [Shams and Bayoumi 2000].

Inspired by CMOS and CPL Full Adders architectures, the Hybrid Full Adder [Navi et al. 2009] contains 26 transistors, with the main advantage of a high output signal and low power properties. Although, the design shows high input capacitance for specific input vectors.

A variety of CMOS Schmitt Trigger designs have been proposed and implemented over the years, with the conventional 6T-CMOS Schmitt Trigger proposed in [Doki 1984] exhibiting the wanted characteristics of different high-to-low and low-to-high transition threshold voltages, giving rise to hysteresis. The ST inverter circuit used in this work was inspired by [Zhang et al. 2003] and modified in [Dokania and Islam 2015] to achieve the desired inverting characteristic, as shown in Figure 4. It is designed for operation at a supply voltage of 0.4V in order to achieve low power consumption, and consists of the junction of two inverters where the output from the second one will be the bulk for the first one.

In this design a dynamic body-bias technique is applied through a feedback mechanism to a standard CMOS inverter circuit, thus allowing a change in the threshold voltages of two MOSFETs, implying a change in the switching voltage. The Full Adder designs are shown in Figure 5.

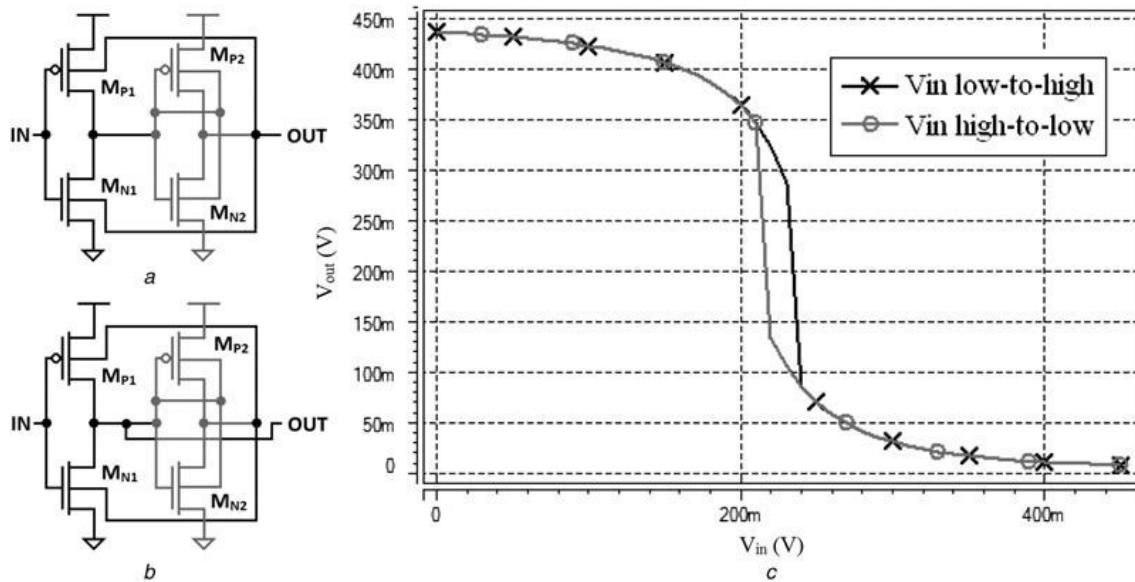


Figure 4. Original Low Power Schmitt Trigger (left above), Modified Low Power Schmitt Trigger (left below) and its hysteresis curve (right) [Dokania and Islam 2015].

All Full Adders layouts will be designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence® with the process design kit (PDK) of 28nm FD-SOI from ST Microelectronics. The simulations will be carried out in HSPICE from Synopsys Company, after the removal of parasitic capacitances from the layouts. Each full adder will be designed with and without the Schmitt Triggers replacement in order to take into account the penalties due to the adoption of the ST technique in terms of area, power consumption and performance. The process variability evaluation will be conducted by 2000 Monte Carlo simulations varying the threshold voltage of the PMOS and NMOS devices according to a Gaussian distribution.

For all experiments, it will be observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: delay, power and energy, where σ/μ represents the sensibility of the cell to process variability.

To avoid underestimating effects of realistic input waveforms on design metrics, the simulations will be carried under a 5-bit ripple carry adder using copies of the 1-bit full adder cell with design metrics being calculated for the middle cell as shown in Figure 6.

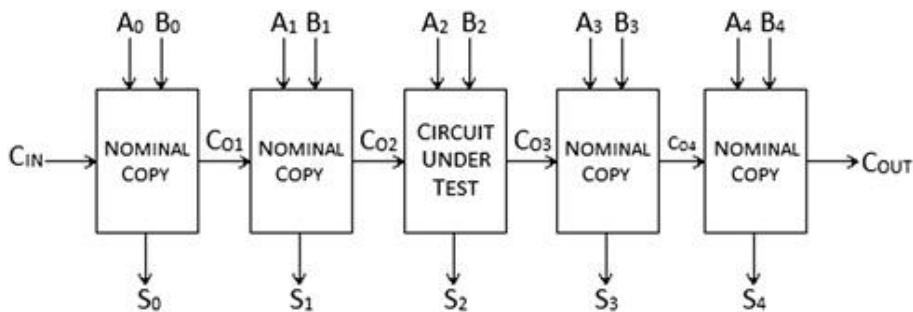


Figure 6. Test Bench [Dokania and Islam 2015].

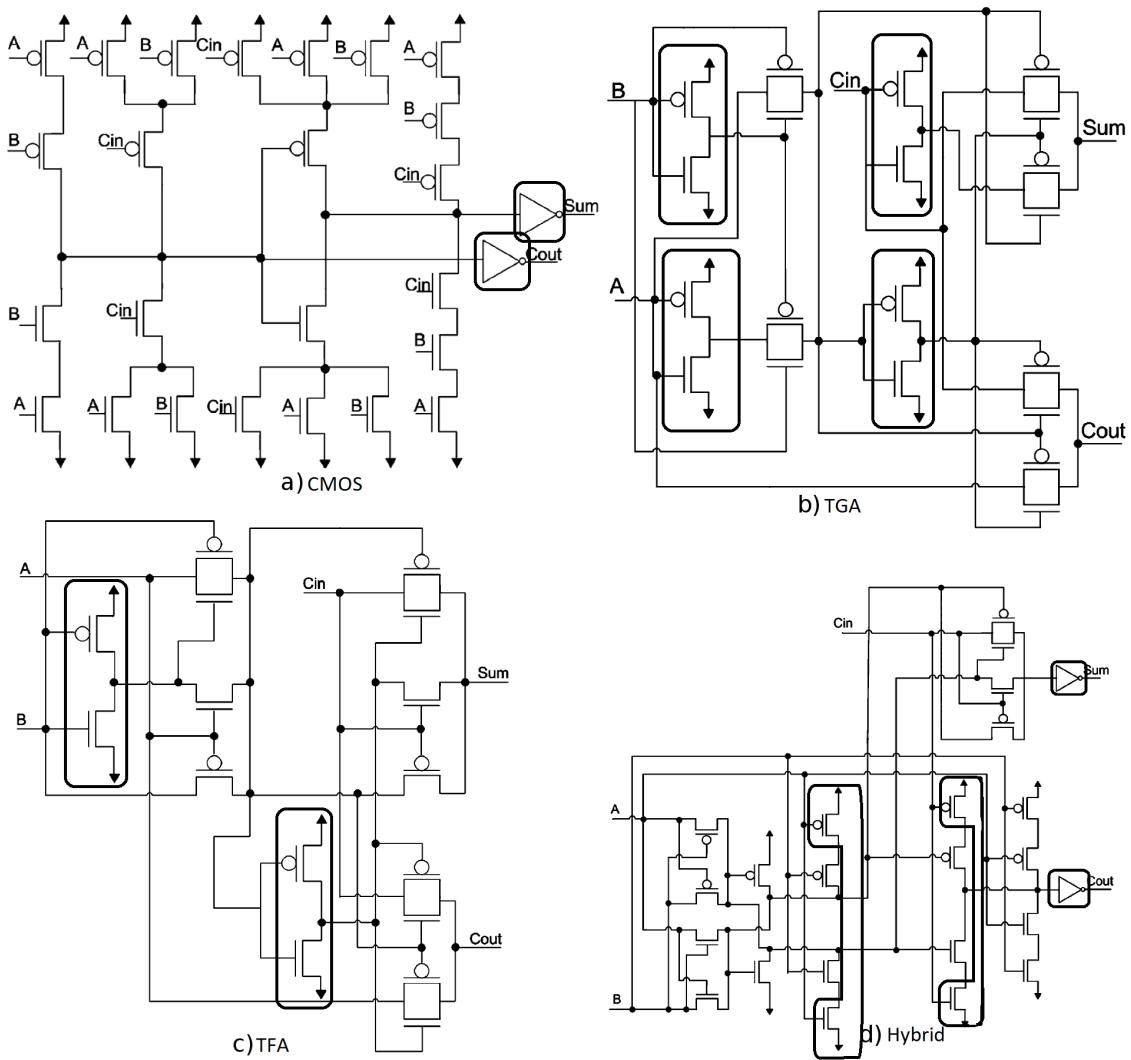


Figure 5. Full Adders with internal inverters to be replaced highlighted [Toledo et al. 2016].

5. Schedule

The reading of articles and review of the state of the art required for the development of this research were carried out from October to December of 2017. This work development will continue accordingly to the schedule presented at Table 3, being executed until the beginning of July.

Table 3. Activity Schedule for 2018

Activity	Jan	Feb	March	April	May	June	July
Familiarization with ST's PDK and dimensioning of the adder transistors	X						
Layout generation without the ST technique		X	X				
Layout generation with the ST technique			X	X			
Analysis and writing of results				X	X		
Writing of TG2 and submission of articles					X	X	X

6. Conclusions

Variability in deep submicron technology is an issue which needs addressing. It can mine any improvement made over technology generations introducing variations in the circuits behavior making it not comply with the industry needs. There are few works introducing novel techniques to mitigate variability effects at circuit level to decrease its impact in its absolute values. Instead, most of the existing techniques aim to detect errors not addressing the problem directly.

Emerging novel technologies are analyzed to compare to previously established technologies for variability robustness improvement. Overall, these technologies bring improvements in performance and power consumption, although it barely addresses the variability concern. A novel technique is introduced which consists of replacing internal inverters of full adders (extendable to other types of logic blocks) with Schmitt Triggers to filter the variations on its inputs providing a more predictable behavior.

This technique has been used and, by now, seems to be a considerable choice. Although, it has not been tested at layout level. This next level of abstraction is necessary to bring a more accurate prediction of the real influence of this technique over target specific circuits.

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