Evaluation of Variability using Schmitt Trigger on Full Adders Layout

Leonardo B. Moraes[1], Alexandra L. Zimpeck[1], Cristina Meinhardt[2], Ricardo Reis[1]

[1]Instituto de Informática – PPGC/PGMicro
Universidade Federal do Rio Grande do Sul (UFRGS) – Porto Alegre – RS – Brazil

[2]Centro de Ciências Computacionais
Universidade Federal do Rio Grande (FURG) – Rio Grande – RS – Brazil

{lbmoraes,alzimpeck,reis}@inf.ufrgs.br, cristina.meinhardt@furg.br

Abstract. *The aggressive technology and voltage scaling which modern digital circuits are facing introduces a higher influence in metrics due to variability. To mitigate that, novel techniques are proposed and tested. This work aims to analyze the impact on variability robustness of a novel technique of Schmitt Trigger-based replacement of full adders internal inverters. Several works points that the given technique helps improve the variability robustness, although, at the electrical level. Therefore, analysis will be performed at layout level using the 28nm library from STMicroelectronics and applied on four full adder designs. Performance, power and area will be taken into account.*

1. Introduction

The technology scaling over the years have significantly increased the density of transistors present on chips. Alongside, with the advance over transistor technology, new challenges were introduced due to the scale down, as aging effects, high power consumption due to leakage current and an increase in the sensibility to transient faults due to radiation and process variability [Abbas et al. 2015].

The same technology scaling that allowed the increase in transistor density also allowed a voltage scaling due to the shortening of gate dimensions, internal capacitances and resistances. These two combined events contributed to the emergence, growth and current dominance of mobile applications over its counterpart. This new context, introduced a concern for battery lifespan which these applications are dependent [Islam et al. 2010].

The ascending number of mobile applications that depends on highly sophisticated processing schemes with a limited power-supply capability of today's batteries brings conflicting needs. The need to explore high-performance designs and implementations to meet the speed constraints for real-time applications and, simultaneously, consider low-power design approaches to extend the battery life of portable devices [Shoarinejad et al. 2003].

Due to the new power consumption concern, novel types of logic blocks for chips started being designed for low power. One of the most present logic blocks in computer systems is the Full Adder. It plays a central role in performing general arithmetic operations such as addition, subtraction, division, shift and so on. The full adder operation

adds two bits considering the Carry Out value from a less significant stage. It follows the equations 1 and 2 with the Truth Table 1.

$$Sum = (A \oplus B) \oplus Cin \tag{1}$$

$$Cout = (A \wedge B) \vee Cin \wedge (A \oplus B) \tag{2}$$

Table 1. Truth Table of Full Adders

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Adder cells define the throughput and are employed in the processor's executive, floating-point, and memory address generation units. Due to its absolute numbers in microprocessors and their part on the critical path of electronic systems, any improvements over adding blocks generates a considerable improvement in the whole system because of the huge influence of power, timing and area characteristics on the system design [Shoarinejad et al. 2003].

Moore's law predicts that the number of transistors per square on integrated circuits will double every year and it has been guiding the industry trending for decades. However, continue with scaling in the bulk CMOS technology has been no straightforward task. At deep nanotechnology nodes, each chip may show different behavior due to process variations during the manufacturing steps. Variations that influence the circuits metrics such as performance and power consumption, hastening the circuit degradation and making it deviate from its correct operation [Abbas et al. 2015] [Nassif 2008].

In this context, this work employs a technique using Schmitt Trigger (ST) inverters for process variability mitigation on different Full Adder topologies with priority on power consumption variations. Performance, power, and area penalty will be analyzed alongside variability robustness.

Promising new commercial technologies based on the FD-SOI (Full Depleted Silicon On Insulator) devices have been introduced to maintain the technology scaling. The process variability impact on those technologies have shown to be less present, although it can not be ignored, being necessary more research concerning the characterization of process variability effect on emerging technologies.

FD-SOI technology consists of a planar process technology with two primary innovations in comparison to the standard bulk-CMOS. First, an ultra-thin layer of buried oxide is positioned on top of the base silicon reducing the parasitic capacitance between

the source and drain and confining the charge carriers in the channel itself significantly reducing performance and power degrading leakage currents. Secondly, a very thin silicon film implements the transistor channel. The silicon film is so thin, it does not require doping the channel, resulting in a fully depleted device [Karel et al. 2016], as shown in Figure 1. These two characteristics introduce some advantages as better control of short channel effects, a decrease of junction capacitance (alongside an improved isolation of neighboring devices), better mobility due to the undoped channel and better threshold voltage (Vt) variability in comparison to previous bulk MOSFET technology. [Federspiel et al. 2012] [Weber et al. 2008]

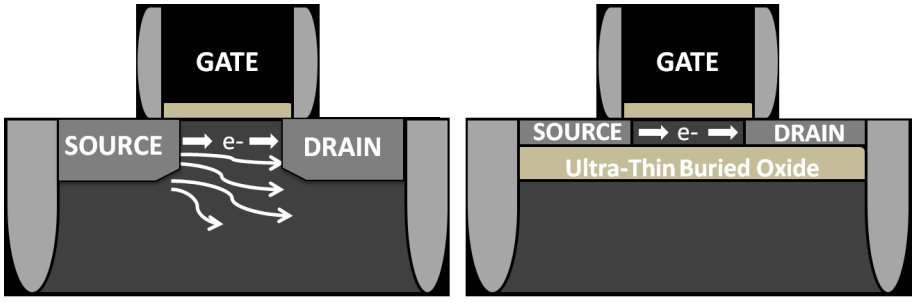

Figure 1. Comparison between Bulk CMOS (left) and FD-SOI (right) transistors. [Karel et al. 2016]

This work is divided into six further sections: Variability Effects and Mitigation Techniques, with a theoretical foundation about variability. Motivation and Objectives, explaining in more details this work's objective. Methodology, presenting how results will be achieved with its experimental setup. Schedule, giving a prospect about next semester plans on future work.

2. Variability Effects and Mitigation Techniques

Standard CMOS devices have been optimized for high-speed and low-power consumption through its lifetime is the backbone of almost all modern digital circuits. The periodic process of technology scaling has resulted in faster and more energy efficient transistor than the previous generation. As channel lengths shrank below 50nm, the ratio of device size to atom-size becomes smaller, hence, a variable structure at the atomic scale has an increased effect on device behavior. There have been advances to reduce the loss of precision due to the manufacturing process. However, the intrinsic quantum-mechanical limitations cannot be overcome, with their impact increasing as the technology shrinks further.

Variability can occur in both spatial and temporal domains with deterministic and stochastic fluctuations [Walker et al. 2010]. In summary, variability consists of deviation of characteristics, internal or external, to the circuit, which can determine its operational features such as power and delay. These characteristics, or factors, as we will address them for the rest of this work, can be divided into three types:

Environmental Factors: Caused by temperature fluctuations and voltage drops. Voltage drops occurs due to abrupt changes in the switching activity, causing large current transients in the system, which can occur locally as well globally across the die [Nassif 2008].

Reliability Factors: Related to the aging process of the circuit, it is introduced by negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), electromigration, time dependent dielectric breakdown, gate oxide integrity, thermal cycling and hot carrier injection [Nassif 2008].

Physical Factors: It is related to variations caused by the manufacturing process, which results in deviations in the electrical parameters defining the behavior of active and passive devices. Those variations can be divided in three types of mechanisms: Systematic, they repeat over many chips or wafers. Design dependent, being particular to each circuit design. And Random, which depends on the random aspects of process manufacturing, as shown in Figure 2 [Nassif 2008].

Additionally, the technology scaling and manufacturing tolerances are not correspondingly moving side by side. For instance, the pace at which the effective channel length is reduced is faster than the improvement of mask fabrication error and mask overlay control [Nassif 2008] [Aghababa et al. 2009].

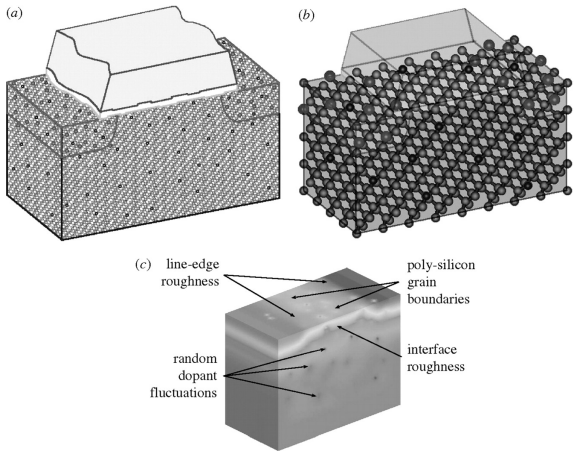

Figure 2. Transistor Variability [Walker et al. 2010]

These three types of variabilities, in conjunction, may prevent circuits from meeting their performance and power goals. Table 2 demonstrates the design impact of performance and power due to different types of variability.

Table 2. Design impact on performance and power due to different types of variability [Rahimi et al. 2016]

Property	Ease of measuring	Variability	Effects of Variability	Effect of missing specification
Performance	Medium	Medium: up to 60%	L, W, R, C, Vth, μ	Slower product, yield, timing error
Leakage Power	Easy	Large: up to 148%	L, Vth, μ, tox	Shorter battery life, yield , heat
Dynamic Power	Difficult	Workload dependent	C, α	Shorter battery life, heat

At circuit level there is multiple techniques to predict and prevent errors: Tuning CMOS knobs, circuit topology optimizations, self-timed circuits, temporal and logical error masking, relaxed retiming and graceful degradation, and inexact circuits. Although, there are few approaches to decrease the process variability at its core. It is due to the technology dependency present in this problem [Rahimi et al. 2016].

It can be observed that many works try to indicate the most robust design for a given type of circuit. For example, in [Dokania et al. 2013] twelve different Full Adder topologies are analyzed considering delay, power and Power-Delay-Product (PDP) variability. It is used a 16nm bulk CMOS technology node in SPICE simulations with Process, Voltage and Temperature (PVT) variability being considered and Monte Carlo simulations performed. The authors concluded that Cell A, CLRCL and Cell B full adders presented the best results for all three metrics (Delay, Power and PDP).

In [Ames et al. 2016] the effects of PVT variability in different full adder designs are investigated. The simulations are performed in HSPICE with the bulk CMOS 32nm node technology. With TGA and TFA architectures showing acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested full adders - 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) Full Adder.

In [Islam and Hasan 2011] various popular 1-bit digital summing circuits functionality and robustness are analyzed in light of PVT variations with the best full adder being simulated in CNFET technology for comparison with the bulk CMOS version. The simulations are carried at the 22nm bulk CMOS and CNFET technology node in HSPICE. Its results show that the TGA has the strongest PVT variability robustness and its CNFET version provides over 3x, 1.14x and 1.1x less propagation delay, power dissipation and energy delay product (EDP) variations, respectively. This work does not consider the total power consumption of each full adder separately.

Some articles analyze the adoption of new technologies: [Guduri and Islam 2015] proposes a hybrid of bulk CMOS and CNFET (Carbon Nanotube Field Effect Transistor) Full Adder at 16nm in deep subthreshold operation region for ultralow-power applications simulated in SPICE which showed some improvement over its bulk CMOS Full Adder counterpart achieving 5% and 1% improvement in power, power-delay and energy-delay products and their variability, respectively.

In [Islam et al. 2011] a new subthreshold-FinFET (Fin Field-Effect Transistor) Full Adder is proposed and compared over multiple full adders showing huge metric improvements provided by the FinFET technology up to 2.22x improvement in power variability. It was simulated in 32nm predictive technology model on HSPICE.

It is notable that none of these works consider a layout approach for its simulations and do not address any novel general technique which can be applied to a range of different types of circuits. Although, some works introduce novel designs.

[Federspiel et al. 2012] presents reliability comparison between 28nm bulk CMOS and FDSOI technologies at layout level, with FDSOI showing 32% improved performance, 40% reduced power consumption and improved matching, with its intrinsic reliability behavior similar to 28nm bulk at the device level. [Alioto and Palumbo 2007] presents a study about the delay variability caused by supply variations in the Transmission Gate Full Adder (TGA). The experiments were performed at 90nm and 180nm bulk CMOS Technology in Spectre at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TG FA presenting worse results 15% (25%) for the 90 nm (180 nm) in comparison to static logic.

Some works focus on evaluating techniques: In [Zimpeck et al. 2016] three di-

mensioning methods are applied on multiple circuits and their impact on variability robustness is analyzed. The simulations were performed considering a 14nm FinFET technology using HSPICE tool. The authors concluded that the Optimized Transistor Sizing (OTS) technique has the best ratio between nominal PDP and PDP under process variability.

[Ahmadi et al. 2017] introduces a new technique to improve the performance of digital circuits in the presence of variations. It consists of a hybrid of two former methods to prevent errors due to delay variations. The simulations were performed with a 45nm predictive technology using HSPICE and applied on ITC'99 and ISCAS'89 benchmarks circuits. The results show that this hybrid technique can tolerate process variations up to 27.3% better than state-of-the-art techniques.

Among these works there is [Dokania and Islam 2015] on which a novel technique based on the replacement of Full Adder's internal inverters with low voltage Schmitt Triggers for PVT variability robustness improvement is originally introduced and applied on seven different full adder designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in PDP. Although, the improvements occur at the cost of an increase in the area and power dissipation of each design.

Schmitt triggers are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. On a typical input (non-Schmitt trigger), its binary value will switch at the same point on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit causing a shift in the threshold voltage.

If the threshold shifts, it will cross the input causing it to switch again. It can go indefinitely causing oscillation. The same thing can happen if there is noise on the input. Schmitt Triggers are applied in these cases to filter noise introducing superior and inferior threshold voltages, as shown in Figure 3.c. The difference between the thresholds is called Hysteresis [Cockrill 2011], its curve is shown at 3.a. According to the Schmitt Trigger behavior, it can mitigate the influence of variations in the inputs product of PVT variability. In figure 3.c is shown a classical CMOS Schmitt Trigger design.

This technique is tested in several works: In [Ahmad et al. 2016] it is presented a novel Schmitt-trigger-based single-ended 11T SRAM cell. It analyses its performance against seven different SRAM topologies. The novel cell showed the least energy consumption per operation with the smallest leakage power and a 6.9x higher Ion/Ioff ratio. Further PVT variability simulations confirmed the robustness of the design regarding read and write operation. The simulations were carried in 22nm predictive technology using HSPICE.

[Moghaddam et al. 2017] presents a Schmitt trigger (ST) buffer using carbon nanotube FET (CNTFET). It was evaluated against other two buffers and showed, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain considering PVT variability robustness. The simulations were carried in 16nm Stanford CNTFET model using HSPICE.

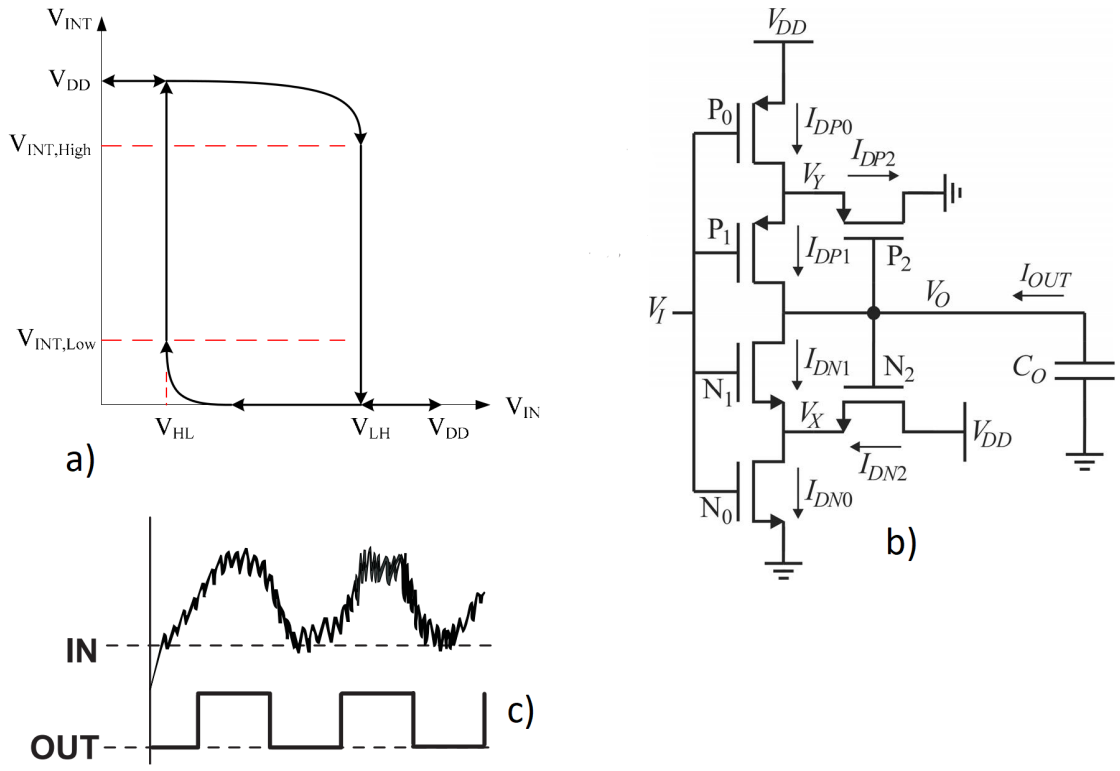

Figure 3. a) General Schmitt Trigger's hysteresis curve b) Classical CMOS Schmitt Trigger Topology c) Typical signal filtering with Schmitt Trigger [Cockrill 2011].

Alongside, in [Toledo et al. 2016] the ST technique is applied on four Full Adders. It presented promising results regarding the power deviation due to the process variability with a decrease up to 79% with a drawback of a significant increase in average energy consumption. The simulations were performed with the 16nm technology predictive technology model in NGSPICE.

3. Motivation and Objectives

Reviewing the works which have explored ST technique, it is evident that there is a lack of tests on layout level. These works have demonstrated the technique strengths at electrical level, with the circuits tested showing improved PVT variability robustness characteristics. Although, it is essential to shed light on multiple levels of abstraction simulation to give a more precise notion of the technique efficiency. Given that, the main goal of this work is to apply on four different full adder topologies at layout level designed on the 28nm FD-SOI technology the technique introduced at [Dokania and Islam 2015] of changing traditional inverters by Schmitt Triggers Inverters to mitigate variability effects, to measure the impact of such technique on power, timing and area.

4. Methodology

For the experiments, there will be considered four different types of Full Adders topologies to evaluate their robustness to process variability with their internal inverters replaced by Schmitt Triggers. The Full Adders listed below have been chosen due to

their promising results in related works [Ames et al. 2016] [Dokania and Islam 2015] [Dokania et al. 2013]:

1. Complementary MOSFET Adder (CMOS)
2. Transmission Gate Adder (TGA)
3. Transmission Function Adder (TFA)
4. Hybrid Full Adder

The CMOS Full Adder is considered the most traditional Full Adder topology containing 28 Transistors arranged in a pull-up and pull-down networks, which are logically complementary. It has a full voltage swing and buffered Sum and Cout signal and the advantages of good conductibility and robustness when working with novel technologies and low voltages. However, it has high capacitance because each input is connected to the gate of at least a PMOS and NMOS device additionally, it shows the impact of the pull-up network that makes the circuit slower due to the low mobility of its holes [Beckett 2002] [Devadas and Kishore 2017] [Islam and Hasan 2011].

Transmission Gate Full Adder [Weste and Eshraghian 1985] contains 16 transistors, and is a high speed and low power design. However, shows low driving capability which may be unacceptable in some cases where there is a long chain of full adders due to the increase in delay [Islam and Hasan 2011]. The Transmission Function Adder is based on transmission gates as well, containing 20 transistors, working satisfactorily with low voltages but losing performance when cascaded due to the lack of supply/ground contacts and, consequently, driving capability [Navi et al. 2009]. Both TFA and TGA generate the XOR function (H = A XOR B) followed by an inverter which produces the XNOR function (H'). H and H' are used to control the transmission gates generating the Sum and Cout outputs. The inverter generates delay between H and H', which will cause the transmission gates to behave as pass transistors, that may introduce glitches and consequently, increase the power consumption of these cells. Additionally, TGA contains three inverters, one more than TFA. The inverters switching introduce more short-circuit power [Shams and Bayoumi 2000].

Inspired by CMOS and CPL Full Adders architectures, the Hybrid Full Adder [Navi et al. 2009] contains 26 transistors, with the main advantage of a high output signal and low power properties. Although, the design shows high input capacitance for specific input vectors.

A variety of CMOS Schmitt Trigger designs have been proposed and implemented over the years, with the conventional 6T-CMOS Schmitt Trigger proposed in [Doki 1984] exhibiting the wanted characteristics of different high-to-low and low-to-high transition threshold voltages, giving rise to hysteresis. The ST inverter circuit used in this work was inspired by [Zhang et al. 2003] and modified in [Dokania and Islam 2015] to achieve the desired inverting characteristic, as shown in Figure 4. It is designed for operation at a supply voltage of 0.4V in order to achieve low power consumption, and consists of the junction of two inverters where the output from the second one will be the bulk for the first one.

In this design a dynamic body-bias technique is applied through a feedback mechanism to a standard CMOS inverter circuit, thus allowing a change in the threshold voltages of two MOSFETs, implying a change in the switching voltage. The Full Adder designs are shown in Figure 5.

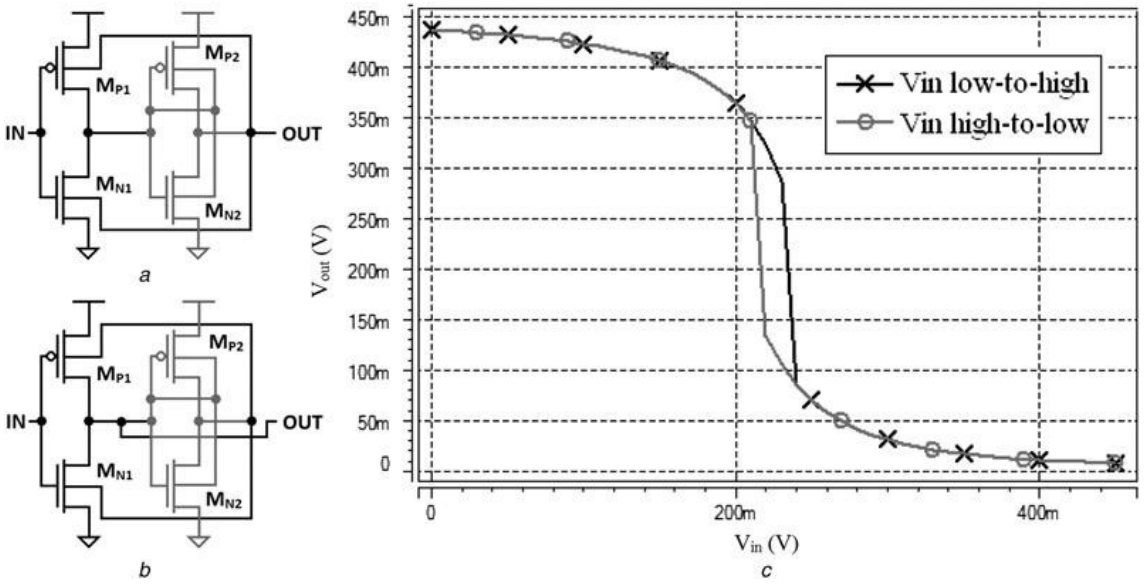

Figure 4. Original Low Power Schmitt Trigger (left above), Modified Low Power Schmitt Trigger (left below) and its hysteresis curve (right) [Dokania and Islam 2015].

All Full Adders layouts will be designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence® with the process design kit (PDK) of 28nm FD-SOI from ST Microelectronics. The simulations will be carried out in HSPICE from Synopsys Company, after the removal of parasitic capacitances from the layouts. Each full adder will be designed with and without the Schmitt Triggers replacement in order to take into account the penalties due to the adoption of the ST technique in terms of area, power consumption and performance. The process variability evaluation will be conducted by 2000 Monte Carlo simulations varying the threshold voltage of the PMOS and NMOS devices according to a Gaussian distribution.

For all experiments, it will be observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: delay, power and energy, where σ/μ represents the sensibility of the cell to process variability.

To avoid underestimating effects of realistic input waveforms on design metrics, the simulations will be carried under a 5-bit ripple carry adder using copies of the 1-bit full adder cell with design metrics being calculated for the middle cell as shown in Figure 6.

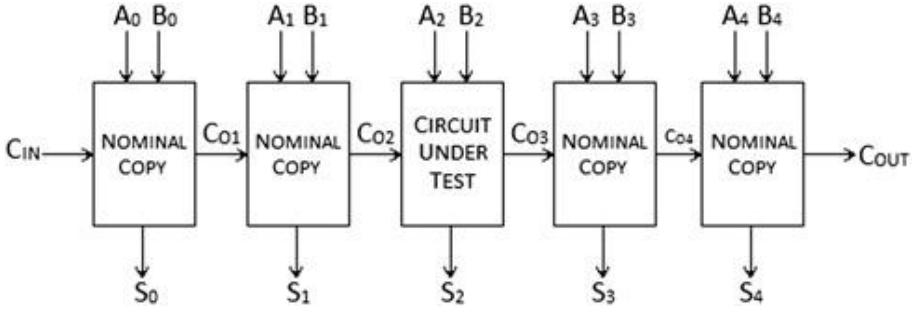

Figure 6. Test Bench [Dokania and Islam 2015].

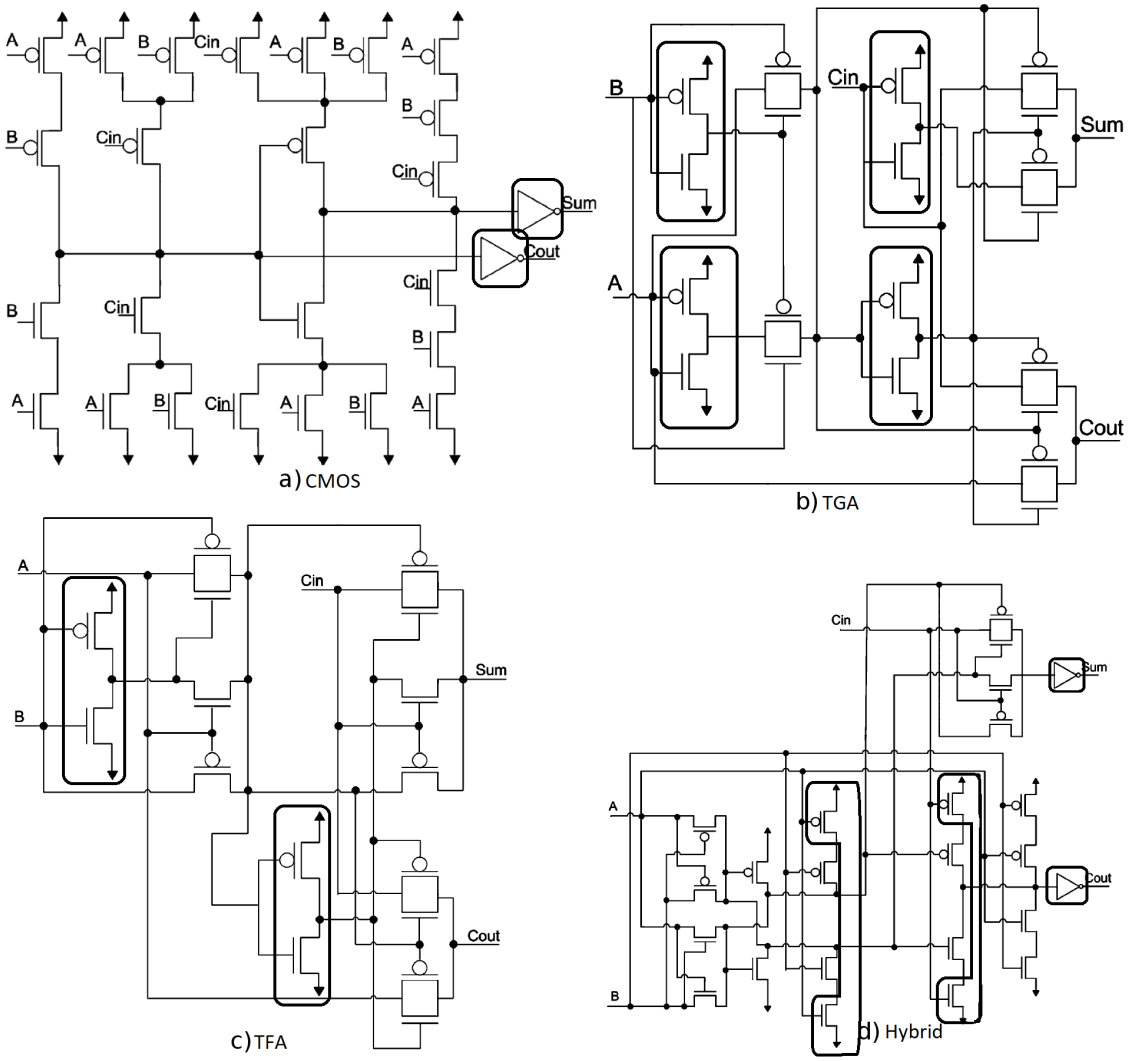

Figure 5. Full Adders with internal inverters to be replaced highlighted [Toledo et al. 2016].

5. Schedule

The reading of articles and review of the state of the art required for the development of this research were carried out from October to December of 2017. This work development will continue accordingly to the schedule presented at Table 3, being executed until the beginning of July.

Table 3. Activity Schedule for 2018

Activity	Jan	Feb	March	April	May	June	July
Familiarization with ST's PDK and dimensioning of the adder transistors	X						
Layout generation without the ST technique		X	X				
Layout generation with the ST technique			X	X			
Analysis and writing of results					X	X	
Writing of TG2 and submission of articles					X	X	X

6. Conclusions

Variability in deep submicron technology is an issue which needs addressing. It can mine any improvement made over technology generations introducing variations in the circuits behavior making it not comply with the industry needs. There are few works introducing novel techniques to mitigate variability effects at circuit level to decrease its impact in its absolute values. Instead, most of the existing techniques aim to detect errors not addressing the problem directly.

Emerging novel technologies are analyzed to compare to previously established technologies for variability robustness improvement. Overall, these technologies bring improvements in performance and power consumption, although it barely addresses the variability concern. A novel technique is introduced which consists of replacing internal inverters of full adders (extendable to other types of logic blocks) with Schmitt Triggers to filter the variations on its inputs providing a more predictable behavior.

This technique has been used and, by now, seems to be a considerable choice. Although, it has not been tested at layout level. This next level of abstraction is necessary to bring a more accurate prediction of the real influence of this technique over target specific circuits.

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