Indian Institute of Technology Hyderabad

Course: Electronic Devices & Circuits Lab

Course Code : EE2301

Lab Assignment 5

Successive Approximation Register Analog to Digital Converter

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1 Introduction

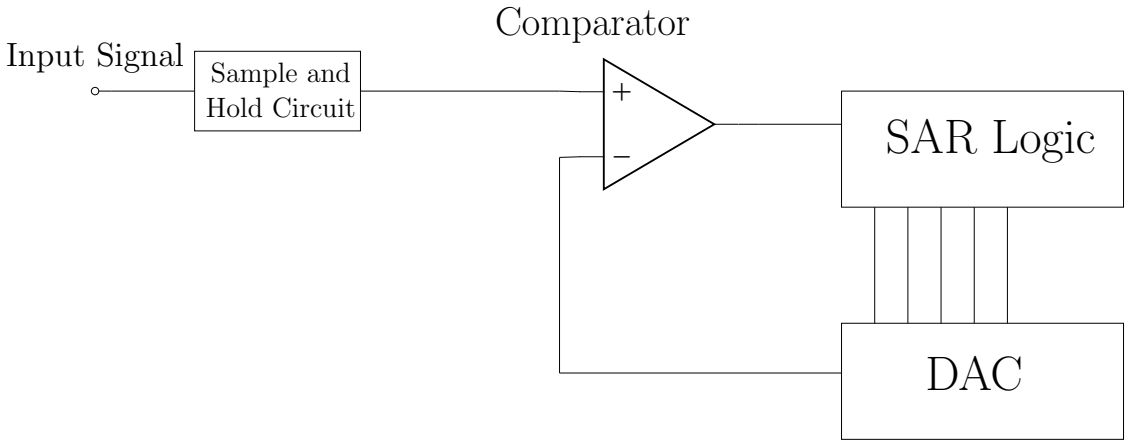
Analog-to-Digital Converters (ADCs) convert continuous analog signals into discrete digital signals, enabling the processing of analog information in digital systems. In this lab project, a SAR ADC was designed and implemented using D Flip-Flops to form the SAR logic, a sample-and-hold circuit to capture the input signal, and an R-2R ladder Digital-to-Analog Converter (DAC) to produce accurate analog reference voltages for comparison.

2 Aim of the Experiment

The aim is to create a functioning SAR ADC that can accurately convert an analog input to its digital equivalent through a step-by-step approximation process.

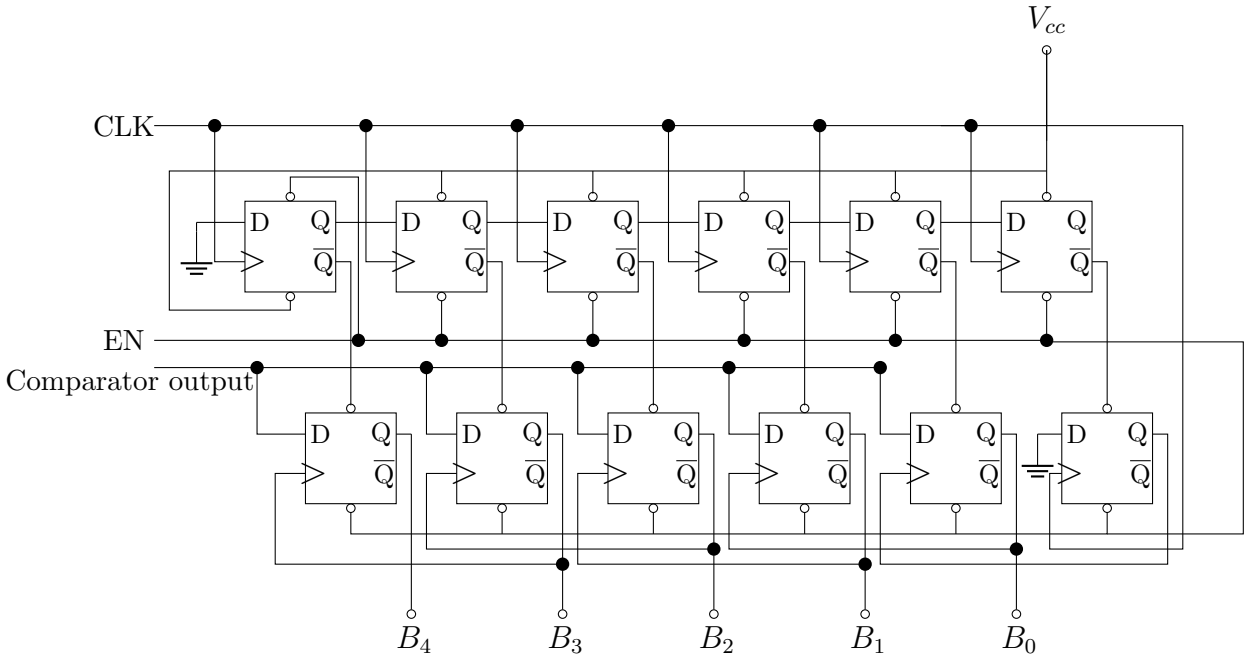
3 Experimental Setup

The circuit consists of 3 parts with their circuit diagrams as given below:



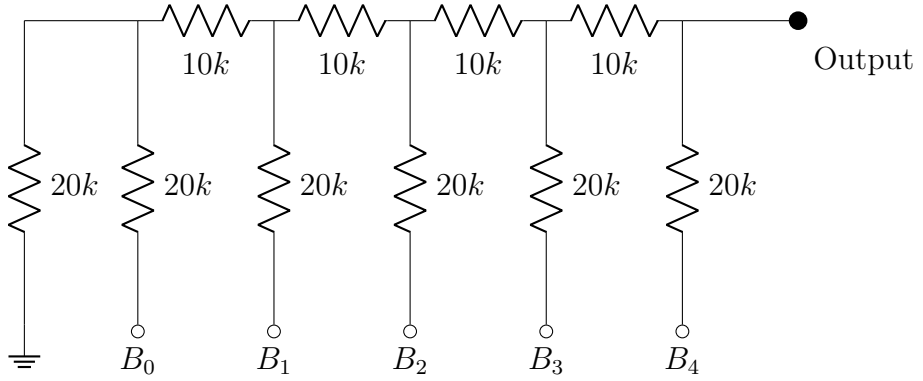
1. **Successive Approximation Register**

   Consists of 12 D Flip Flops (6× 7474 ICs) connected in the below configuration:



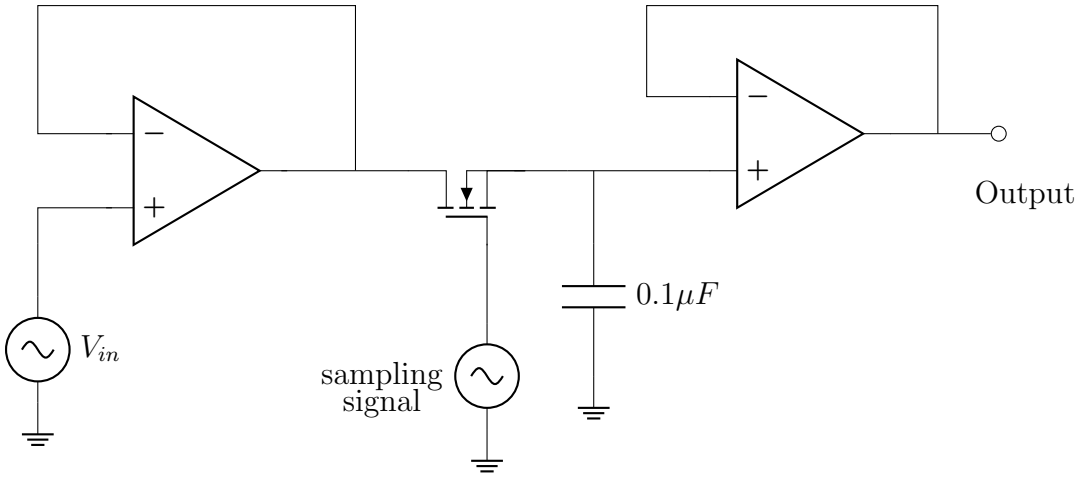
2. **R-2R Ladder Digital-to-Analog Converter**

Consists of R ($10k\Omega$) and 2R ($20k\Omega$) resistors connected in the below ladder configuration:



3. **Sample and Hold Circuit**

Consists of one op-amp (LM386) as input buffer, a MOSFET (N7000) to control sampling rate, a capacitor (to hold the sampled voltage) and an another op-amp (LM386) as the output buffer. These are connected as shown below:



4 Working Principle

1. **Sample and Hold Circuit**

   The sample and hold circuit samples the analog input signal and keeps its value constant for the time it takes to give the digital output in SAR. The input signal is given to a buffer op-amp which outputs the voltage to the MOSFET. The MOSFET is switched at the sampling frequency. When the MOSFET is on, the capacitor right after it charges to the input voltage. Then the MOSFET turns off but the capacitor maintains the same voltage for the output buffer. This way, the input signal is sampled and held.

2. **Successive Approximation Register**

Inputs		**Outputs**			
$\overline{PR}$	$\overline{CLR}$	**CLK**	**D**	**Q**	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	$\overline{Q_0}$

D Flip Flop Truth Table

- The Enable signal is a waveform that remains low for a short duration and remains high for the remaining time period. This causes all the D Flip Flops on the top row to store 100000 (first flip flop has $\overline{PRE} = 0$

and $\overline{CLR} = 1$ which sets it to 1 and remaining 5 have $\overline{PRE} = 1$ and $\overline{CLR} = 0$ which sets them to 0).

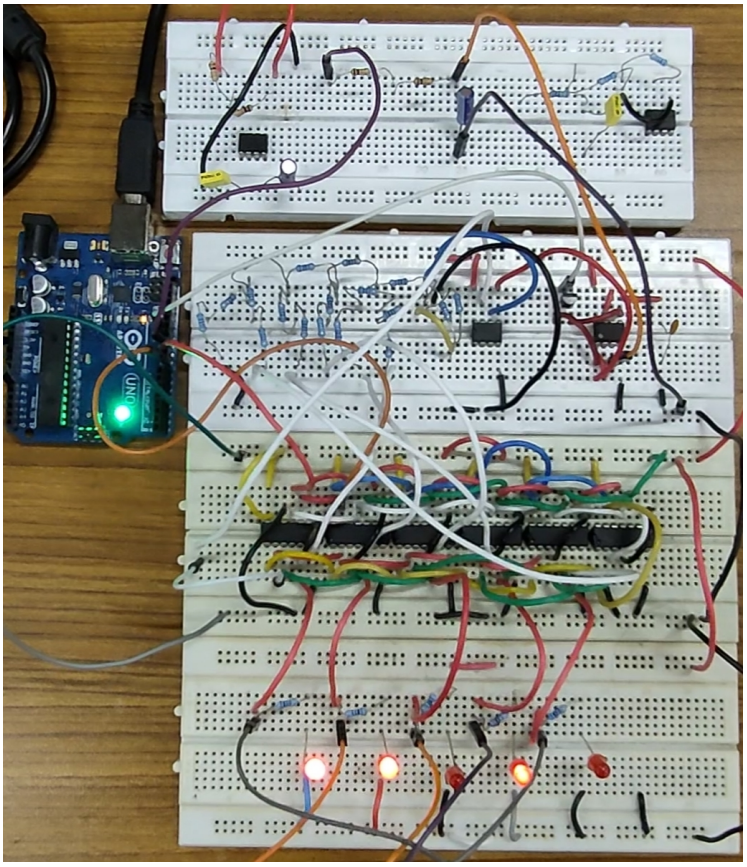
- 100000 in the top row causes the $\overline{PRE}$ of the lower-row flip flops to be 011111 respectively (note that $\overline{Q}$ is connected here). When EN is low, $\overline{PRE} = 1$ and $\overline{CLR} = 0$ for last 5 FFs so they set to 0. When EN becomes high, $\overline{PRE} = 0$ and $\overline{CLR} = 1$ for first FF so it becomes 1. Therefore, lower row becomes 100000 just before any operation begins. The 5-bit output is 10000, the starting state.
- Now, EN is high so the top row of FFs is in normal operation. The 1 in the first flip flop will move forward (like a shift register) at rising edges of the clocks ($100000 \rightarrow 010000 \rightarrow 001000 \ldots \rightarrow 000001$). Now, in the top row, if a FF stores 0, the FF right below it is in normal operation mode, while if the top row FF stores 1, the FF right below it is pulled to 1.
- Let us assume the sampled voltage (explained in later parts) is such that the target output is 11010.
  - The SAR output initially is 10000, so it is lower than 11010. The comparator will give output 1 (explained later). When top row is 100000, the first lower FF is pulled to 1.
  - In the next rising edge, top row becomes 010000, causing 1st lower FF to be in normal operation. The 2nd lower FF is pulled to 1 from 0, triggering the 1st FF to store comparator output 1 (output = 11000, lower than 11010).
  - In next clock edge, top row is 001000, causing 3rd FF to be pulled to 1 from 0, causing 2nd FF to trigger and store 1. Now output is 11100, which is more than 11010, so comparator output is 0.
  - In the next cycle, top row becomes 000100, similarly 3rd FF will trigger and store 0 (comparator output), so now output is 11010. Due to non-ideality of sample hold circuit (i.e., it can't sample exactly 26), comparator output may become 1 (if input is more than 26).
  - The operation will continue similarly and final output at the end of 5 clock cycles will be 11010.
- Once the output is obtained, it remains visible till the EN becomes 0. This again causes the starting state 10000 right after EN becomes 1. The SAR now finds the value of the new sampled voltage in binary.

3. **R-2R Ladder DAC**

   Refer to diagram in **Experimental Setup** section.

   The equivalent voltage between B_0 and ground to V_{Node_1}:
   $(V_{Node_1}) = \frac{V_{B_0} \times 20K\Omega + 0 \times 20K\Omega}{20K\Omega + 20K\Omega} = \frac{V_{B_0}}{2}$
   And the equivalent resistance between B_0 and ground to $V_{Node_1} = 10K\Omega$
   Similarly, The equivalent voltage between B_1, B_0 ground:
   $(V_{Node_2}) = \frac{\frac{V_{B_0}}{2} \times 20K\Omega + V_{B_1} \times 20K\Omega}{20K\Omega + 20K\Omega} = \frac{V_{B_0}}{4} + \frac{V_{B_1}}{2}$
   And the equivalent resistance between B_1. B_0 and ground to $V_{Node_2} = 10K\Omega$
   Continuing till Output node, We get:
   The equivalent voltage between B_4, B_3, B_2, B_1, B_0, ground to Output:
   $V_O = \frac{V_{B_0}}{32} + \frac{V_{B_0}}{16} + \frac{V_{B_0}}{8} + \frac{V_{B_0}}{4} + \frac{V_{B_1}}{2}$

A picture of the circuit is attached below:



5 Observations

To check the functioning of the ADC, we tested it with two types of inputs: Sine Wave and Sawtooth Wave each of time period 32 seconds. The output of the SAR (bits B_0 to B_4) were visualized through LEDs. They were also input to an Arduino to convert them into the relevant decimal value and plot the digital version of the analog input.

The outputs are shown below:

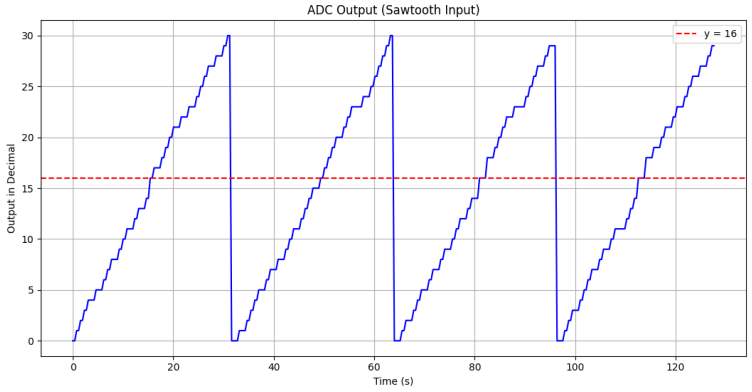


Figure 1: Output for Sawtooth Input

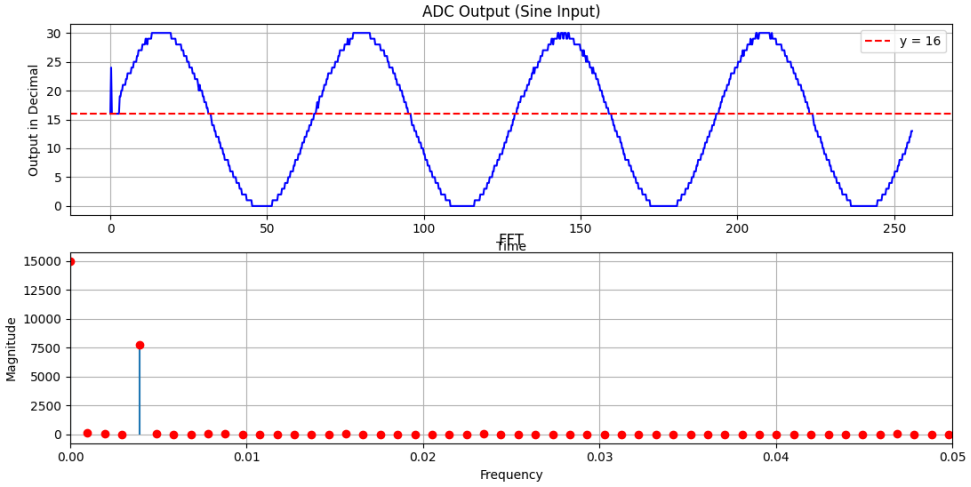


Figure 2: Output and FFT for Sine Input

The Fourier Transform for the sine input was also calculated and plotted. It is

observed that the peak frequency corresponds to a time period of 256 seconds. There are 4 cycles plotted which means that time period of each cycle is 32 seconds, equal to the input sine wave's time period. There were imperfections in the data measurement as a result of which it is showing the combined period of 4 cycles.

6 Challenges

Few of the challenges we faced while building the circuit were:

- Precise timing of the clock, enable and sampling frequencies was difficult to achieve for high frequency inputs. Ideally, the ADC should give the output in short time but for high frequency signals, it is difficult to demonstrate with the clock frequency generated by Arduino which is limited to 1 MHz.
- Modifying the circuit by varying enable signal was required to update the output corresponding to variable input in real time.

7 Conclusion

The Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) was successfully designed and implemented using D Flip-Flops for SAR logic, a sample-and-hold circuit, and an R-2R ladder Digital-to-Analog Converter (DAC). The observations demonstrated that the SAR ADC effectively converted analog signals to digital form.