EE6361:Advanced Topics in VLSI

Assignment 1

1. Write a Verilog code to create a memory consisting of 32 registers of 8 bits each. Control the read and write operations using signals read enable and write enable respectively. Use a 5-bit address bus (5:32 decoder) for register selection

2. Also Write a testbench code to demonstrate:

   a) Writing a value into selected register.

   b) Reading from selected register.

   c) Moving contents from one register to another.

Note:

- First understand how to create a Flip flop and register with read and write enable signals. Then create a Register bank with read and write enable signals and address select lines. Next build a 5:32 decoder to reduce the number of address lines.
- We will also run a plagiarism check to ensure that the code is not copied .
- Maintain Good Practices and add comments in your code explaining what you have done.
- Assignment should be submitted on or before **Thursday,22 February 2024,11:59:59 pm** .
- Assignment should be sent in a zip file to **cindrellask@tenet.res.in** and cc to **ee23s059@smail.iitm** with subject **"EE6361 Assignment 1".** The format of the zip file should be (Rollno).zip
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  The zip file should contain:
  a) .v files of the module and testbench
  b) Screenshot of the Simulation