Design of a Bluetooth Receiver and narrowband LNA using 0.13 µm CMOS technology

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Abstract **- In this paper, an approach to design the RX chain for Bluetooth using the given specification is described in the first half. The receiver specifications at each point in the chain are described along with the test taken or the scenario achievable by the blocker mask. In the second half, the design of a narrowband LNA using CMOS technology in Cadence is described along with the simulation results.**

Keywords - RF, low IF, LNA, CMOS, blocker, modulation

I. INTRODUCTION

The current trends in the semiconductor industry are leaning towards computing and communication with devices which have low form factors and consume less power. While scaling in transistor technologies and novel design techniques at the higher levels of design have enabled prototyping and have shortened time-to-market, architectural innovations in transceiver design will help in the reliable transfer and receipt of information in a fast-paced society.

There are numerous papers which describe various receiver architectures, such as super-heterodyne, homodyne, image-reject and low-IF architecture. Each architecture comes with its own pros and cons, and a designer would need to choose the appropriate architecture on the basis of several factors such as:

1) The number of components,
2) The overall noise figure,
3) The overall gain of the system,
4) Various second order effects such as inter-modulation, cross-modulation, gain compression, etc.
5) The sensitivity of the received signal.

amongst others. The sections below describe each of the architectures in brief, before going on to describe the architecture chosen to meet the given Bluetooth specifications.

II. RECEIVER ARCHITECTURES

A. Super-heterodyne Receiver Architecture:

The Super-heterodyne architecture was the most widely used receiver for wireless purposes in the past due to its high selectivity and sensitivity. It consists of three discrete component filters: RF Filter, Image-Reject Filter and IF Filter [1].The RF filter removes out-of-band interferers or blockers and rejects image-band signals as well. The image-reject filter usually appears after the LNA and attenuates the unwanted signals present at image frequencies. The IF filter which follows the first downconversion mixer reduces the distortion and linearity requirements of successive stages in the receiver chain.

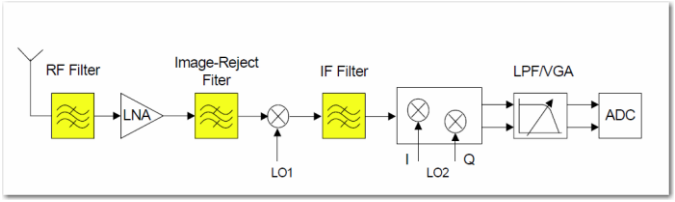

Fig 2.1. Conventional Super-heterodyne receiver architecture

The first mixer down-converts the incoming RF signal to the first high IF and then to second or zero IF. The second mixer then down-converts the resultant signal from first IF to DC (zero IF). Image signals arising from adjacent bands or in band are suppressed by placing the image-reject filter before the first mixer. The use of high IF provides significant image rejection while low IF suppresses nearby interferers. However both of these require large Q, which is not practically feasible. Since the filter is realized using passive components and since the LNA drives the 50-Ω input impedance of the same, this imposes heavy constraints in the LNA in terms of noise figure, stability, and power dissipation. We therefore take a look at another method of suppressing images, known as the image-reject architecture.

B. Image-Reject Receiver Architecture:

The image reject architecture relies on the ability to process the image and the desired signal differently, cancelling the image using its negated replica[1]. This is possible since the signal and the image are on the opposite sides of the LO frequency. There are 2 main architectures used for this: 1) Hartley and 2) Weaver. In the Hartley architecture, the RF input is mixed with the quadrature phases of the local oscillator, low-pass filtered, and shifted in-phase by 90°. The image is then cancelled by adding the in-phase and quadrature components.

However, the phase imbalance in LO and the gain imbalance in the shifter causes the image to corrupt the downconverted signal. With a high IF, proper image rejection can be achieved. However, the stringent matching requirements and

the effects of noise are often a deterrent from using this architecture. In the Weaver architecture, the phase shifter from Hartley is replaced by a second quadrature operation, reversing the polarities of the signal and the image. Thus, subtraction gives the signal, while addition gives the image portion. There exists, however, the problem of incomplete image rejection due to gain and phase mismatch. The problem of second image also exists due to the fact that the secondary downconversion mixer may translate the IF signal to nonzero frequency, causing the secondary interferer's image to fall into the desired channel. This can be resolved using four mixers and adding/subtracting the 4 I/Q components depending on their position w.r.t f_{LO1}. The additional cost of 4 mixers proves to be a deterrent, forcing us to look at the homodyne architecture.

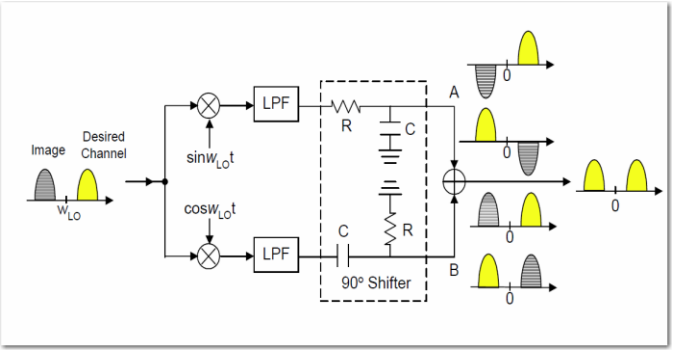

Fig 2.2 Hartley architecture

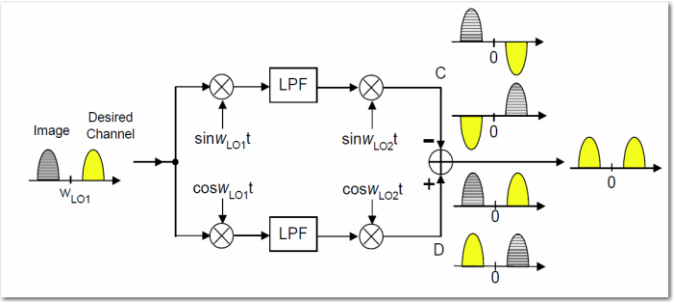

Fig 2.3. Weaver architecture

C. Homodyne (Zero-IF) Receiver architecture:

The homodyne architecture only requires a lowpass filter with sharp cutoff characteristics [1]. The drawbacks of this filter are dc offset, which may be caused by LO leakage appearing at the inputs of the LNA and the mixer, producing a time-varying DC offset. The multiplication of a interferer leaking from the LNA or mixer to the LO port with itself, also called 'LO *self-mixing'* can saturate successive stages, preventing signal amplification. Flicker noise can be reduced by using BJT's or PMOS devices. Even order distortion can also result in low frequency beats appearing at the output of the mixer, corrupting the desired signal. We therefore take another architecture free of these issues, which is known as the low-IF architecture.

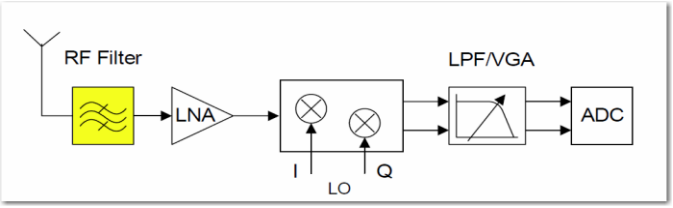

Fig 2.4. Conventional homodyne receiver architecture

D. Low-IF Receiver architecture:

In the low-IF architecture. the signal is translated to IF frequency, which is close to DC (zero frequency) [1]. The image reject filter is now replaced by a poly-phase filter, which provides considerable attenuation in the image frequency band. Furthermore, quadrature mixers are used to for further image rejection when the IF signal is converted to zero frequency in the digital domain. The low-IF frequencies could be from several kHz to several MHz depending on the wireless standard used.

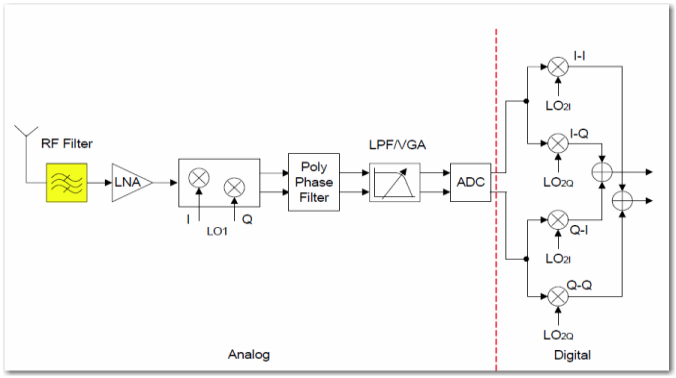

Fig 2.5. Low-IF receiver architecture.

III. ARCHITECTURAL CHOICE

For Bluetooth, the low-IF architecture was chosen because the modulation scheme Bluetooth uses is Gaussian Frequency Shift Keying (GFSK). In this scheme, since the spectrum has considerable energy at zero frequencies, image rejection must be performed without signal distortion. This necessitates the need to use poly-phase filters, which offer considerable attenuation at image frequencies without signal distortion. Bluetooth operates in the ISM band, which ranges from 2.4 GHz to 2.4835 GHz. Hence we use an RF filter at the front end to select this band and suppress out-of-band blockers. Double-balanced mixers are used as direct-conversion mixers for less even order distortion. This serves to suppress the low-frequency beat caused as described above in the direct-conversion architecture section due to LNA non-linearity, which would degrade IIP2 severely. Single-ended to differential converters are also used since the LNA output is single ended while the mixers require differential RF inputs. Placing the SDC between the LNA and the mixers also helps to avoid LO leakage to the LNA or the antenna to some extent. The poly-phase Butterworth filter is used for image rejection.

The low-pass filters in the LPF/VGA chains are selected to be programmable to change the cutoff frequency in order to select the desired channels. The VGA is used to adjust the input of the ADC to the appropriate levels and its gain is determined by using the minimum and maximum reception levels for Bluetooth. The ADC's are programmable for the Bluetooth standard.

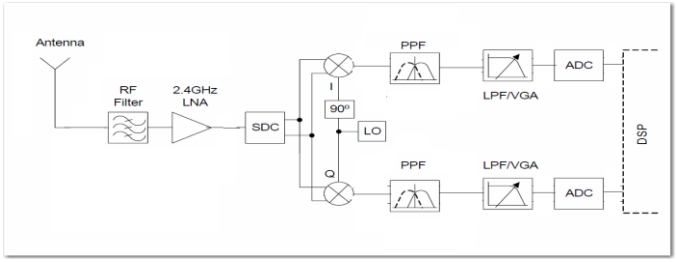

Fig 3.1 Proposed Low-IF receiver architecture for Bluetooth.

IV. AIR INTERFACE, BLOCKING PROFILE AND INTERMODULATION CHARACTERISTICS

The air interface for Bluetooth specifies a bandwidth of 1 MHz, with the modulation scheme chosen to be GFSK. The channel spacing is the same as the channel bandwidth. FHSS (Frequency Hopping Spread Spectrum) is chosen as the multiple access scheme. Time-Division-Duplexing (TDD) is used as the duplexing standard. The blocking profile shown below can be used to define the top-level system specifications.

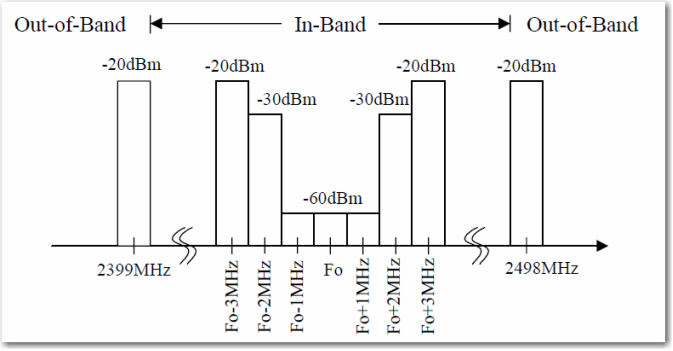

Fig 4.1 Bluetooth blocking profile

The intermodulation characteristics are used to derive linearity specifications such as IIP2 and IIP3. The tests used for the above as taken from the PHY are: The reference sensitivity (-70dBm) performance, BER=0.1%, shall be met under the following conditions.

- The wanted signal at frequency fo with power level 6dB over the reference sensitivity level.
- A static sine wave signal at f1 with a power level of -39dBm
- A Bluetooth modulated signal at f2 with a power level of -39dBm such that fo=2f1-f2 and |f2-f1|=n*1MHz, where n can be 3, 4, or 5.

The system must fulfill one of the three alternatives.

V. TOP-LEVEL RECEIVER SPECIFICATIONS

The top-level receiver specifications such as the noise figure, linearity, phase noise and dynamic range of the ADC can be extracted by examining the Bluetooth standard [1][7].

A. Noise Figure:

Noise Figure is a measure of how much the SNR degrades as the received signal passes through the receiver. The definition of noise factor, which can be converted to noise figure by taking 10*Log, is:

$$\text{noise factor} = SNR_{in}/SNR_{out} \qquad (5.1)$$

The relationship between the required *SNR*, which is required to maintain the required BER (Bit Error Rate), and the overall system noise figure (NF_{system}) is expressed by:

$$NF_{system} = P_{min} + 174dBm/Hz - SNR_{req} - 10Log(BW) \qquad (5.2)$$

where P_{min} is minimum sensitivity, SNR_{req} is minimum *SNR* for certain BER, and *BW* is channel bandwidth. Based on the air interface for Bluetooth and the specifications in the PHY, the overall NF_{system} for Bluetooth is found to be 21dB.

Table 5.1 : Bluetooth NF specification

$Sensitivity_{min}$	$Noise_{in}$	SNR_{in}	SNR_{req}	NF_{system}
-70dBm	-114dBm	44dB	23dB	21dB

B. Input-Referred Third Order Intercept Point (IIP3):

The input referred third-order intercept point is a measure of how linear a system is. This is because in-band interferers cannot be blocked by the front end RF filter, and these in-band interferers can give rise to third-order intermodulation products, that can lie in-band and corrupt the desired signal. This requires that the IIP3 of a system be sufficiently high to avoid non-linearity due to IM3 products. The overall IIP3 of the system can be calculated as follows:

$$IIP3_{system} = P_{int} + (P_{int} - P_{sig} + SNR_{req} + M)/2 \qquad (5.3)$$

where P_{int} is the power of the interferer, P_{sig} is the power of the desired signal, SNR_{req} is the required SNR, and *M* is the system margin, which is usually 6dB. Based on this, the overall $IIP3_{system}$ for Bluetooth comes out to be -17.5 dB. In case one wishes to take the cross-modulation effect due to mixing of the blocker with TX leakage into RX , then we can also calculate IIP3 due to cross-modulation as follows:

$$IIP3_{cross\text{-}mod} = P_{TX\text{-}Leakage} + (P_{blocker} - P_{cross\text{-}mod} + c)/2 \qquad (5.4)$$

where $P_{TX\text{-}leakage}$ is power of the transmission leakage, $P_{blocker}$ is power of the blocker, $P_{cross\text{-}mod}$ is the power of the cross-modulation with respect to the thermal noise floor, and *c* is the correction factor, which can be varied according to the standard. The IIP3 in this case is higher due to cross-modulation.

C. Input-Referred Second Order Intercept Point (IIP2)

Second-order distortion can arise in low-IF receivers, when low-frequency beats due to IM2 products appear at the output due to the feed-through of the mixer. This can be lowered by using double-balanced mixers as suggested in Section III. IIP2 is used to characterize second-order distortion and is calculated as follows:

$$IIP2_{system} = 2*P_{int} - P_{sig} + SNR_{req} + M \qquad (5.5)$$

where P_{int} is the power of the interferer, P_{sig} is the power of the desired signal, SNR_{req} is the required SNR, and *M* is the system margin, which is usually 10 ~ 15dB. Based on this, the overall $IIP2_{system}$ for Bluetooth comes out to be 12 dBm.

D. Phase Noise:

Since local oscillators are not ideal, the spectrum can exhibit the shape of a skirt near the center frequency due to phase noise. Hence, in the output, the skirt of the desired signal can overlay with the skirt of the interferer, leading to a phenomenon called as *'reciprocal mixing'*. Considering both the in-band and out-of-band blocking profiles, and a constant phase noise across the band of interest, the required phase noise, $PN(\Delta f_c)$of local oscillator at a frequency offset Δf_c from the desired LO frequency is obtained as follows:

$$PN(\Delta f_c) = P_{sig} - P_{blocker} - 10\log(BW) - SIR \qquad (5.6)$$

where P_{sig} is the power of the desired signal, $P_{blocker}$ is the power of the blocker, BW is the bandwidth, and SIR is signal to reciprocal mixing interferer ratio, which is 15dB. Based on this, the phase noise for Bluetooth is as follows:

Table 5.2 : Bluetooth phase noise specification

Offset	1MHz	2MHz	3MHz
Phase Noise	-80dBc/Hz	-110dBc/Hz	-120dBc/Hz

For lower phase noise, the SIR must be atleast 15 dB or above.

VI. SUBDIVISION OF SPECS ALONG RX CHAIN

To satisfy the overall system requirements regarding IIP2, IIP3, gain and noise figure, a proper distribution of the same is required across all the building blocks listed in Figure 6. The VGA range must be considered to reduce the dynamic range of the ADC and ensure strong input levels for the same.

A. Noise Figure:

Using Friis equation, we have:

$$NF_{total}=1+(NF_1-1)+(NF_2-1)/A_1+(NF_3-1)/A_1A_2+\ldots+(NF_n-1)/A_1A_2..A_{n-1}$$

where NF_{total} is the cumulative noise figure of n-stages referring to the input of the first stage, NF_i is the noise figure of the *i-th* stage, A_i is the gain or attenuation of the *i-th* stage. Our objective is to make NF_{total} less than NF_{system} as specified in Section V.A. We use the 2 stage version of the equation above and extend it to calculate the NF_{total} at the input of the system. Note that a lower NF can be achieved if the gains of the first few stages are relatively high, and our distribution therefore aims to lower noise figure by achieving the same.

B. Input-Referred Third Order Intercept Point (IIP3):

The IIP3 test, also known as a *'two-tone'* test, is performed by applying 2 interferers close to each other in the frequency domain, which leads to some non-harmonic output components. This arises due to mixing of the two when their sum is raised to a power greater than unity. Assuming that the IM3 signals are correlated (the worst case) and therefore add in phase, we have:

$$1/IIP3^2_{n\text{-}stages}=1/IIP3_1^2+A_1^2/IIP3_2^2+A_1^2A_2^2/IIP3_3^2+..(A_1A_2..A_{n-1}^2/IIP3_n^2 \quad (6.2)$$

In order to achieve a high IIP3, the gains of the preceding stages must be relatively low, while those of the latter stages relatively high. Note that this is in direct conflict with the requirements for a low noise figure, and hence a tradeoff must be made.

C. Input-Referred Second Order Intercept Point (IIP2):

The calculation for IIP2 is similar to IIP3 and it is assumed that the IM2 signals are correlated and therefore add in phase, giving:

$$1/IIP2^2_{n\text{-}stages}=1/IIP2_1^2+A_1/IIP2_2^2+A_1A_2/IIP2_3^2+\ldots A_1A_2..A_{n-1}/IIP2_n^2 \quad (6.3)$$

The requirements for achieving a high IIP2 are the same as those for achieving a high IIP3.

VII. RECEIVER MODELLING

Using the equations described in Section VI above, we implement an excel-spreadsheet based calculator and choose the proper values of NF, IIP3 and IIP2 for each block, and iteratively calculate until NF_{total}, $IIP3_{total}$ and $IIP2_{total}$ are better than or equal to NF_{system}, $IIP3_{system}$ and $IIP2_{system}$ [7]. The block-level specifications for a few blocks are given below:

Table 7.1 Specification of polyphase filter (Butterworth)

Bandwidth	Image Attenuation (-0.5MHz)
1MHz	> 30dB

Table 7.2 Specification of low pass filter (Butterworth)

Bandwidth	Type
1 MHz	Programmable 6th order

For the variable gain range amplifier, the range chosen is 14-54 dB.

: Table 7.3 Specification of ADC

Dynamic Range	Resolution
51 dB	9 bits

The overall system specifications for the entire system are given below:

Table 7.4. NF subdivision

Block	NF (dB)	Cumulative NF (min gain)	Cumulative NF (max gain)
RF Filter	2	21.69	9.74
LNA	5(min),2(max)	19.69	7.74
SDC	10	27.55	23.98
Mixer	18	30.48	26.81
PPF	25	32.23	28.21
LPF	25	31.32	25.4
VGA	30(min),15(max)	30.17	15
ADC	30	N/A	N/A

Table 7.5. IIP2 subdivision

Block	IIP2 (dBm)	Cumulative IIP2 (min gain)	Cumulative IIP2 (max gain)
RF Filter	80	24.25	14.54
LNA	30(min),25(max)	22.27	12.55
SDC	40	34.86	32.91
Mixer	50	44.86	40.98
PPF	60	53.87	46.77
LPF	60	59.78	48.91
VGA	60(min),20(max)	51.75	11.75
ADC	70	N/A	N/A

Table 7.6. Gain subdivision

Block	Voltage gain (dB)	Cumulative gain (min)	Cumulative gain (max)
RF Filter	-2	-3	-3
LNA	8(min),18(max)	5	15
SDC	3	8	18
Mixer	2	10	20
PPF	0	10	20
LPF	0	10	20
VGA	14(min),54(max)	24	74
ADC	0	24	74

Table 7.7 IIP3 subdivision

Block	IIP3 (dBm)	Cumulative IIP3 (min gain)	Cumulative IIP3 (max gain)
RF Filter	50	-6.76	-3
LNA	0(min),-5(max)	-8.76	15
SDC	5	-0.13	18
Mixer	8	4.45	20
PPF	12	8.99	20
LPF	12	12	20
VGA	12(min),-30(max)	8.46	74
ADC	25	N/A	N/A

The table below compares the spreadsheet specs with the overall specifications: As observed, the performance of the receiver satisfies all of the overall system requirements. Here '*min*' stands for minimum gain while *'max*' stands for maximum gain. *N/A* stands for *'Not Applicable'* in the case the parameter measurement is not warranted.

Table 7.8 Performance summary

Parameter	Result	Requirement
NF (dB)	10.7	21
IIP3 (dBm)	-17.1	-17.5
IIP2 (dBm)	15.5	12

VIII. LNA DESIGN

The sections below describe the design of a narrowband LNA using 0.13µm CMOS technology in Cadence. It begins by describing the LNA topology chosen, the criteria used for verifying its architecture, and finally goes on to describe the simulation results.

IX. OVERVIEW

The LNA (Low Noise Amplifier) is a block that is commonly present at the front-end of all RF architectures. Being the first active block, the LNA is required to provide a very high gain so that the main focus of the succeeding blocks would be on noise reduction and not amplification. An LNA must provide good input impedance matching with 50Ω matching (100 Ω if differential). This is required since if the received signal was very weak most of it would be reflected and it would be impossible to provide proper amplification for the same. A low noise figure is also desirable since it heavily influences the receiver's sensitivity and its SNR (Signal-to-Noise Ratio).

X. INPUT IMPEDANCE MATCHING

An LNA must provide good input matching for the element that provides the signal from the antenna. Since the received signal is very weak, good input matching would ensure that none of the signal is lost due to transmission line effects between the LNA and the preceding block. This becomes even more crucial if the preceding block is an RF filter since they are extremely sensitive to termination impedances.

Several topologies have been proposed for solving the problem of input impedance matching, such as:

1) Resistive termination,
2) Shunt-series feedback,
3) Common gate, and
4) Common source with inductive degeneration.

Each topology has its own drawbacks. For example, using resistive termination can degrade the amplifier's noise figure. Shunt-series feedback often requires higher power dissipation compared to other topologies for the same noise figure. Hence, we chose one amongst the common gate and common source with inductive degeneration for our final implementation [2][4][5]. These two topologies are discussed next.

XI. COMMON GATE AND COMMON SOURCE CONFIGURATIONS

Figure 11.1 shows a common gate configuration that shows an input impedance (single-ended) of 50 Ω, which implies $1/(g_m+g_{mb})=50\Omega$, where g_m and g_{mb} are transconductances of the top-gate and back-gate transistors respectively. The principal drawback of the configuration would be that the transconductances cannot be high for fear of having improper input matching. The input impedance Z*in* is given as follows:

$$Z_{in} = (R_D+r_o)/(1+(g_m+g_{mb})\,r_o) = 1/(g_m+g_{mb}) \qquad (11.1)$$

where it has been assumed that $R_D << r_o$ and $1<< (g_m+g_{mb})\,r_o$.

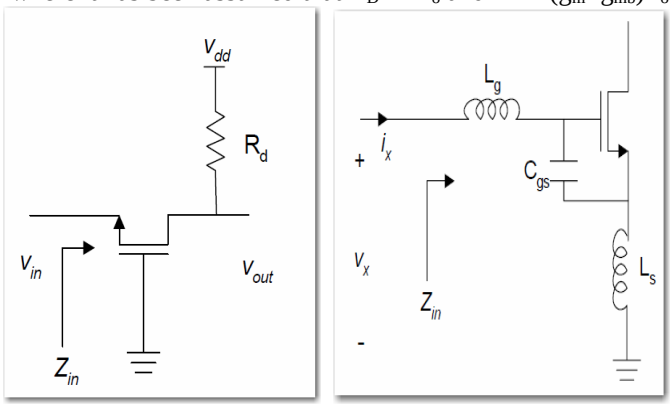

Fig 11.1 Common gate (left) and common source (right) LNA's

For the common source stage with inductive degeneration, we have:

$$v_x=i_x*s*L_g+i_x*(1/sC)+(i_x+g_mV_{gs})*s*L_g \qquad (11.2)$$

$$v_{gs}=i_x/(s*C_{gs}) \qquad (11.3)$$

Therefore, we can express Z_{in} as:

$$Z_{in}=v_x/i_x=s*(L_g+Ls)+1/(s*C_{gs})+(g_m*L_s)/C_{gs} \qquad (11.4)$$

At resonance, we have:

$$s*(L_g+Ls)+1/(s*C_{gs})=0 \qquad (11.5)$$

giving:

$$Z_{in}=(g_m*L_s)/C_{gs} = 50\Omega \qquad (11.6)$$

XII. NOISE MODELLING

The noise factor is usually defined as:

F=total output noise power/(output noise due to source alone) (12.1)

It serves as a measure of the degradation to the signal-to-noise ratio introduced by a system. The noise figure is obtained by taking 10*log(F). If no noise is added, F is 1 and the noise figure is 0dB. For calculating the noise produced by the common source configuration with inductive degeneration, we can use the model below:

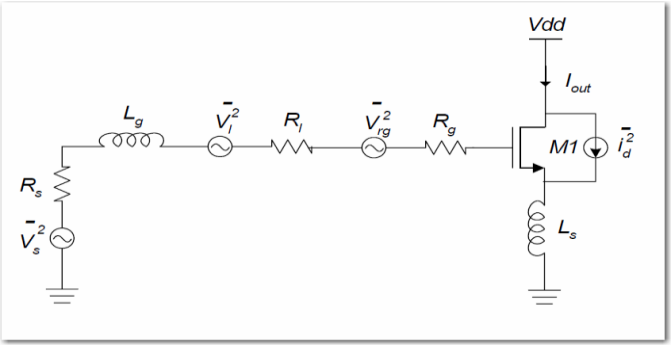

Fig 12.1 Circuit for LNA noise calculation

Here the most significant noise contributor is the drain channel thermal noise, which is modelled using I_d. Its value is given by:

$$i_d^2=4*k*T*\gamma*g_{d0}*\Delta f \quad (12.2)$$

where g_{d0} is the zero bias transconductance and γ is the coefficient of channel thermal noise. For long channel devices, it is 2/3. For short channel devices, it is much greater than 2/3. We use the following equation for finding the value of g_{d0} [6].

$$\alpha=(gm/gd0) \quad (12.3)$$

where α represents the departure in behavior from the long channel regime. We can refer the output noise current to the input as a voltage source by using the following equation:

$$v_n^2=i_d^2*r_{ds}^2/(g_m*r_{ds})^2= (4*k*T*\gamma*g_{d0}*\Delta f)/g_m^2 \quad (12.4)$$

This equivalent input referred noise source does not completely represent all the noise present at the output, since a current flows even when the input is open circuited and the induced gate current is ignored. To account for this open circuit condition, we multiply the input voltage noise source by the input admittance $\omega*C_{gs}$, yielding:

$$i_d^2=v_n^2*(\omega*C_{gs})^2=(4*k*T*\gamma*g_{d0}*\Delta f) *(\omega*C_{gs})^2/g_m^2 \quad (12.5)$$

Now adding all the noise sources at the input i.e $v_{in}^2=v_s^2+v_l^2+v_{rg}^2+i_d^2*R_s^2$, the equivalent noise voltage observed at the output is given by:

$$v_{in}^2=(4*k*T*\Delta f) *(R_s+R_l+R_g+(\gamma*g_{d0}*R_s^2* \omega^2)/ \omega_T^2))$$

wherein we have assumed $\omega_T=g_m/C_{gs}$ as the unity gain frequency of the transistor.

Substituting the above equations into the definition of F gives:

$$F=1+(R_l/R_s)+(R_g/R_s)+(\gamma*g_{d0}*R_s*(\omega/ \omega_T)^2) \quad (12.7)$$

We can deduce a few key points from the equation above as follows:

1) The last term in the above equation is the dominant term and shows that F increases with an increase in g_{d0}. We know that both g_m and g_{d0} increase with increasing $V_{ov}=V_{gs}-V_{th}$,. However, at the point of velocity saturation leading to short channel effects, g_m becomes constant and g_{d0} continues to increase, leading to an increase in F. So the characteristic shows that the noise figure drops initially with increasing V_{ov}, but increases later on due to increasing g_{d0}. This means there is an maximum current which can be present for optimal performance.

2) The physical dimensions of the transistor (W,L) can be modified as well for obtaining better performance. Making L smaller and increasing W helps to decrease the gate resistance R_g, and hence leads to a smaller gate noise contribution. But since I_d is directly proportional to W, increasing W, also leads to an increase in I_d beyond its optimum value and can negatively impact performance. So we need to choose an optimal width that can get us the optimal current I_d and hence the best performance.

3) If we were to choose the common gate topology and change W, then we would also change g_m and hence we wouldn't achieve proper input matching ($Z_{in}=1/(g_m+g_{mb})$)

4) Since we wish to achieve input matching to 100Ω differential and want to change W at the same time for best performance, we choose the common source topology.

XIII. DESIGN OF THE LNA

The requirements of the LNA in general are high linearity, low noise figure, moderate gain , input matching and low power consumption. The common source topology can satisfy all of these requirements, in addition to providing good reverse isolation. From Equation (6.2) and Equation (6.3), we see that linearity of the system is dominated by successive stages. Hence the primary goal of the LNA is to provide input matching and minimize power dissipation. The LNA is designed to provide 20dB or more in high gain mode and 8dB or more in low gain mode.

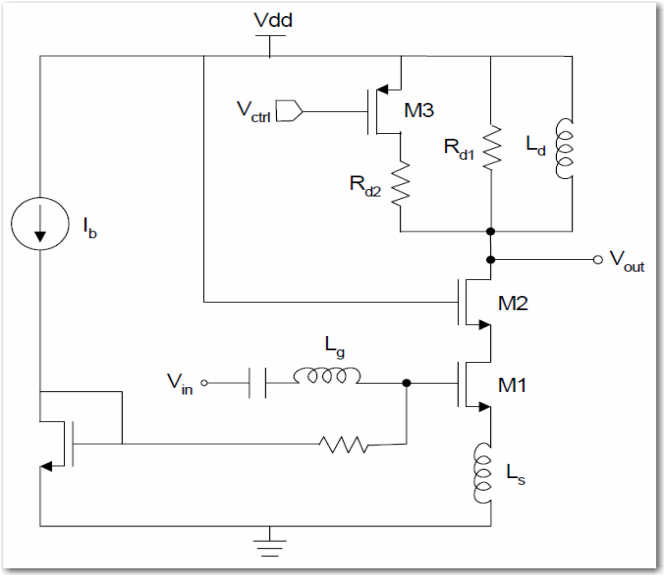

Fig 13.1 Proposed LNA schematic

The low gain mode is especially useful for applications such as AGC's (Automatic Gain Control) wherein the LNA must be in the above mode when the AGC is inactive to limit power consumption. The high gain mode involves the use of the damped resonator L_d and R_{d1}. The damping resistor R_{d1} provides sufficient bandwidth for the 2.4 GHz band. The

resonant frequency was calculated to be 2.45 GHz and the 1-db bandwidth was 300 MHz. We can achieve low gain by connecting R_{d2} in parallel with L_d and R_{d1}, and the Q of the resonator can be reduced by connecting R_{d2} to the drain of M3. The size of M3 is carefully chosen by considering the parasitic capacitances and the on-resistance since it affects the resonant frequency and gain of the LNA.

Since the LNA is differential, we use a balun so that we can apply differential inputs to it in our test circuit. Our example test configuration is show below:

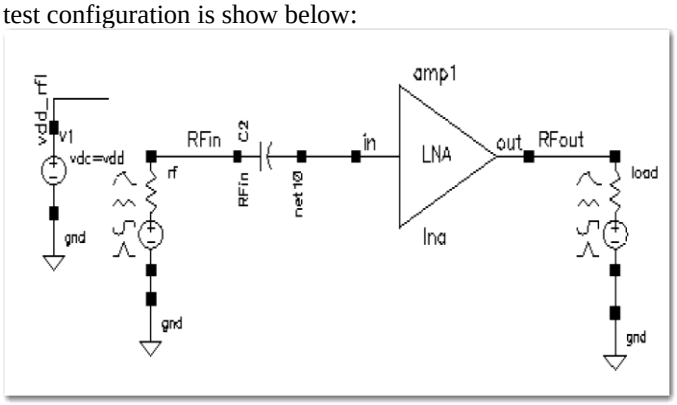

Fig 13.2 Testbench for proposed 2.45 GHz LNA

A. Matching Parameters:

The matching parameters of the chosen LNA were the S-parameters - S11, S12, S21 and S22.S11 and S22 are reflection coefficients, while S12 and S21 were transmission coefficients. The scattering parameter matrix of the single-ended LNA is given by [S11 S12; S21 S22]. Here S21 is the gain of the LNA while other parameters indicate the quality of impedance matching at each port. S12 is the strength of the reverse signal [3]. The simulated S-parameter results for S11 and S12 are shown below:

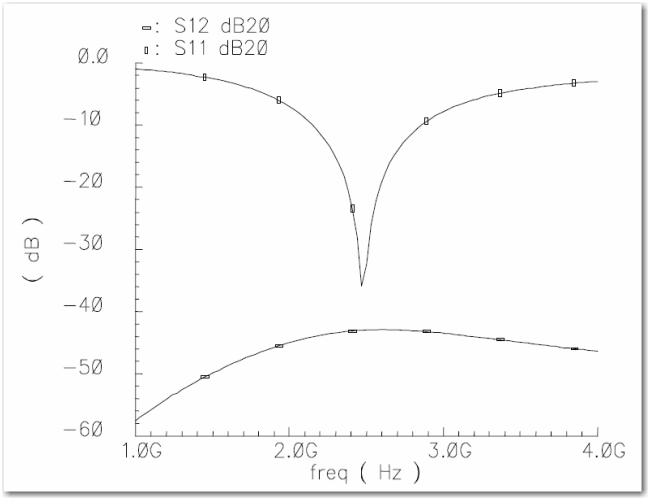

Fig 13.2 S11 and S12 for 2.45 GHz LNA

B. Gain:

Three gain parameters are normally used for verifying LNA design [3][4][5].

a) Transducer power gain G_T:

This is defined as the ratio of the power delivered to the load divided by the power available to the source.

$$G_T = ((1-|r_s|^2)*|s_{21}|^2*(1-|r_L|^2))/(|1-s_{11}r_s|^2)*(|1-r_{out}r_L|^2) \quad (13.1)$$

Operating power gain is defined as the ratio of the power delivered to the load and the power input to the network.

$$G_p = (1*|s_{21}|^2*(1-|r_L|^2))/(1-|r_{in}|2)*(|1-r_{22}r_L|^2) \quad (13.2)$$

c) Available power gain G_A:

Available power gain is defined as the ratio between the power available from the network and the power available from the source.

$$G_A = = ((1-|r_s|^2)*|s_{21}|^2*1)/(|1-s_{11}r_s|^2)*(1-|r_{out}|^2) \quad (13.3)$$

Because the power available from the source is greater than the power input to the LNA network, $G_p > G_T$. Also, because the power available from the LNA network is greater than the power delivered to the load, $G_A > G_T$.

The simulated results for the available power gain G_A is shown next:

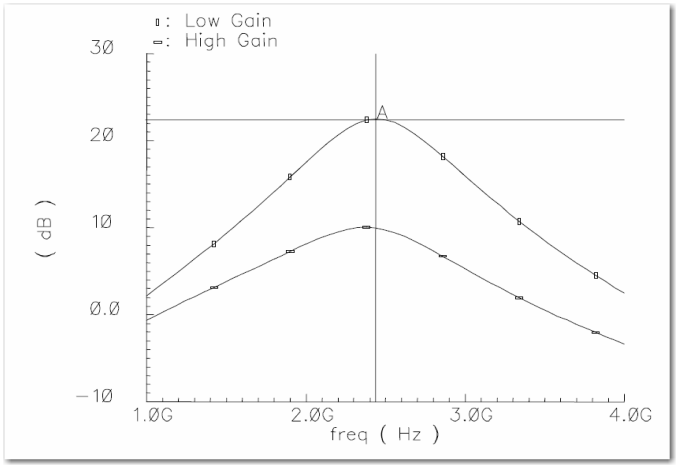

Fig 13.3 Available power gain (G_A) for low and high gain modes for 2.45 GHz LNA

C. Noise Figure:

The noise figure of the LNA has to be the smallest in the chain since it needs to amplify a very weak signal without adding noise to it. The noise figure characteristic is shown below:

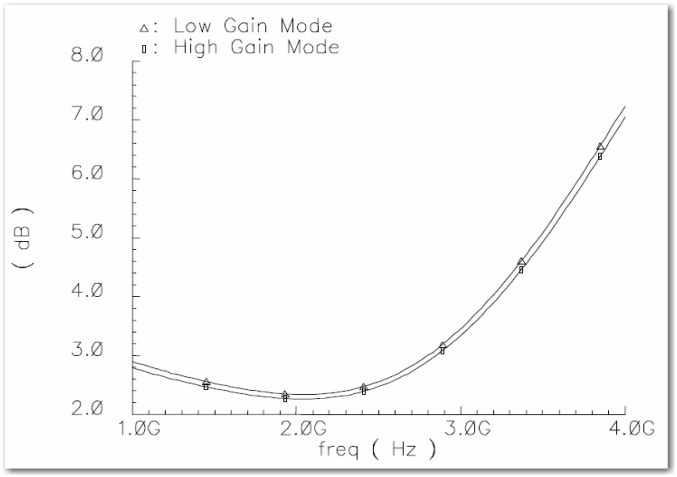

Fig 13.4. Noise Figure (NF) for 2.45 GHz LNA

D. IIP3:

The IIP3 of the LNA needs to be the maximum in order to alleviate linearity requirements for succeeding stages. The IIP3 characteristic is shown on the next page, along with the LNA performance summary. From the summary, we see that the all of the performance specs are met except for NF which is slightly greater than 2 dB. Note that the tests have been performed for the typical (TT) corner, with supply voltage set to 1.8 V and temperature equal to 27°C.

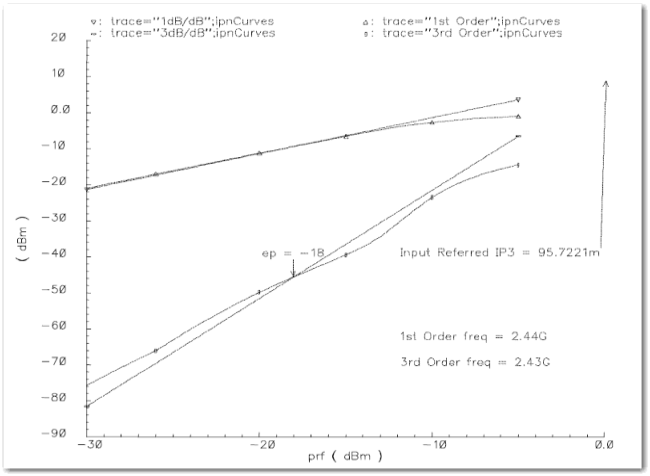

Fig 13.5. IIP3 for 2.45 GHz LNA

Table 13.1 2.45 GHz LNA performance summary

Parameter	Measured	Requirements
S11 (dB)	-17.4	> -10 dB
S12 (dB)	-46.2	N/A
NF (dB) (High gain)	2.05	< 2 dB
NF (dB) (Low gain)	2.2	N/A
Overall gain (dB) (High gain)	22	>= 20dB
Overall gain (dB) (Low gain)	10.2	>= 8dB
IIP3 (dBm)	0.95	>= 0 dB
IIP2 (dBm)	20.8	N/A
Supply Voltage	1.8	N/A
DC Current (mA)	3.18	N/A
Power (mW)	5.724	< 6 mW

XIV. CONCLUSION

In this first part of the paper, the design of a Bluetooth receiver was described along with the subdivision of the specs along the RX chain. The main criteria kept in mind were the overall gain, IIP3, IIP2 and noise figure, amongst others. In the second part, the design and implementation of a 2.45 GHz narrowband LNA using 0.13 µm CMOS technology in Cadence was described, along with the simulation results for the same. It is hoped that this paper would prove to be a useful reference for others who wish to look for a starting point for designing for various wireless standards.

XIV. REFERENCES

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