Lab4 Intro
Creating a Processor System

Vivado HLS 2013.3 Version
ZedBoard

Objectives

- **After completing this lab, you will be able to:**
  - Understand the steps and directives involved in creating a IP-XACT adapter from a synthesized design in Vivado HLS
  - Create a processor system using IP Integrator in Vivado
  - Integrate the generated IP-XACT adapter into the created processor system

The Design

- The design consists of a FIR filter to filter a 4 KHz tone added to a CD quality (48 KHz) music. This lab requires you to develop a peripheral core of the designed filter that can be instantiated in a processor system. The processor system will acquire a stereo music using on-board ADAU1761 CODEC chip from Analog Devices and I^2S controller, process (bandstop filter) it through the designed filter, and output back to the speaker

Procedure

- Create a Vivado HLS project for the FIR filter
- Run simulation and verify functionality
- Synthesize the design
- Run RTL/C Co-simulation
- Setup IP-XACT adapter
- Generate the IP-XACT adapter
- Create a Vivado project
- Generate bitstream and export to SDK
- Generate an application
- Verify in hardware

Summary

- In this lab, you added RESOURCE directive to create an IP-XACT adapter. You generated the IP-XACT adapter. You then created a processor system using IP Integrator, integrated the generated ip core, and tested the system with the provided application