# Convolutional Neural Networks

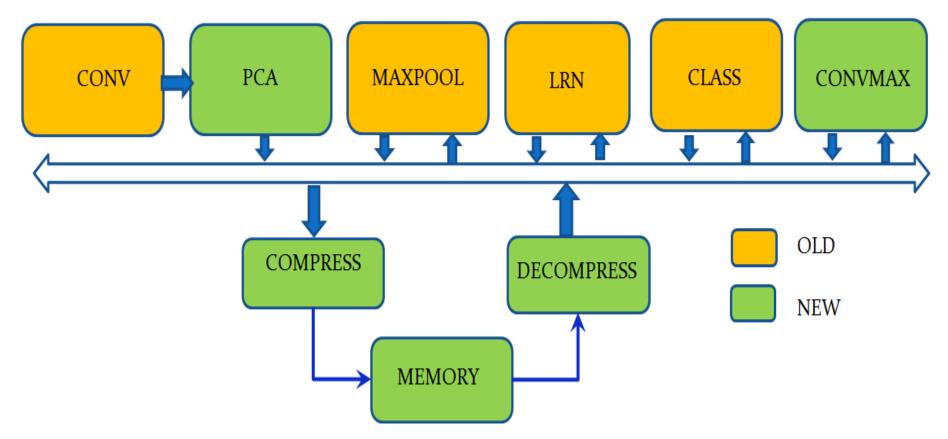
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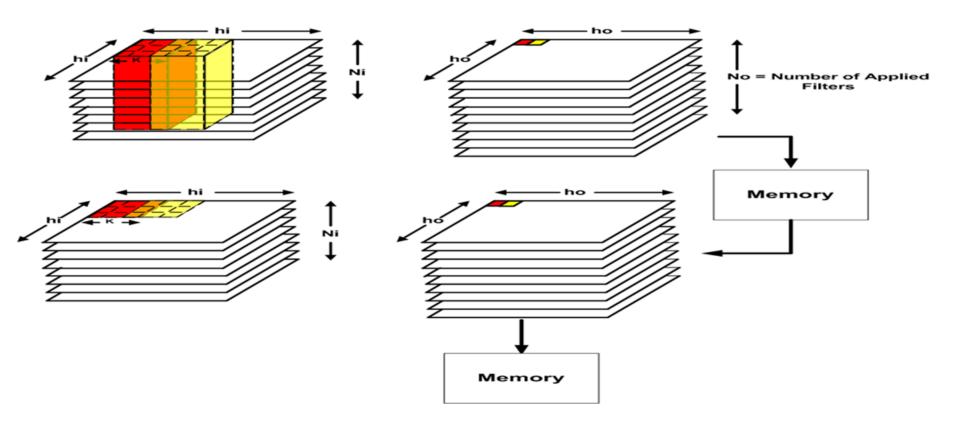
#### **Agenda**

- Computational Modules
- Increasing system parallelism
- Memory Architecture
- Discussion

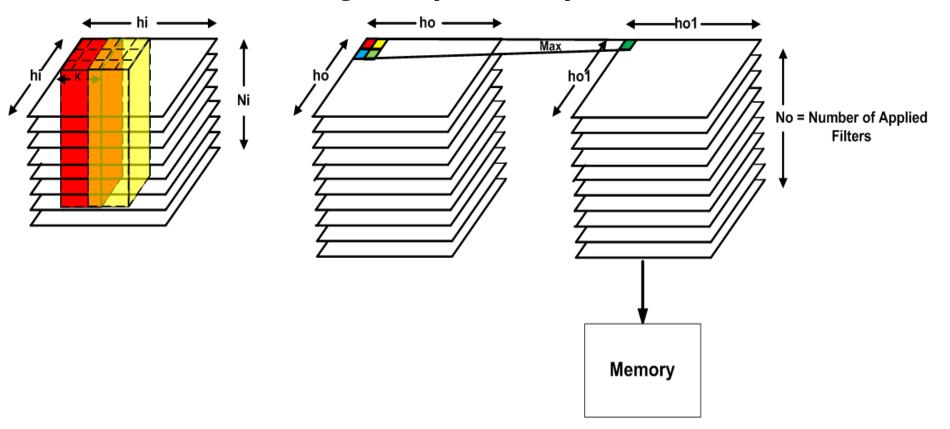
## **System-Level Diagram**



# ConvMax Layer



#### ConvMax Layer (Cont.)



# ConvMax Layer (Cont.)

Directives	Estimated	Latency	Latency	Interval	Interval	BRAM_18K	DSP48E	FF	LUT
	Clock	Min	Max	Min	Max				
No Directive	8.09	227	227	228	228	0	5	903	1944
Outer Loop Pipeline + Data flow	8.09	53	53	41	41	0	5	1595	1446
Outer Loop Pipeline	8.63	65	65	66	66	0	5	1134	1515
Outer Loop Pipeline + Data flow + Intermediate Array partition	8.63	51	51	40	40	0	5	1861	2776

# **Caffe GPU implementation**

1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1	1		2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1			2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1				2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1	1		2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1	1		2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9

 $20 \times 20 = 400$ 

1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	2	2	1	1	2	2	1	1	2	2	1	1	2	2
2	2	3	3	2	2	3	3	2	2	3	3	2	2	3	3
3	3	4	4	3	3	4	4	3	3	4	4	3	3	4	4
4	4	5	5	4	4	5	5	4	4	5	5	4	4	5	5
5	5	6	6	5	5	6	6	5	5	6	6	5	5	6	6
6	6	7	7	6	6	7	7	6	6	7	7	6	6	7	7
7	7	8	8	7	7	8	8	7	7	8	8	7	7	8	8
8	8	9	9	8	8	9	9	8	8	9	9	8	8	9	9
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	2	2	1	1	2	2	1	1	2	2	1	1	2	2
2	2	3	3	2	2	3	3	2	2	3	3	2	2	3	3
3	3	4	4	3	3	4	4	3	3	4	4	3	3	4	4
4	4	5	5	4	4	5	5	4	4	5	5	4	4	5	5
5	5	6	6	5	5	6	6	5	5	6	6	5	5	6	6
6	6	7	7	6	6	7	7	6	6	7	7	6	6	7	7
7	7	8	8	7	7	8	8	7	7	8	8	7	7	8	8
8	8	9	9	8	8	9	9	8	8	9	9	8	8	9	9
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	2	2	1	1	2	2	1	1	2	2	1	1	2	2
2	2	3	3	2	2	3	3	2	2	3	3	2	2	3	3
3	3	4	4	3	3	4	4	3	3	4	4	3	3	4	4
4	4	5	5	4	4	5	5	4	4	5	5	4	4	5	5
5	5	6	6	5	5	6	6	5	5	6	6	5	5	6	6
6	6	7	7	6	6	7	7	6	6	7	7	6	6	7	7
7	7	8	8	7	7	8	8	7	7	8	8	7	7	8	8
8	8	9	9	8	8	9	9	8	8	9	9	8	8	9	9





# **Extending parallelism**

1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	7	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
1	1	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	
																				]
	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1			1 1 1 1 2 2 3 1 1 1 1 1 2 2 3 1 1 1 1 1 2 2 3 1 1 1 1 1 2 2 3	1 1 1 1 2 2 3 3 1 1 1 1 1 2 2 3 3 1 1 1 1 1 2 2 3 3 1 1 1 1 1 2 2 3 3	1 1 1 1 2 2 3 3 4 1 1 1 1 2 2 3 3 4 1 1 1 1 2 2 3 3 4 1 1 1 1 2 2 3 3 4	1 1 1 1 2 2 3 3 4 4 1 1 1 1 2 2 3 3 4 4 1 1 1 1 2 2 3 3 4 4 1 1 1 1 2 2 3 3 4 4	1 1 1 1 2 2 3 3 4 4 5 1 1 1 1 2 2 3 3 4 4 5 1 1 1 1 2 2 3 3 4 4 5 1 1 1 1 2 2 3 3 4 4 5 1 1 1 1 2 2 3 3 4 4 5 1 1 1 1 2 2 3 3 4 4 5	1 1 1 1 2 2 3 3 4 4 5 5 1 1 1 1 2 2 3 3 4 4 5 5 1 1 1 1 2 2 3 3 4 4 5 5 1 1 1 1 2 2 3 3 4 4 5 5 1 1 1 1 2 2 3 3 4 4 5 5 1 1 1 1 2 2 3 3 4 4 5 5	1   1   1   1   2   2   3   3   4   4   5   5   6     1   1   1   1   2   2   3   3   4   4   5   5   6     1   1   1   1   2   2   3   3   4   4   5   5   6     1   1   1   1   2   2   3   3   4   4   5   5   6     1   1   1   1   2   2   3   3   4   4   5   5   6     1   1   1   1   2   2   3   3   4   4   5   5   6     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 1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7 <th>1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8     1   1   1   1   2   2   3   3   4   4   &lt;</th> <th>1   1   1   1   2   2   3   3   4   4   5   5   6   6   7   7   8   8     1   1   1   1   2   2   3   3   4   4   5   5   6   6   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#### **Memory Interface**

- This is a programmable interface.
- Each module has an interface associated with it.
- The interface accesses the memory, retrieves the data and passes it on to the module.
- Similarly it can access the memory to write the output of the module.

#### Continue ...

- The controller programs the starting and ending address of the memory for each interface.
- The handshaking requires monitoring the valid bit set at the starting address by the preceding module.
- Upon accessing the data, the bit is cleared by the succeeding block.

## **Memory diagram**

#### Valid bit



#### Continue ...

 This allows preceding block to write the new output to the same address if required.

## Synthesis results

#### Performance Estimates

Timing (ns)

Clock		solution1	solution2
default	Target	10.00	10.00
	Estimated	7.22	6.92

Latency (clock cycles)

		solution1	solution2
Latency	main	5	5
	max	11	9
Interval	min	6	6
	max	12	10

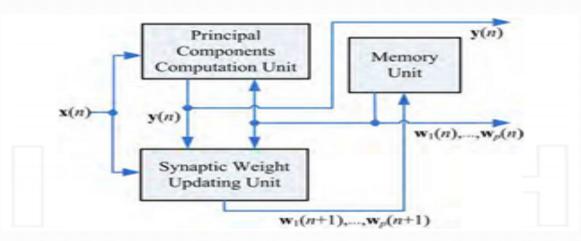
#### Cont ...

#### **Utilization Estimates**

	solutionl	solution2
BRAM_18K	0	0
DSP48E	0	0
FF	83	102
LUT	325	409

#### PCA proposed architecture

#### Proposed architecture



From: http://cdn.intechopen.com/pdfs-wm/30440.pdf

#### Time plan

- □ System Integration (Computational modules
  - + Memory) (May -10)
- Development of test suite to measure system performance (May 20)
- □ Replication of computational modules to extend parallelism (May - 31)