High-Level Synthesis using Vivado HLS
Course Intro

Vivado HLS 2013.3 Version

Course Objectives

- **After completing this course, you will be able to:**
  - Describe the high level synthesis flow
  - Understand the control and datapath extraction
  - Describe scheduling and binding phases of the HLS flow
  - Identify steps involved in validation and verification flows
  - State various directives which can be helpful in improving performance and resource utilization
  - Describe how to use OpenCV functions in the Vivado HLS tool
  - Perform system-level integration of blocks generated by the Vivado HLS tool

Course Outline
Day 1

The course consists of the following modules:

- Introduction to High-Level Synthesis (HLS)
- Using Vivado HLS
- Lab 1: Creating Project and Understanding Reports
- Improving Performance
- Lab 2: Optimizing Performance through Pipelining
- Data Types

Course Outline
Day 2

- Improving Area and Resources Utilization
- Lab 3: Improving Area and Resources Utilization
- Handling Block- and Ports- Level Protocols
- Coding Considerations
- Creating a Processor System
- Lab 4: Creating a Processor System to filter Audio Signal

Prerequisites

- Familiarity with the Xilinx Vivado Design Suite tool set
- Basic C programming
- Basic understanding of a processor-based system

Platform Support

- **Vivado Design Suite: System Edition HLS 2013.3**
- **Xilinx University board**
  - ZedBoard
- **Supported Operating Systems**
  - Windows XP (SP2) (32/64 Bit)
  - Windows 7 Professional (32/64 Bit)
  - Red Hat Enterprise Linux 4 (32/64 Bit)
  - SUSE Linux Enterprise (32/64 Bit)