A PROJECT REPORT

On

Implementation of High-Speed Constant Multiplication

Submitted in partial fulfillment of the requirement for

The award of the Degree of

BACHELOR OF TECHNOLOGY

In

ELECTRONICS AND COMMUNICATION ENGINEERING

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CERTIFICATE

This is to certify that the project report entitled "IMPLEMENTATION OF HIGH-SPEED CONSTANT MULTIPLICATION" being submitted by N. SANDEEP SAI (15JN1A0493) K. G. N. SAI SRIRAM (15JN1A0475), M. SASI KUMAR (15JN1A0487), P. PRADEEP (15JN1A04A8), M. RAVI KUMAR (15JN1A0478) in partial fulfillment for the award of the award of the Degree of BACHELOR OF TECHNOLOGY in ELECTRONICS AND COMMUNICATION ENGINEERING to the Jawaharlal Nehru Technological University Ananthapuramu, is a record of bonafied work carried out under my guidance and supervision. The results embodied in this project report have not been submitted to any other University or Institute for the award of any degree.

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We hereby declare that the project report entitled, "IMPLEMENTATION OF HIGH-SPEED CONSTANT MULTIPLICATION" completed and written by us has not been previously formed the basis for the award of any degree certificate.

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ACKNOWLEDGEMENT

We take our project guide, **MR. P. ANIL KUMAR,** for his guidance, valuable suggestions and support in the completion of the project.

We take this opportunity to express our cordial and gratitude and deep sense of indebtness to our project guide Asst. Prof. Mr. P. ANIL KUMAR for the valuable guidance and his kind and whole hearted support to us. We feel thankful to him for his innovative ideas, which lead to the successful completion of our project work.

We owe our guidance to our beloved head of the department of "**ELECTRONICS AND COMMUNICATION ENGINEERING" P. GIRI PRASAD**, for his timely help, encouragement and interest in this work.

We owe our guidance to our beloved principal **Dr. S. V. PADMAJARANI**, for her timely help, encouragement and interest in this work.

We are thankful to our beloved chairman **Sri Dr. P. BABU NAIDU** who took keen interest and encouraged us in every effort throughout this course.

In conclusion, we express my sincere thanks to teaching staff, lab assistants, classmates and friends who have helped us either directly or indirectly in carrying out this project work and especially to our parents who helped us thoroughly for shaping out the things well in order.

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ABSTRACT

FPGA contains the limited resources such as limited multipliers, look up tables, memory and DSP blocks. Operations such as FIR and FFT contains a large number of multipliers. The major theme of this project is to implement a reconfigurable multiplier based on the Look up tables which saves a lot of resources.

By using the proposed method, it reduces the run-time of the fusion process, which raises the usability and application domain of the proposed method of run-time reconfiguration. It introduces a new approach to generate pipelined run-time reconfigurable constant multipliers for field programmable gate arrays (FPGAs). It produces results close to the optimum. It is based on an optimal algorithm which fuses already optimized pipelined constant multipliers generated by an existing heuristic called reduced pipelined adder graph (RPAG). It searches for solutions that result in minimal multiplexer overhead. An extensive evaluation of the proposed method confirms a FPGA resource reduction on average compared to previous work. Switching between given set of constants of such multipliers is important to realize hardware efficient run time adaptable filters. Two low level optimizations are presented, which further reduce resource consumption and are included into an automatic VHDL code generation.

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