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Release 14.7 Trace  (nt64)
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C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3
-n 3 -fastpaths -xml Digital_Clock_12_hrFomrat.twx
Digital_Clock_12_hrFomrat.ncd -o Digital_Clock_12_hrFomrat.twr
Digital_Clock_12_hrFomrat.pcf

Design file:              Digital_Clock_12_hrFomrat.ncd
Physical constraint file: Digital_Clock_12_hrFomrat.pcf
Device,package,speed:     xc7a100t,fgg484,C,-3 (PRODUCTION 1.10 2013-10-13)
Report level:             verbose report

Environment Variable      Effect
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NONE                      No environment variables were set
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INFO:Timing:2698 - No timing constraints found, doing default enumeration.
INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
   option. All paths that are not constrained will be reported in the
   unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.
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Data Sheet report:

All values displayed in nanoseconds (ns)

Setup/Hold to clock clk

Source	Max Setup to clk (edge)	Process Corner	Max Hold to clk (edge)	Process Corner	Internal Clock(s)	Clock Phase
center	0.694(R)	SLOW	1.426(R)	SLOW	clk_BUFGP	0.000
down	1.073(R)	FAST	1.761(R)	SLOW	clk_BUFGP	0.000
left	0.047(R)	FAST	1.510(R)	SLOW	clk_BUFGP	0.000
right	0.065(R)	FAST	1.701(R)	SLOW	clk_BUFGP	0.000
up	0.509(R)	FAST	1.313(R)	SLOW	clk_BUFGP	0.000

Clock clk to Pad

| | Max (slowest) clk | Process | Min (fastest) clk | Process |

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|                       | Clock   |
Destination            | (edge) to PAD |   Corner  | (edge) to PAD |   Corner
|Internal Clock(s) | Phase   |
-----------------------+---------------+-----------+---------------+-----------+-----
-------------+--------+
AMPM_indicator_led     |        8.679(R)|    SLOW   |        3.811(R)|    FAST
|clk_BUFGP         |   0.000|
an<0>                  |        7.970(R)|    SLOW   |        3.350(R)|    FAST
|clk_BUFGP         |   0.000|
an<1>                  |        7.799(R)|    SLOW   |        3.267(R)|    FAST
|clk_BUFGP         |   0.000|
an<2>                  |        7.974(R)|    SLOW   |        3.344(R)|    FAST
|clk_BUFGP         |   0.000|
an<3>                  |        7.806(R)|    SLOW   |        3.278(R)|    FAST
|clk_BUFGP         |   0.000|
clock_mode_indicator_led|       8.833(R)|    SLOW   |        3.908(R)|    FAST
|clk_BUFGP         |   0.000|
seg<0>                 |        9.120(R)|    SLOW   |        4.031(R)|    FAST
|clk_BUFGP         |   0.000|
seg<1>                 |        9.157(R)|    SLOW   |        4.041(R)|    FAST
|clk_BUFGP         |   0.000|
seg<2>                 |        8.492(R)|    SLOW   |        3.719(R)|    FAST
|clk_BUFGP         |   0.000|
seg<3>                 |        9.303(R)|    SLOW   |        4.153(R)|    FAST
|clk_BUFGP         |   0.000|
seg<4>                 |        9.341(R)|    SLOW   |        4.141(R)|    FAST
|clk_BUFGP         |   0.000|
seg<5>                 |        9.175(R)|    SLOW   |        4.048(R)|    FAST
|clk_BUFGP         |   0.000|
seg<6>                 |        8.646(R)|    SLOW   |        3.793(R)|    FAST
|clk_BUFGP         |   0.000|
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-------------+--------+


Clock to Setup on destination clock clk
--------------+---------+---------+---------+---------+
              | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock  |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
--------------+---------+---------+---------+---------+
clk           |   3.075|         |         |         |
--------------+---------+---------+---------+---------+


Analysis completed Sun Mar 21 18:07:14 2021
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Trace Settings:
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Trace Settings

Peak Memory Usage: 5003 MB
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