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Xilinx XPower
Analyzer
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| Release                | 14.7 - P.20131013
(nt64)
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| Command Line           | C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\xpwr.exe -intstyle
ise -ol std Digital_Clock_12_hrFomrat.ncd Digital_Clock_12_hrFomrat.pcf -o
Digital_Clock_12_hrFomrat.pwr  |
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1. Settings

1.1. Project

Project	
Design File	Digital_Clock_12_hrFomrat.ncd
Settings File	NA
Physical Constraints File	Digital_Clock_12_hrFomrat.pcf
Simulation Activity File	NA
Design Nets Matched	NA
Simulation Nets Matched	NA

1.2. Device

Device	
Family	Artix7
Part	xc7a100t
Package	fgg484
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Characterization	Production,v1.0,2012-07-11

1.3. Environment

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

1.4. Default Activity Rates

Default Activity Rates	
FF Toggle Rate (%)	12.5
I/O Toggle Rate (%)	12.5
Output Load (pF)	5.0
I/O Enable Rate (%)	100.0
BRAM Write Rate (%)	50.0
BRAM Enable Rate (%)	50.0
DSP Toggle Rate (%)	12.5

2. Summary

2.1. On-Chip Power Summary

On-Chip Power Summary					
On-Chip	Power (mW)	Used	Available	Utilization (%)	
Clocks	0.00	1	---	---	
Logic	0.00	248	63400	0	
Signals	0.00	239	---	---	
IOs	0.00	21	285	7	
Static Power	82.05				
Total	82.05				

2.2. Thermal Summary

Thermal Summary	
Effective TJA (C/W)	2.8
Max Ambient (C)	84.8
Junction Temp (C)	25.2

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Static Power

| Supply Power (mW) | 82.05 | 0.00 | 82.05 |

| Power Supply Currents |

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.000	16.64	0.00	16.64
Vccaux	1.800	13.14	0.00	13.14
Vcco18	1.800	4.00	0.00	4.00
Vccbram	1.000	0.35	0.00	0.35
Vccadc	1.710	20.00	0.00	20.00

2.4. Confidence Level

Confidence Level	User Input Data	Confidence	Details	Action
	Design implementation state	High	Design is completely routed	
	Clock nodes activity	High	User specified more than 95% of clocks	
	I/O nodes activity	High	User specified more than 95% of inputs	
	Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
	Device models	High	Device models are Production	

Overall confidence level	Medium

3. Details

3.1. By Hierarchy

By Hierarchy	Power (mW)	Logic Power (mW)	Signal Power (mW)	# FFs	# LUTs	# CARRY4s
Hierarchy total	0.00	0.00	0.00	112	209	14
Digital_Clock_12_hrFomrat	0.00	0.00	0.00	54 / 112	125 / 209	9 / 14
SSM	0.00	0.00	0.00	58	76	5
sec[5]_PWR_1_o_mod_62	0.00	0.00	0.00	0	4	0
min[5]_PWR_1_o_mod_60	0.00	0.00	0.00	0	4	0

4. Warnings

WARNING:PowerEstimator:270 - Power estimate is considered inaccurate. To see details, generate an advanced report with the "-v" switch.
WARNING:Power:1337 - Clock frequency for clock net "clk_BUFGP" is zero.
WARNING:Power:1337 - Clock frequency for clock net "clk_BUFGP/IBUFG" is zero.
WARNING:Power:1369 - Clock frequency for one or more clocks was not found through timing constraints (PCF file) or simulation data. Without knowing the clock frequency of all clocks, dynamic power information for those clock domains will default to zero which may under-estimate the power for this design. To avoid this warning, provide at least one of the following:

1. The proper timing constraints (PERIOD) for clocks (re-implement design and load the newly generated PCF file into XPower Analyzer)
2. A post PAR simulation-generated VCD or SAIF file indicating clock frequencies
3. The clock frequency for clocks in the "By Type -> Clocks" view in the XPower Analyzer GUI and then applying "Update Power Analysis"

Analysis completed: Sun Mar 21 18:14:41 2021