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Release 14.7 par P.20131013 (nt64)
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DESKTOP-7L7738E::  Sun Mar 21 18:06:39 2021

par -w -intstyle ise -ol high -mt off Digital_Clock_12_hrFomrat_map.ncd
Digital_Clock_12_hrFomrat.ncd Digital_Clock_12_hrFomrat.pcf


Constraints file: Digital_Clock_12_hrFomrat.pcf.
Loading device for application Rf_Device from file '7a100t.nph' in environment
C:\Xilinx\14.7\ISE_DS\ISE\.
   "Digital_Clock_12_hrFomrat" is an NCD, version 3.2, device xc7a100t, package fgg484,
speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to
ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically
improve the performance of all
   internal clocks in this design. Because there are not defined timing requirements, a
timing score will not be
   reported in the PAR report in this mode. The PAR timing summary will list the
performance achieved for each clock.
   Note: For the fastest runtime, set the effort level to "std".  For best performance,
set the effort level to "high".

Device speed data version:  "PRODUCTION 1.10 2013-10-13".



Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers:                   112 out of 126,800    1%
    Number used as Flip Flops:                 112
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                        248 out of  63,400    1%
    Number used as logic:                      225 out of  63,400    1%
      Number using O6 output only:             162
      Number using O5 output only:              35
      Number using O5 and O6:                   28
      Number used as ROM:                        0
    Number used as Memory:                       0 out of  19,000    0%
    Number used exclusively as route-thrus:     23
      Number with same-slice register load:      0
      Number with same-slice carry load:         2
      Number with other load:                   21

Slice Logic Distribution:
  Number of occupied Slices:                    90 out of  15,850    1%
  Number of LUT Flip Flop pairs used:          270
    Number with an unused Flip Flop:           166 out of     270   61%
    Number with an unused LUT:                  22 out of     270    8%
    Number of fully used LUT-FF pairs:          82 out of     270   30%
    Number of slice register sites lost
      to control set restrictions:               0 out of 126,800    0%
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  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:
  Number of bonded IOBs:                        21 out of     285    7%

Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                  0 out of     135    0%
  Number of RAMB18E1/FIFO18E1s:                  0 out of     270    0%
  Number of BUFG/BUFGCTRLs:                      1 out of      32    3%
    Number used as BUFGs:                        1
    Number used as BUFGCTRLs:                    0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:        0 out of     300    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:        0 out of     300    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:        0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:        1 out of     300    1%
    Number used as OLOGICE2s:                    1
    Number used as OLOGICE3s:                    0
    Number used as OSERDESE2s:                   0
  Number of PHASER_IN/PHASER_IN_PHYs:            0 out of      24    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:          0 out of      24    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      96    0%
  Number of BUFRs:                               0 out of      24    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DNA_PORTs:                           0 out of       1    0%
  Number of DSP48E1s:                            0 out of     240    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of GTPE2_CHANNELs:                      0 out of       4    0%
  Number of IBUFDS_GTE2s:                        0 out of       4    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       6    0%
  Number of IN_FIFOs:                            0 out of      24    0%
  Number of MMCME2_ADVs:                         0 out of       6    0%
  Number of OUT_FIFOs:                           0 out of      24    0%
  Number of PCIE_2_1s:                           0 out of       1    0%
  Number of PHASER_REFs:                         0 out of       6    0%
  Number of PHY_CONTROLs:                        0 out of       6    0%
  Number of PLLE2_ADVs:                          0 out of       6    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of XADCs:                               0 out of       1    0%


Overall effort level (-ol):   High
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 12 secs
Finished initial Timing Analysis.  REAL time: 12 secs

Starting Router


Phase  1  : 1254 unrouted;      REAL time: 13 secs
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Phase  2  : 1080 unrouted;      REAL time: 14 secs

Phase  3  : 202 unrouted;      REAL time: 14 secs

Phase  4  : 202 unrouted; (Par is working to improve performance)     REAL time: 18 secs

Updating file: Digital_Clock_12_hrFomrat.ncd with current fully routed design.

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 19 secs

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 19 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 19 secs

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 19 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 19 secs
Total REAL time to Router completion: 19 secs
Total CPU time to Router completion: 19 secs

Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.
INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.
Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (*) preceding a constraint indicates it was not met.
   This may be due to a setup or hold violation.

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  Constraint                                |    Check    | Worst Case |  Best Case |
Timing |   Timing
                                            |             |    Slack   | Achievable |
Errors |    Score
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  Autotimespec constraint for clock net clk | SETUP       |         N/A|     3.075ns|
N/A|           0
  _BUFGP                                    | HOLD        |     0.159ns|
|       0|           0
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All constraints were met.
INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the
   constraint is not analyzed due to the following: No paths covered by this
   constraint; Other constraints intersect with this constraint; or This
   constraint was disabled by a Path Tracing Control. Please run the Timespec
   Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.


Generating Pad Report.

All signals are completely routed.
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Total REAL time to PAR completion: 19 secs
Total CPU time to PAR completion: 19 secs

Peak Memory Usage:  4846 MB

Placer: Placement generated during map.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 2

Writing design to file Digital_Clock_12_hrFomrat.ncd



PAR done!
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