Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.14 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.14 secs

--> Reading design: Digital_Clock_12_hrFomrat.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "Digital_Clock_12_hrFomrat.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "Digital_Clock_12_hrFomrat"
Output Format   : NGC
Target Device   : xc7a100t-3-fgg484

---- Source Options
Top Module Name   : Digital_Clock_12_hrFomrat
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 32
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v" into
library work
Parsing module <SSM_Seven_Segment_Module>.
Analyzing Verilog file "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v" into
library work
Parsing module <Digital_Clock_12_hrFomrat>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <Digital_Clock_12_hrFomrat>.

Elaborating module <SSM_Seven_Segment_Module>.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v" Line
```

```
56: Result of 20-bit expression is truncated to fit in 19-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v" Line
59: Result of 3-bit expression is truncated to fit in 2-bit target.
WARNING:HDLCompiler:295 - "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v" Line
104: case condition never applies
WARNING:HDLCompiler:295 - "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v" Line
109: case condition never applies
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 77: Result of 7-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 96: Result of 7-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 100: Result of 32-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 102: Result of 32-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 118: Result of 7-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 123: Result of 32-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 146: Result of 7-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 150: Result of 7-bit expression is truncated to fit in 6-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 160: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 162: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 164: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 172: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 174: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 183: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 194: Result of 6-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 200: Result of 5-bit expression is truncated to fit in 4-bit target.
WARNING:HDLCompiler:413 - "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v"
Line 201: Result of 6-bit expression is truncated to fit in 4-bit target.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <Digital_Clock_12_hrFomrat>.
    Related source file is "C:/Users/Masth/Downloads/Digital_Clock_12_hrs_format (3).v".
        max_count = 625000
        display_time = 1'b0
        set_time = 1'b1
    Found 1-bit register for signal <current_mode>.
    Found 32-bit register for signal <counter>.
    Found 6-bit register for signal <hrs>.
    Found 1-bit register for signal <toggle>.
    Found 6-bit register for signal <min>.
    Found 6-bit register for signal <sec>.
    Found 4-bit register for signal <min_ones>.
    Found 4-bit register for signal <min_tens>.
    Found 4-bit register for signal <sec_ones>.
    Found 4-bit register for signal <sec_tens>.
```

```
    Found 4-bit register for signal <hrs_ones>.
    Found 4-bit register for signal <hrs_tens>.
    Found 1-bit register for signal <AMPM_indicator_led>.
    Found 1-bit register for signal <clock_mode_indicator_led>.
    Found 6-bit adder for signal <sec[5]_GND_1_o_add_5_OUT> created at line 77.
    Found 32-bit adder for signal <counter[31]_GND_1_o_add_9_OUT> created at line 90.
    Found 6-bit adder for signal <min[5]_GND_1_o_add_10_OUT> created at line 96.
    Found 6-bit adder for signal <hrs[5]_GND_1_o_add_25_OUT> created at line 118.
    Found 6-bit subtractor for signal <GND_1_o_GND_1_o_sub_14_OUT<5:0>> created at line 100.
    Found 6-bit subtractor for signal <GND_1_o_GND_1_o_sub_29_OUT<5:0>> created at line 123.
    Found 32-bit comparator greater for signal <counter[31]_GND_1_o_LessThan_4_o> created
at line 73
    Found 32-bit comparator greater for signal <counter[31]_GND_1_o_LessThan_9_o> created
at line 88
    Found 6-bit comparator greater for signal <GND_1_o_hrs[5]_LessThan_28_o> created at
line 121
    Found 6-bit comparator greater for signal <n0051> created at line 144
    Found 6-bit comparator greater for signal <n0055> created at line 148
    Found 6-bit comparator greater for signal <n0059> created at line 152
    Found 6-bit comparator greater for signal <GND_1_o_hrs[5]_LessThan_60_o> created at
line 165
    Found 6-bit comparator greater for signal <hrs[5]_GND_1_o_LessThan_65_o> created at
line 175
    Found 6-bit comparator greater for signal <hrs[5]_GND_1_o_LessThan_75_o> created at
line 192
    Summary:
        inferred   6 Adder/Subtractor(s).
        inferred  78 D-type flip-flop(s).
        inferred   9 Comparator(s).
        inferred  13 Multiplexer(s).
Unit <Digital_Clock_12_hrFomrat> synthesized.

Synthesizing Unit <SSM_Seven_Segment_Module>.
    Related source file is "C:/Users/Masth/Downloads/SSM_Seven_Segment_Module (2).v".
        max_count = 500000
WARNING:Xst:647 - Input <hrs_ones> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <hrs_tens> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
    Found 2-bit register for signal <digit_display>.
    Found 28-bit register for signal <n0092>.
    Found 6-bit register for signal <an>.
    Found 7-bit register for signal <seg>.
    Found 19-bit register for signal <counter>.
    Found 19-bit adder for signal <counter[18]_GND_2_o_add_8_OUT> created at line 56.
    Found 2-bit adder for signal <digit_display[1]_GND_2_o_add_9_OUT> created at line 59.
    Found 4x6-bit Read Only RAM for signal <digit_display[1]_PWR_2_o_wide_mux_94_OUT>
    Found 28-bit 16-to-1 multiplexer for signal
<digit_display[1]_display[3][6]_wide_mux_93_OUT> created at line 63.
    Found 7-bit 4-to-1 multiplexer for signal
<digit_display[1]_display[3][6]_wide_mux_95_OUT> created at line 83.
    Found 1-bit 4-to-1 multiplexer for signal
<digit_display[1]_four_bit[3][3]_wide_mux_12_OUT<3>> created at line 63.
    Found 1-bit 4-to-1 multiplexer for signal
<digit_display[1]_four_bit[3][3]_wide_mux_12_OUT<2>> created at line 63.
    Found 1-bit 4-to-1 multiplexer for signal
<digit_display[1]_four_bit[3][3]_wide_mux_12_OUT<1>> created at line 63.
    Found 1-bit 4-to-1 multiplexer for signal
<digit_display[1]_four_bit[3][3]_wide_mux_12_OUT<0>> created at line 63.
```

```
    Found 19-bit comparator greater for signal <counter[18]_PWR_2_o_LessThan_8_o> created
at line 55
    Summary:
        inferred   1 RAM(s).
        inferred   2 Adder/Subtractor(s).
        inferred  62 D-type flip-flop(s).
        inferred   1 Comparator(s).
        inferred  70 Multiplexer(s).
Unit <SSM_Seven_Segment_Module> synthesized.

Synthesizing Unit <mod_6u_4u>.
    Related source file is "".
    Found 10-bit adder for signal <n0165> created at line 0.
    Found 10-bit adder for signal <GND_3_o_b[3]_add_1_OUT> created at line 0.
    Found 9-bit adder for signal <n0169> created at line 0.
    Found 9-bit adder for signal <GND_3_o_b[3]_add_3_OUT> created at line 0.
    Found 8-bit adder for signal <n0173> created at line 0.
    Found 8-bit adder for signal <GND_3_o_b[3]_add_5_OUT> created at line 0.
    Found 7-bit adder for signal <n0177> created at line 0.
    Found 7-bit adder for signal <GND_3_o_b[3]_add_7_OUT> created at line 0.
    Found 6-bit adder for signal <n0181> created at line 0.
    Found 6-bit adder for signal <a[5]_b[3]_add_9_OUT> created at line 0.
    Found 6-bit adder for signal <n0185> created at line 0.
    Found 6-bit adder for signal <a[5]_GND_3_o_add_11_OUT> created at line 0.
    Found 6-bit adder for signal <n0189> created at line 0.
    Found 6-bit adder for signal <a[5]_GND_3_o_add_13_OUT> created at line 0.
    Found 10-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 9-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 8-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 7-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0007> created at line 0
    Summary:
        inferred  14 Adder/Subtractor(s).
        inferred   7 Comparator(s).
        inferred  37 Multiplexer(s).
Unit <mod_6u_4u> synthesized.

Synthesizing Unit <div_6u_4u>.
    Related source file is "".
    Found 10-bit adder for signal <n0165> created at line 0.
    Found 10-bit adder for signal <GND_4_o_b[3]_add_1_OUT> created at line 0.
    Found 9-bit adder for signal <n0169> created at line 0.
    Found 9-bit adder for signal <GND_4_o_b[3]_add_3_OUT> created at line 0.
    Found 8-bit adder for signal <n0173> created at line 0.
    Found 8-bit adder for signal <GND_4_o_b[3]_add_5_OUT> created at line 0.
    Found 7-bit adder for signal <n0177> created at line 0.
    Found 7-bit adder for signal <GND_4_o_b[3]_add_7_OUT> created at line 0.
    Found 6-bit adder for signal <n0181> created at line 0.
    Found 6-bit adder for signal <a[5]_b[3]_add_9_OUT[5:0]> created at line 0.
    Found 6-bit adder for signal <n0185> created at line 0.
    Found 6-bit adder for signal <a[5]_GND_4_o_add_11_OUT[5:0]> created at line 0.
    Found 10-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 9-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 8-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 7-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0007> created at line 0
    Summary:
```

```
        inferred  12 Adder/Subtractor(s).
        inferred   7 Comparator(s).
        inferred  21 Multiplexer(s).
Unit <div_6u_4u> synthesized.

Synthesizing Unit <mod_6u_5u>.
    Related source file is "".
    Found 11-bit adder for signal <GND_6_o_b[4]_add_1_OUT> created at line 0.
    Found 10-bit adder for signal <GND_6_o_b[4]_add_3_OUT> created at line 0.
    Found 9-bit adder for signal <GND_6_o_b[4]_add_5_OUT> created at line 0.
    Found 8-bit adder for signal <GND_6_o_b[4]_add_7_OUT> created at line 0.
    Found 7-bit adder for signal <GND_6_o_b[4]_add_9_OUT> created at line 0.
    Found 6-bit adder for signal <a[5]_b[4]_add_11_OUT> created at line 0.
    Found 6-bit adder for signal <a[5]_GND_6_o_add_13_OUT> created at line 0.
    Found 11-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 10-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 9-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 8-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 7-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0007> created at line 0
    Summary:
        inferred   7 Adder/Subtractor(s).
        inferred   7 Comparator(s).
        inferred  37 Multiplexer(s).
Unit <mod_6u_5u> synthesized.

Synthesizing Unit <div_6u_5u>.
    Related source file is "".
    Found 11-bit adder for signal <GND_5_o_b[4]_add_1_OUT> created at line 0.
    Found 10-bit adder for signal <GND_5_o_b[4]_add_3_OUT> created at line 0.
    Found 9-bit adder for signal <GND_5_o_b[4]_add_5_OUT> created at line 0.
    Found 8-bit adder for signal <GND_5_o_b[4]_add_7_OUT> created at line 0.
    Found 7-bit adder for signal <GND_5_o_b[4]_add_9_OUT> created at line 0.
    Found 6-bit adder for signal <a[5]_b[4]_add_11_OUT[5:0]> created at line 0.
    Found 11-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 10-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 9-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 8-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 7-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 6-bit comparator lessequal for signal <BUS_0007> created at line 0
    Summary:
        inferred   6 Adder/Subtractor(s).
        inferred   7 Comparator(s).
        inferred  26 Multiplexer(s).
Unit <div_6u_5u> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 4x6-bit single-port Read Only RAM                     : 1
# Adders/Subtractors                                   : 113
 10-bit adder                                          : 16
 11-bit adder                                          : 2
 19-bit adder                                          : 1
 2-bit adder                                           : 1
 32-bit adder                                          : 1
 6-bit adder                                           : 42
```

```
 6-bit subtractor                                      : 2
 7-bit adder                                           : 16
 8-bit adder                                           : 16
 9-bit adder                                           : 16
# Registers                                            : 19
 1-bit register                                        : 4
 19-bit register                                       : 1
 2-bit register                                        : 1
 28-bit register                                       : 1
 32-bit register                                       : 1
 4-bit register                                        : 6
 6-bit register                                        : 4
 7-bit register                                        : 1
# Comparators                                          : 73
 10-bit comparator lessequal                           : 9
 11-bit comparator lessequal                           : 2
 19-bit comparator greater                             : 1
 32-bit comparator greater                             : 2
 6-bit comparator greater                              : 7
 6-bit comparator lessequal                            : 25
 7-bit comparator lessequal                            : 9
 8-bit comparator lessequal                            : 9
 9-bit comparator lessequal                            : 9
# Multiplexers                                         : 357
 1-bit 2-to-1 multiplexer                              : 258
 1-bit 4-to-1 multiplexer                              : 4
 28-bit 16-to-1 multiplexer                            : 1
 4-bit 2-to-1 multiplexer                              : 9
 5-bit 2-to-1 multiplexer                              : 1
 6-bit 2-to-1 multiplexer                              : 19
 7-bit 2-to-1 multiplexer                              : 64
 7-bit 4-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================

WARNING:Xst:1290 - Hierarchical block <hrs[5]_PWR_1_o_mod_66> is unconnected in block
<Digital_Clock_12_hrFomrat>.
   It will be removed from the design.
WARNING:Xst:1290 - Hierarchical block <hrs[5]_PWR_1_o_div_67> is unconnected in block
<Digital_Clock_12_hrFomrat>.
   It will be removed from the design.
WARNING:Xst:1290 - Hierarchical block <hrs[5]_PWR_1_o_mod_75> is unconnected in block
<Digital_Clock_12_hrFomrat>.
   It will be removed from the design.
WARNING:Xst:1290 - Hierarchical block <hrs[5]_PWR_1_o_mod_77> is unconnected in block
<Digital_Clock_12_hrFomrat>.
   It will be removed from the design.
WARNING:Xst:1290 - Hierarchical block <hrs[5]_PWR_1_o_div_78> is unconnected in block
<Digital_Clock_12_hrFomrat>.
   It will be removed from the design.

Synthesizing (advanced) Unit <Digital_Clock_12_hrFomrat>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
The following registers are absorbed into counter <sec>: 1 register on signal <sec>.
Unit <Digital_Clock_12_hrFomrat> synthesized (advanced).

Synthesizing (advanced) Unit <SSM_Seven_Segment_Module>.
```

```
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
The following registers are absorbed into counter <digit_display>: 1 register on signal
<digit_display>.
INFO:Xst:3231 - The small RAM <Mram_digit_display[1]_PWR_2_o_wide_mux_94_OUT> will be
implemented on LUTs in order to maximize performance and save block RAM resources. If you
want to force its implementation on block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 4-word x 6-bit                      |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <digit_display> |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
Unit <SSM_Seven_Segment_Module> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 4x6-bit single-port distributed Read Only RAM         : 1
# Adders/Subtractors                                   : 63
 4-bit adder carry in                                  : 4
 5-bit adder                                           : 1
 6-bit adder                                           : 14
 6-bit adder carry in                                  : 42
 6-bit subtractor                                      : 2
# Counters                                             : 4
 19-bit up counter                                     : 1
 2-bit up counter                                      : 1
 32-bit up counter                                     : 1
 6-bit up counter                                      : 1
# Registers                                            : 81
 Flip-Flops                                            : 81
# Comparators                                          : 73
 10-bit comparator lessequal                           : 9
 11-bit comparator lessequal                           : 2
 19-bit comparator greater                             : 1
 32-bit comparator greater                             : 2
 6-bit comparator greater                              : 7
 6-bit comparator lessequal                            : 25
 7-bit comparator lessequal                            : 9
 8-bit comparator lessequal                            : 9
 9-bit comparator lessequal                            : 9
# Multiplexers                                         : 357
 1-bit 2-to-1 multiplexer                              : 258
 1-bit 4-to-1 multiplexer                              : 4
 28-bit 16-to-1 multiplexer                            : 1
 4-bit 2-to-1 multiplexer                              : 9
 5-bit 2-to-1 multiplexer                              : 1
 6-bit 2-to-1 multiplexer                              : 19
 7-bit 2-to-1 multiplexer                              : 64
 7-bit 4-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
```

```
=========================================================================
WARNING:Xst:1710 - FF/Latch <an_4> (without init value) has a constant value of 1 in block
<SSM_Seven_Segment_Module>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <an_5> (without init value)
has a constant value of 1 in block <SSM_Seven_Segment_Module>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1710 - FF/Latch <sec_tens_3> (without init value) has a constant value of 0 in
block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization
process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <min_tens_3> (without init
value) has a constant value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will
be trimmed during the optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <hrs_tens_3> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.

Optimizing unit <Digital_Clock_12_hrFomrat> ...

Optimizing unit <SSM_Seven_Segment_Module> ...
WARNING:Xst:2677 - Node <hrs_tens_0> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_tens_1> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_tens_2> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_ones_0> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_ones_1> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_ones_2> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:2677 - Node <hrs_ones_3> of sequential type is unconnected in block
<Digital_Clock_12_hrFomrat>.
WARNING:Xst:1710 - FF/Latch <hrs_5> (without init value) has a constant value of 0 in
block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization
process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_20> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_21> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_22> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_23> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_24> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_25> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_26> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_27> has a constant
value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the
optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_28> has a constant
```

value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_29> has a constant value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_30> has a constant value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1896 - Due to other FF/Latch trimming, FF/Latch <counter_31> has a constant value of 0 in block <Digital_Clock_12_hrFomrat>. This FF/Latch will be trimmed during the optimization process.
INFO:Xst:2261 - The FF/Latch <SSM/display_0_10> in Unit <Digital_Clock_12_hrFomrat> is equivalent to the following FF/Latch, which will be removed : <SSM/display_0_7>
INFO:Xst:2261 - The FF/Latch <SSM/display_0_24> in Unit <Digital_Clock_12_hrFomrat> is equivalent to the following FF/Latch, which will be removed : <SSM/display_0_21>
INFO:Xst:3203 - The FF/Latch <current_mode> in Unit <Digital_Clock_12_hrFomrat> is the opposite to the following FF/Latch, which will be removed : <clock_mode>

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Digital_Clock_12_hrFomrat, actual ratio is 0.

Final Macro Processing ...

===
Final Register Report

Macro Statistics
Registers   : 112
 Flip-Flops   : 112

===

===
*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Design Summary   *
===

Top Level Output File Name   : Digital_Clock_12_hrFomrat.ngc

Primitive and Black Box Usage:

BELS   : 468
GND   : 1
INV   : 5
LUT1   : 37
LUT2   : 18
LUT3   : 32
LUT4   : 48
LUT5   : 99

```
#      LUT6                        : 56
#      MUXCY                       : 52
#      MUXF7                       : 54
#      MUXF8                       : 26
#      VCC                         : 1
#      XORCY                       : 39
# FlipFlops/Latches                : 112
#      FD                          : 76
#      FDE                         : 2
#      FDR                         : 24
#      FDRE                        : 10
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 20
#      IBUF                        : 5
#      OBUF                        : 15

Device utilization summary:
---------------------------

Selected Device : 7a100tfgg484-3


Slice Logic Utilization:
 Number of Slice Registers:             112  out of  126800     0%
 Number of Slice LUTs:                  295  out of  63400     0%
    Number used as Logic:               295  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    323
   Number with an unused Flip Flop:     211  out of    323    65%
   Number with an unused LUT:            28  out of    323     8%
   Number of fully used LUT-FF pairs:    84  out of    323    26%
   Number of unique control sets:         9

IO Utilization:
 Number of IOs:                         21
 Number of bonded IOBs:                 21  out of    285     7%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
```

```
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 112   |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.706ns (Maximum Frequency: 369.563MHz)
   Minimum input arrival time before clock: 2.160ns
   Maximum output required time after clock: 1.142ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.706ns (frequency: 369.563MHz)
  Total number of paths / destination ports: 4824 / 158
-------------------------------------------------------------------------
Delay:               2.706ns (Levels of Logic = 4)
  Source:            min_0 (FF)
  Destination:       min_3 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: min_0 to min_3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q            12   0.361   0.744  min_0 (min_0)
     LUT6:I0->O           19   0.097   0.379  _n0203<5>1 (_n0203)
     LUT6:I5->O            4   0.097   0.293  Mmux_current_mode_min[5]_mux_45_OUT211
(Mmux_current_mode_min[5]_mux_45_OUT21)
     MUXF7:S->O            1   0.335   0.295  current_mode_min[5]_mux_45_OUT<3>21_SW5 (N113)
     LUT6:I5->O            1   0.097   0.000  current_mode_min[5]_mux_45_OUT<3>1
(current_mode_min[5]_mux_45_OUT<3>1)
     FDRE:D                    0.008          min_3
    ----------------------------------------
    Total                      2.706ns (0.995ns logic, 1.711ns route)
                                       (36.8% logic, 63.2% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 70 / 27
-------------------------------------------------------------------------
Offset:              2.160ns (Levels of Logic = 5)
  Source:            down (PAD)
  Destination:       min_5 (FF)
  Destination Clock: clk rising

  Data Path: down to min_5
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

```
    ----------------------------------------  ------------
     IBUF:I->O            27   0.001   0.789  down_IBUF (down_IBUF)
     LUT5:I0->O            1   0.097   0.379  Mmux_current_mode_min[5]_mux_45_OUT211_SW0
(N163)
     LUT6:I4->O            2   0.097   0.299  current_mode_min[5]_mux_45_OUT<4>11
(current_mode_min[5]_mux_45_OUT<4>11)
     LUT6:I5->O            1   0.097   0.295  current_mode_min[5]_mux_45_OUT<3>21_SW3 (N110)
     LUT6:I5->O            1   0.097   0.000  current_mode_min[5]_mux_45_OUT<5>1
(current_mode_min[5]_mux_45_OUT<5>1)
     FDRE:D                    0.008          min_5
    ----------------------------------------
    Total                      2.160ns (0.397ns logic, 1.763ns route)
                                       (18.4% logic, 81.6% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 13 / 13
-------------------------------------------------------------------------
Offset:              1.142ns (Levels of Logic = 2)
  Source:            current_mode (FF)
  Destination:       clock_mode_indicator_led (PAD)
  Source Clock:      clk rising

  Data Path: current_mode to clock_mode_indicator_led
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             46   0.361   0.388  current_mode (current_mode)
     INV:I->O              1   0.113   0.279  current_mode_inv1_INV_0
(clock_mode_indicator_led_OBUF)
     OBUF:I->O                 0.000          clock_mode_indicator_led_OBUF
(clock_mode_indicator_led)
    ----------------------------------------
    Total                      1.142ns (0.474ns logic, 0.668ns route)
                                       (41.5% logic, 58.5% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.705|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 16.00 secs
Total CPU time to Xst completion: 15.94 secs

-->

Total memory usage is 4617976 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   53 (   0 filtered)
```

Number of infos   :   4 (0 filtered)