Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'Digital_Clock_12_hrFomrat'

Design Information

Command Line : map -intstyle ise -p xc7a100t-fgg484-3 -w -logic_opt off -ol high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off -power off -o Digital_Clock_12_hrFomrat_map.ncd Digital_Clock_12_hrFomrat.ngd Digital_Clock_12_hrFomrat.pcf
Target Device : xc7a100t
Target Package : fgg484
Target Speed : -3
Mapper Version : artix7 -- $Revision: 1.55 $
Mapped Date : Sun Mar 21 18:05:48 2021

Design Summary

Number of errors: 0
Number of warnings: 23
Slice Logic Utilization:

Number of Slice Registers:	112	out of	126,800	1%
Number used as Flip Flops:	112			
Number used as Latches:	0			
Number used as Latch-thrus:	0			
Number used as AND/OR logics:	0			
Number of Slice LUTs:	248	out of	63,400	1%
Number used as logic:	225	out of	63,400	1%
Number using O6 output only:	162			
Number using O5 output only:	35			
Number using O5 and O6:	28			
Number used as ROM:	0			
Number used as Memory:	0	out of	19,000	0%
Number used exclusively as route-thrus:	23			
Number with same-slice register load:	0			
Number with same-slice carry load:	2			
Number with other load:	21			

Slice Logic Distribution:

Number of occupied Slices:	90	out of	15,850	1%
Number of LUT Flip Flop pairs used:	270			
Number with an unused Flip Flop:	166	out of	270	61%
Number with an unused LUT:	22	out of	270	8%
Number of fully used LUT-FF pairs:	82	out of	270	30%
Number of unique control sets:	9			
Number of slice register sites lost to control set restrictions:	48	out of	126,800	1%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.
OVERMAPPING of BRAM resources should be ignored if the design is over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs:	21	out of	285	7%

Specific Feature Utilization:

Number of RAMB36E1/FIFO36E1s:	0	out of	135	0%
Number of RAMB18E1/FIFO18E1s:	0	out of	270	0%

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  Number of BUFG/BUFGCTRLs:                      1 out of      32    3%
    Number used as BUFGs:                        1
    Number used as BUFGCTRLs:                    0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:        0 out of     300    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:        0 out of     300    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:        0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:        1 out of     300    1%
    Number used as OLOGICE2s:                    1
    Number used as OLOGICE3s:                    0
    Number used as OSERDESE2s:                   0
  Number of PHASER_IN/PHASER_IN_PHYs:            0 out of      24    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:          0 out of      24    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      96    0%
  Number of BUFRs:                               0 out of      24    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DNA_PORTs:                           0 out of       1    0%
  Number of DSP48E1s:                            0 out of     240    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of GTPE2_CHANNELs:                      0 out of       4    0%
  Number of IBUFDS_GTE2s:                        0 out of       4    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       6    0%
  Number of IN_FIFOs:                            0 out of      24    0%
  Number of MMCME2_ADVs:                         0 out of       6    0%
  Number of OUT_FIFOs:                           0 out of      24    0%
  Number of PCIE_2_1s:                           0 out of       1    0%
  Number of PHASER_REFs:                         0 out of       6    0%
  Number of PHY_CONTROLs:                        0 out of       6    0%
  Number of PLLE2_ADVs:                          0 out of       6    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of XADCs:                               0 out of       1    0%

Average Fanout of Non-Clock Nets:                4.59

Peak Memory Usage:  5025 MB
Total REAL time to MAP completion:  48 secs
Total CPU time to MAP completion:   47 secs

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Section 1 - Errors
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Section 2 - Warnings
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WARNING:LIT:701 - PAD symbol "clk" has an undefined IOSTANDARD.
WARNING:LIT:702 - PAD symbol "clk" is not constrained (LOC) to a specific location.
WARNING:PhysDesignRules:2452 - The IOB an<0> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB an<1> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB an<2> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB an<3> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB an<4> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB an<5> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB clk is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB up is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<0> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<1> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB AMPM_indicator_led is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<2> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<3> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<4> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<5> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seg<6> is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB right is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB left is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB down is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB center is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB clock_mode_indicator_led is either not constrained (LOC) to a specific location and/or has an undefined I/O Standard (IOSTANDARD). This condition may seriously affect the device and will be an error in bitstream creation. It should be corrected by properly specifying the pin location and I/O Standard.

Section 3 - Informational

INFO:LIT:244 - All of the single ended outputs in this design are using slew rate limited output drivers. The delay on speed critical single ended outputs can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
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   2 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):
TYPE   BLOCK
GND   XST_GND
VCC   XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
AMPM_indicator_led	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<0>	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<1>	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<2>	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<3>	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<4>	IOB	OUTPUT	LVCMOS18		12	SLOW			
an<5>	IOB	OUTPUT	LVCMOS18		12	SLOW			
center	IOB	INPUT	LVCMOS18						
clk	IOB	INPUT	LVCMOS18						
clock_mode_indicator_led	IOB	OUTPUT	LVCMOS18		12	SLOW			
down	IOB	INPUT	LVCMOS18						
left	IOB	INPUT	LVCMOS18						
right	IOB	INPUT	LVCMOS18						
seg<0>	IOB	OUTPUT	LVCMOS18		12	SLOW			
seg<1>	IOB	OUTPUT	LVCMOS18		12	SLOW			
seg<2>	IOB	OUTPUT	LVCMOS18		12	SLOW			
seg<3>	IOB	OUTPUT	LVCMOS18		12	SLOW			
seg<4>	IOB	OUTPUT	LVCMOS18						

	12	SLOW			
seg<5>			IOB	OUTPUT	LVCMOS18
	12	SLOW			
seg<6>			IOB	OUTPUT	LVCMOS18
	12	SLOW			
up			IOB	INPUT	LVCMOS18

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.