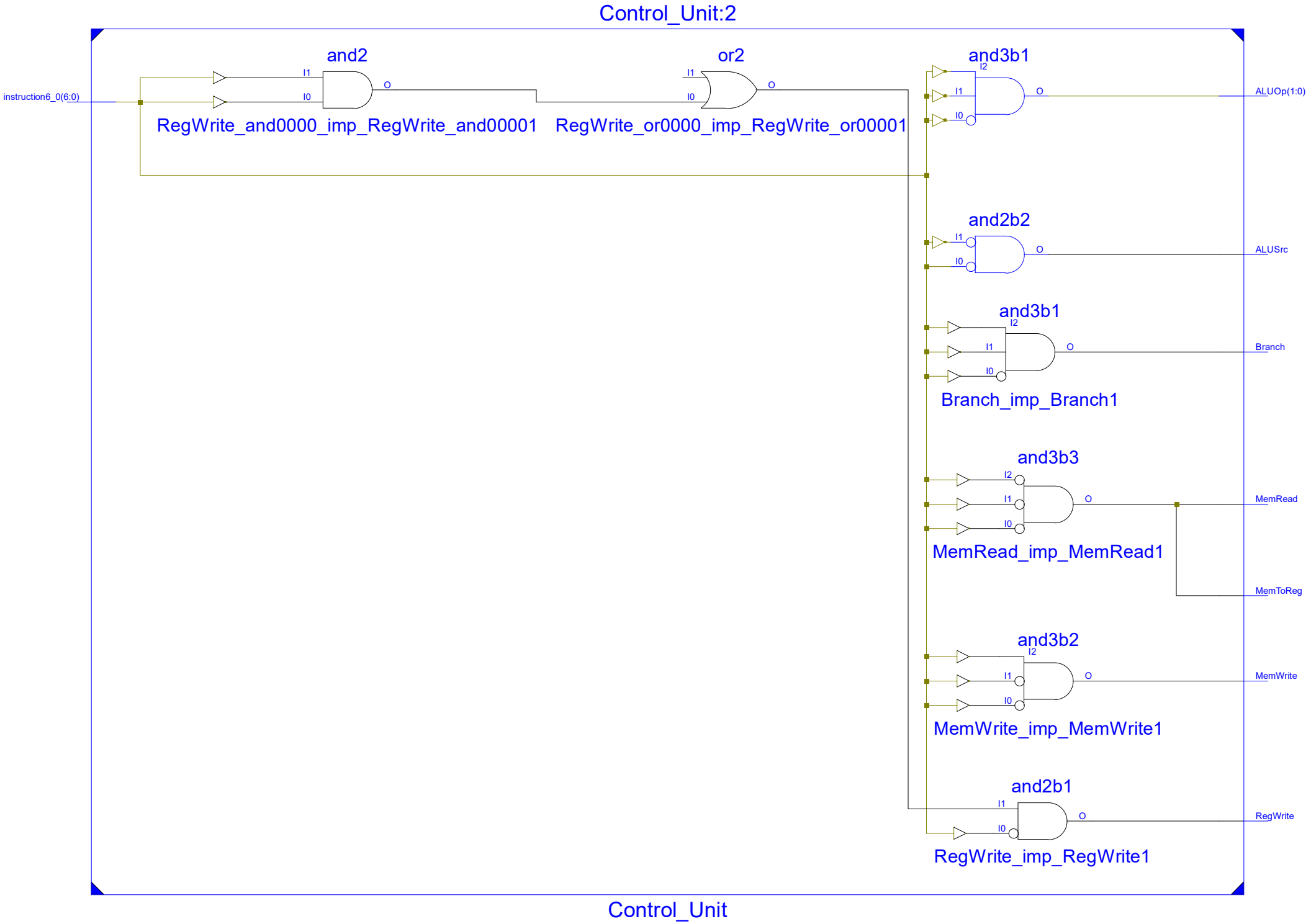
Control_Unit:2
and2
or2
and3b1
instruction6_0(6:0)
I1
I0
O
RegWrite_and0000_imp_RegWrite_and00001
RegWrite_or0000_imp_RegWrite_or00001
I2
ALUOp(1:0)
and2b2
ALUSrc
Branch
Branch_imp_Branch1
and3b3
MemRead
MemRead_imp_MemRead1
MemToReg
and3b2
MemWrite
MemWrite_imp_MemWrite1
and2b1
RegWrite
RegWrite_imp_RegWrite1
Control_Unit