Venkata Narendra Reddy Yaramala

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Objective

I am looking for physical design roles where I can contribute to projects and grow in my career. I trained in physical design at RV Skills, Bengaluru, and graduated from Gitam University, Visakhapatnam, in 2024 with a degree in ECE specializing in AIML.

Core Skills

- Experienced in ASIC flow, APR, including floor planning, power planning, clock tree synthesis, and routing. And Basic knowledge on Python, TCL scripting and Linux.
- STA concepts like slew, setup and hold, timing arcs, timing paths, input/output delays, timing models, and clock skew. Generated and analyzed timing reports.
- Worked on floorplan, handling macro placement, pin alignment, and power planning to minimize IR drop and build a proper power mesh to connect macros and standard cells without DRC errors.
- Implemented placement by arranging standard cells to fix timing and reduce congestion (GRC), and performed max transition and max delay timing analysis.
- Performed CTS using both classic and CCD techniques, optimized timing for the design, generated timing reports, and analyzed timing for max and min paths.
- Implemented routing while following DRC rules and resolved Antenna and shorts violations.

Experience

Physical Design Engineer Trainee (RV SKILLS, July 2024 – January 2025)

- Tool Used: ICC2 by Synopsys and PrimeTime.
- Designed: 40nm Physical Design Block.
- Insights: Worked on floorplan, power planning, placement, clock tree synthesis & Routing

Custom Layout Intern (CHIPEXTech, May 2023 - June 2023)

- Tool Used: Cadance Virtuoso XL, Caliber
- Designed: Various logic gates
- Insights: VLSI design principles and layout design

Domain Specific Project

Block level 40nm Technology low-power Physical Design

- Implemented block-level physical design for the Agni Subsystem using 40nm technology with Low Power Design.
- Key features include: Clock Frequency - 1 GHz, Macros - 34, Standard Cells - 41k, Area - 4.2 sq.mm, Supply Voltage – (1.1V, 1.8V), IR-Drop - 59mV, Metal Layers - 7, Clocks – 5.

Challenges

- Designed a floorplan by placing macros and created a power plan with the right spacing, pitch, and width values for metal layers to control IR drop, checked the power plan to fix DRC errors, ensuring no floating pins or short vias, and corrected PG DRC errors in the power network.
- Created the placement by positioning pre-placement cells, managing congestion, trying different floorplan options to improve the design, and fixing legality errors like overlapping cells, tap cells, boundary cells, and power switches.
- Understood CTS to meet target skew and latency requirements, resolved timing issues, and performed Static Timing Analysis (STA) after CTS to check timing reports for max transition, max delay, and min delay.
- Done routing while following DRC rules and resolved antenna, short and LVS violations.

Static Timing Analysis (STA)

- Analyzed timing of flip-flops and latches in different operating scenarios, considering OCV, AOCV, CRPR, and uncertainty factors.
- Tool use: Prime Time, ICC II

Challenges

- Analyzed timing exception violations, such as incorrect timing paths, disabled paths, and multi-cycle paths, and reported them for changes in the constraint file.
- Studied how clock latency, skew, OCV, AOCV, and CRPR affect timing.
- Reviewed timing reports for different path groups with latches and flip-flops to check for timing violations, compared PBA and GBA, and analyzed the effects of X-talk.
- Understood clock abnormalities like skew, jitter, and uncertainty.

Designing of Various Logic Gates using Cadence Virtuoso

- Implemented layouts and ran verifications including DRC, and LVS.
- Logic gates such as INV, NAND, XOR, XNOR, MUXS, DFFS, etc.
- Technology used: 28nm

Education

B.Tech-ECE AIML (2020-2024)

GITAM University, Visakhapatnam — CGPA - 8.22

Intermediate Education (2020)

Narayana Junior College, Hyderabad — Percentage - 94.7%

Secondary School of Education (2018)

New Era School, Khammam — GPA - 8.8

Extracurricular Activities

Graphical design lead - IETE Student Chapter

- Lead a team of 5 people and assisted in creating posters for various national and regional events. Experienced in using Adobe Photoshop.

Volunteer - National Service Scheme

- Tutored students, organized clean-up drives and fundraising events

Personal Profile

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