Digital VLSI SoC design and planning @ 21 Nov 2025 – 30 Nov 2025

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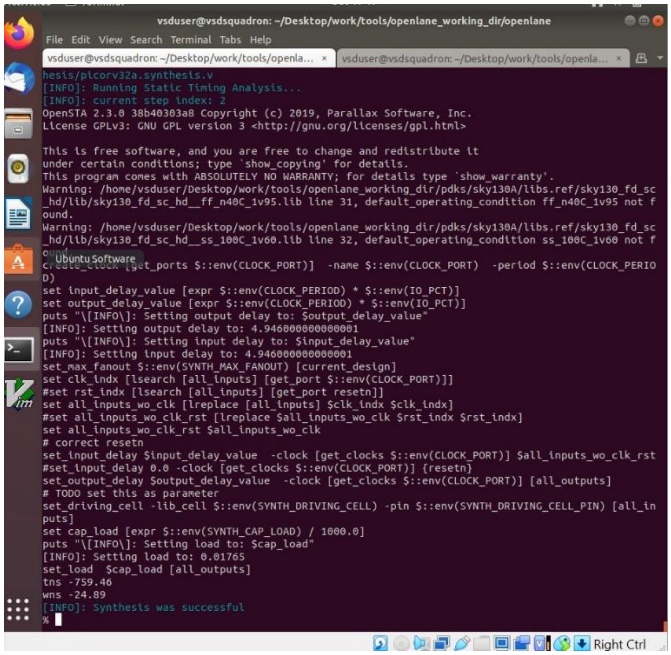
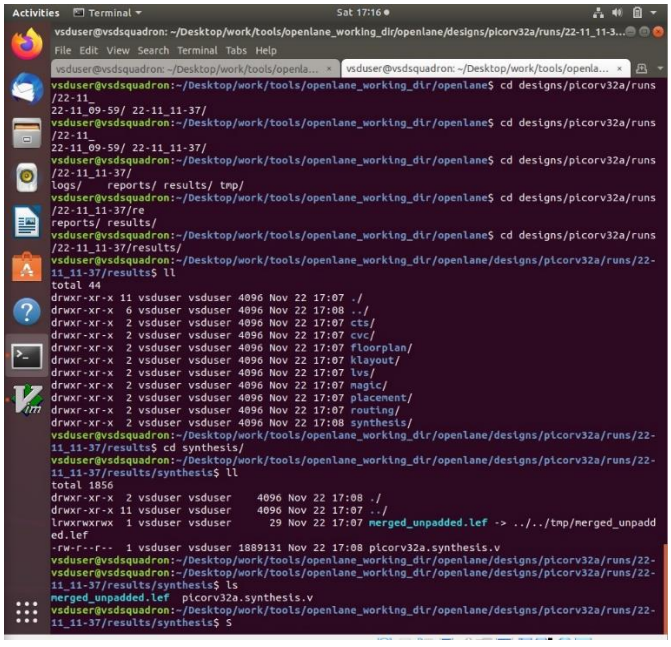
OpenLANE environment is set up and synthesis tool initialized for SKY130 PDK.



Synthesis completed showing total cell count and DFF statistics.



Synthesis completed.

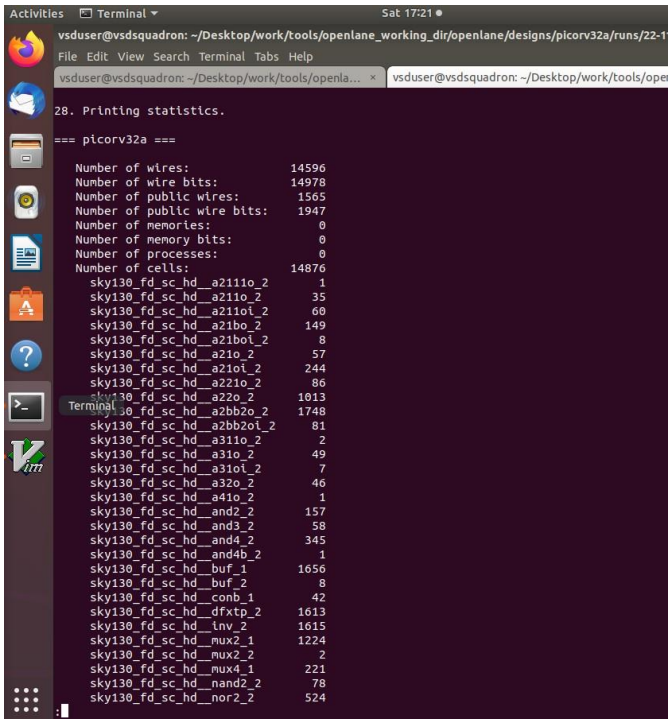
No of cells = 14876

DFF=1613 (D-flipflops)

DFF Ratio = (no of FF/ Total no of Cells) *100

Ratio=10.8%

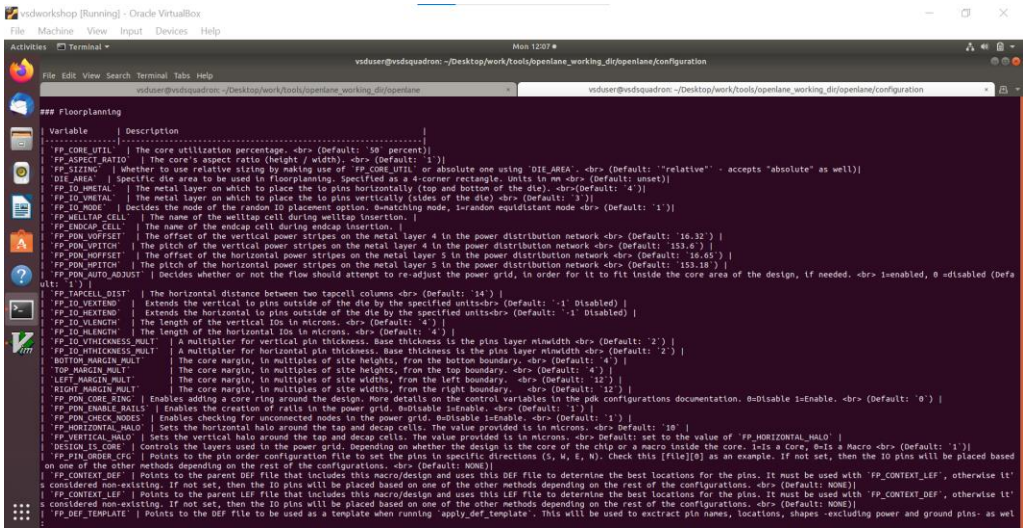
Floorplan stage begins showing switches used for configuring layout.



Floorplan

This are the switches used in the floorplan.

Default floorplan settings such as aspect ratio and utilization displayed.



Execution of run_floorplan command generating required floorplan files.

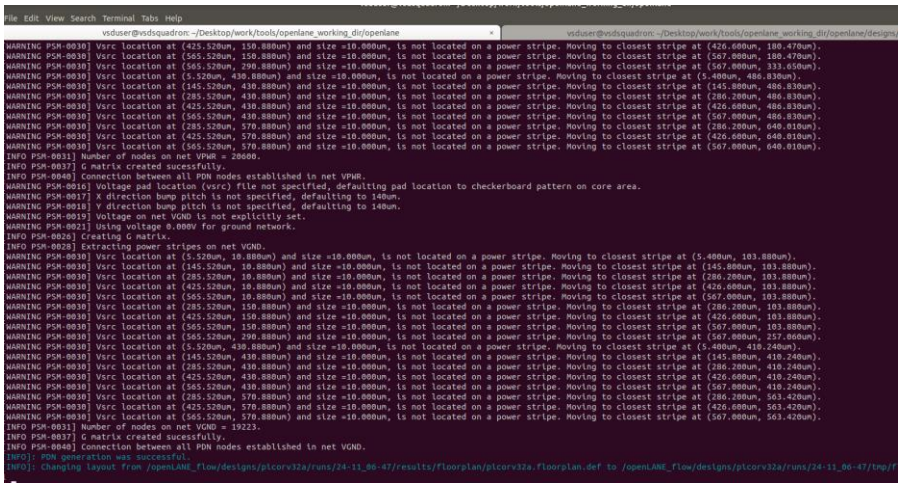
System default settings.

```
# Floorplan defaults
set ::env(FP_IO_VMETAL) 3
set ::env(FP_IO_HMETAL) 4

set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
set ::env(FP_IO_HTHICKNESS_MULT) 2

set ::env(BOTTOM_MARGIN_MULT) 4
set ::env(TOP_MARGIN_MULT) 4
set ::env(LEFT_MARGIN_MULT) 12
set ::env(RIGHT_MARGIN_MULT) 12

set ::env(FP_HORIZONTAL_HALO) 10
set ::env(FP_VERTICAL_HALO) $::env(FP_HORIZONTAL_HALO)

set ::env(DESIGN_IS_CORE) 1
(END)
```

floorplan.

Run_floorplan (is the command used for the running the floorplan)

All floorplan run files created including DEF and config outputs.



All the run files got created for the floorplan.

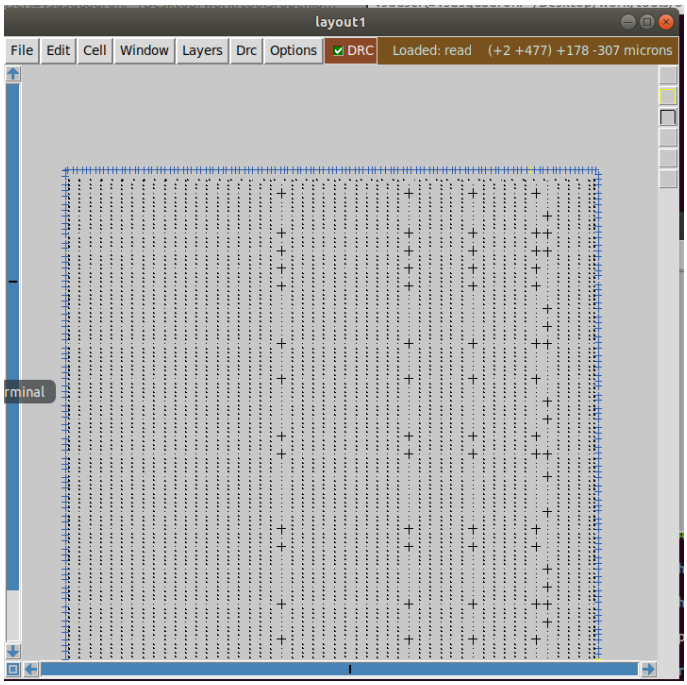
Generated floorplan DEF visualizing core boundaries and IO pin positions.

```
y130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd runs
/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ll
total 24
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:17 ./
drwxr-xr-x 4 vsduser docker  4096 Nov 22 15:29 ../
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 15:36 22-11_09-59/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 17:08 22-11_11-37/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 22:30 22-11_17-00/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:20 24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
 24-11_06-47/
logs/    reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
 24-11_06-47/
logs/    reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
 24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-
11_06-47$ ll
total 68
drwxr-xr-x  6 vsduser vsduser  4096 Nov 24 12:20 ./
drwxr-xr-x  6 vsduser vsduser  4096 Nov 24 12:17 ../
-rw-r--r--  1 vsduser vsduser  4743 Nov 24 12:20 cmds.log
-rw-r--r--  1 vsduser vsduser 21023 Nov 24 12:20 config.tcl
-rw-r--r--  1 vsduser vsduser   241 Nov 24 12:18 error.log
drwxr-xr-x 11 vsduser vsduser  4096 Nov 24 12:17 logs/
-rw-r--r--  1 vsduser vsduser    15 Nov 24 12:17 OPENLANE_VERSION
-rwxr-xr-x  1 vsduser vsduser   170 Jun 28  2021 PDK_SOURCES*
drwxr-xr-x 11 vsduser vsduser  4096 Nov 24 12:18 reports/
drwxr-xr-x 11 vsduser vsduser  4096 Nov 24 12:17 results/
drwxr-xr-x 11 vsduser vsduser  4096 Nov 24 12:19 tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-
11_06-47$ ls
cmds.log  config.tcl  error.log  logs  OPENLANE_VERSION  PDK_SOURCES  reports  results  tmp
```

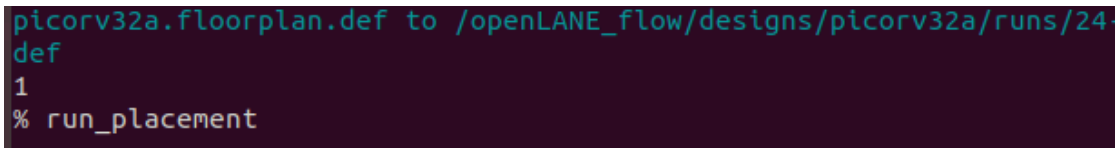
Cell rows and placement boundaries from floorplanning are shown.

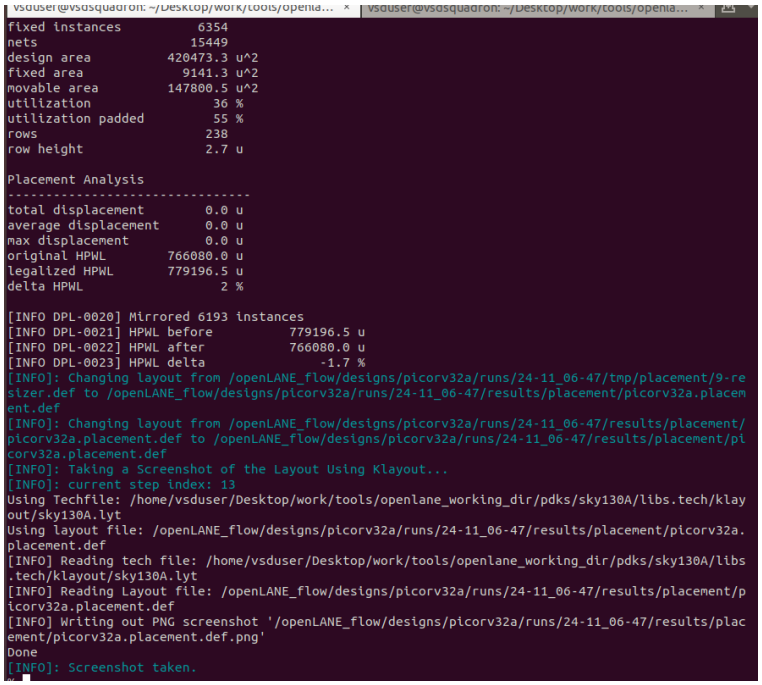
```
VERSION 5.8 ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;
DESIGN picorv32a ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 660685 671405 ) ;
ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_19 unithd 5520 62560 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_20 unithd 5520 65280 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_21 unithd 5520 68000 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_22 unithd 5520 70720 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_23 unithd 5520 73440 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_24 unithd 5520 76160 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_25 unithd 5520 78880 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_26 unithd 5520 81600 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_27 unithd 5520 84320 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_28 unithd 5520 87040 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_29 unithd 5520 89760 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_30 unithd 5520 92480 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_31 unithd 5520 95200 N DO 1412 BY 1 STEP 460 0 ;
```

created the floorplan.



Global placement running to arrange standard cells optimally.

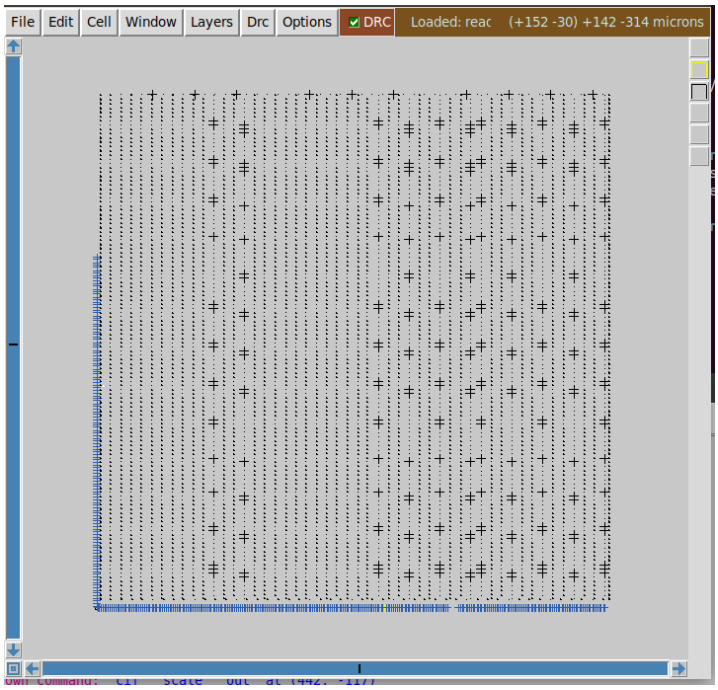




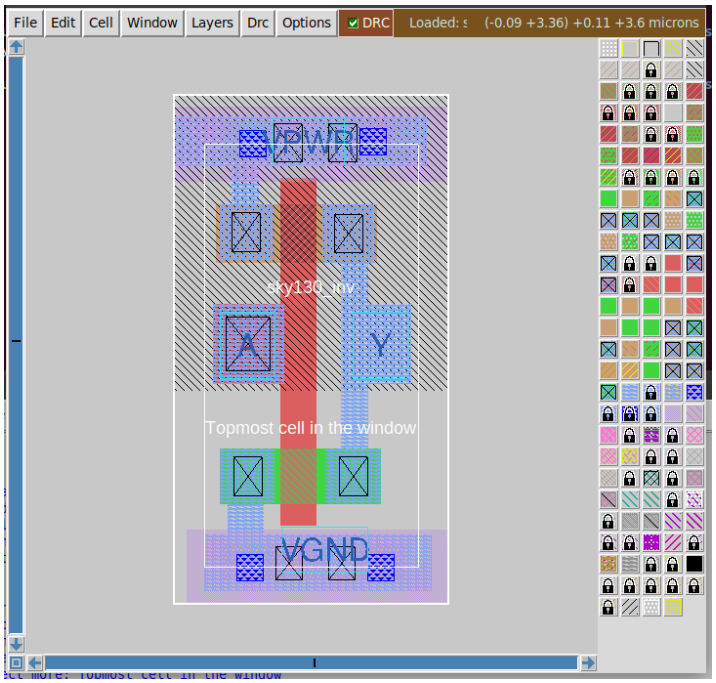
IO configuration set to 2 for improved pin distribution.

```
% set ::env(FP_IO_MODE) 2
2
% run_floorplan
```

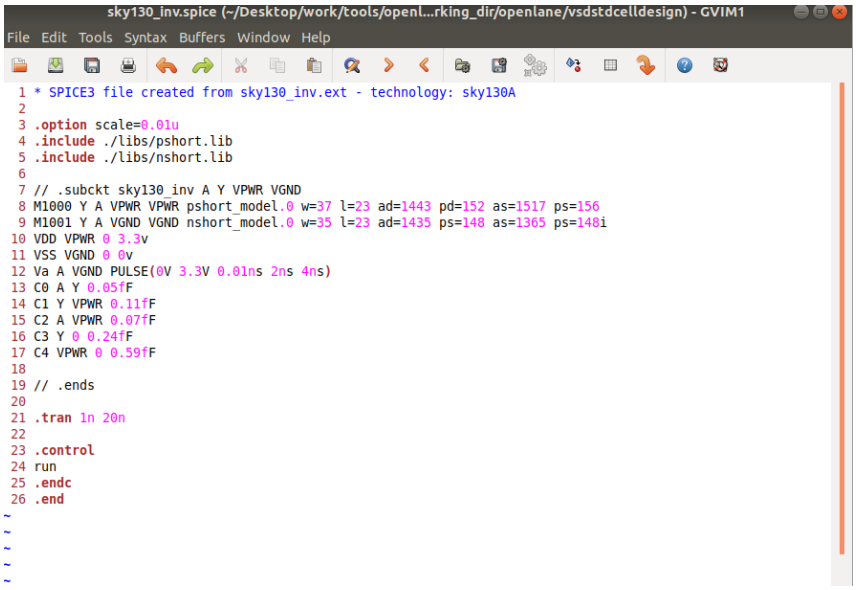
Standard cells arrangement visible for placement and routing.



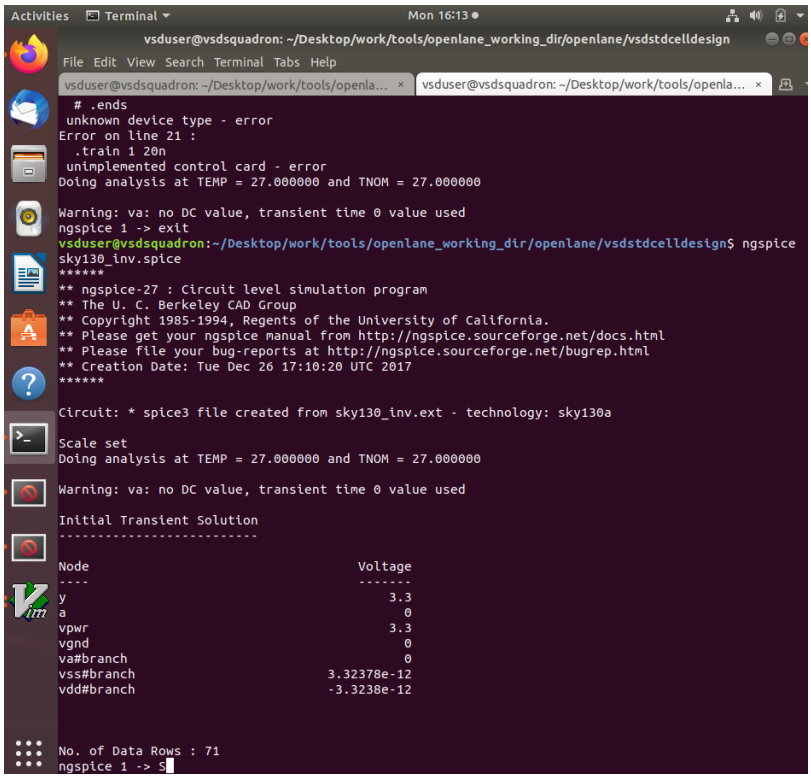
Flow for generating SPICE netlist of inverter shown.



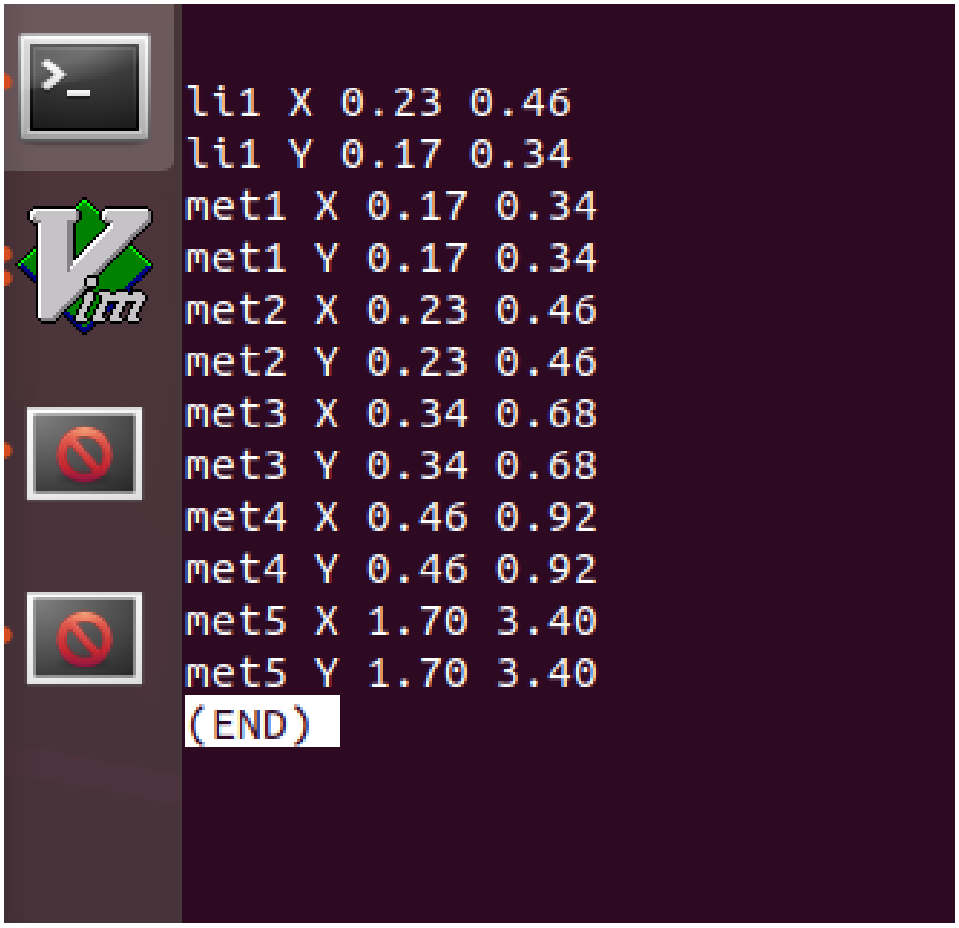
Flow for spice of an inverter.



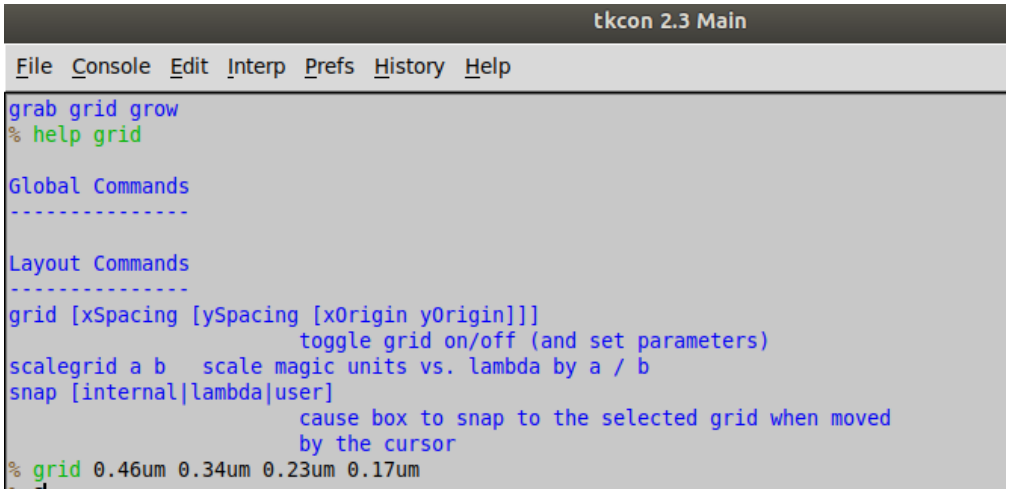
Inverter schematic with PMOS/NMOS connections displayed.



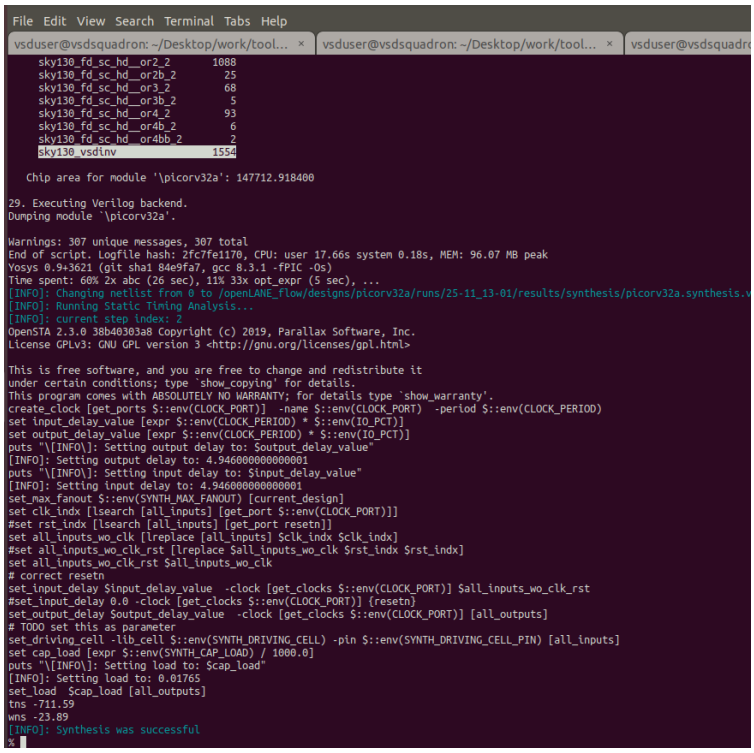
Track information generated for metal routing alignment.



Track mapping showing metal layer pitches and routing lanes.



We will extracted the lef of this standard cell. And will include that lef in the synthesis. This the image of no of inv add in the design

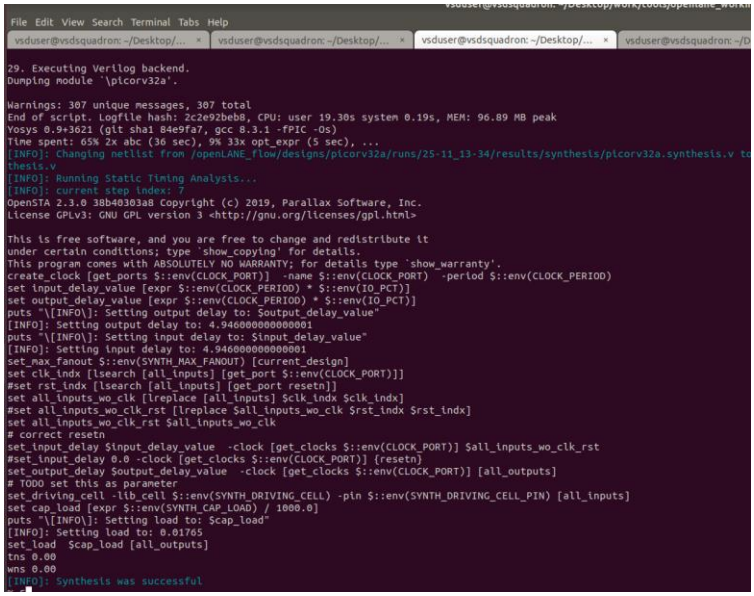


After we set some strategies

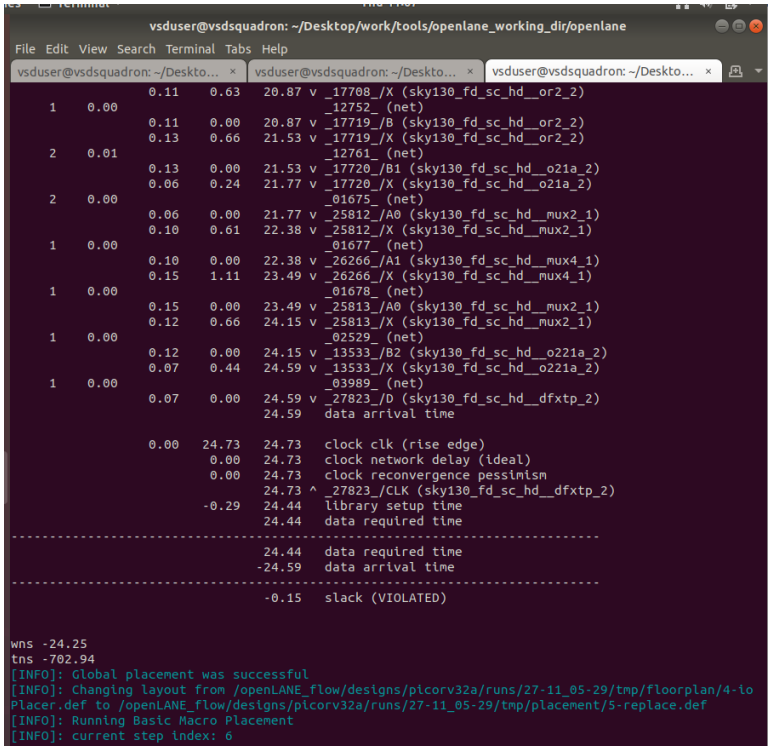
Set ::env(SYNTH_STRATEGY) “DELAY 1”

Set ::env(SYNTH_SIZING) 1

Floorplan run completed successfully.

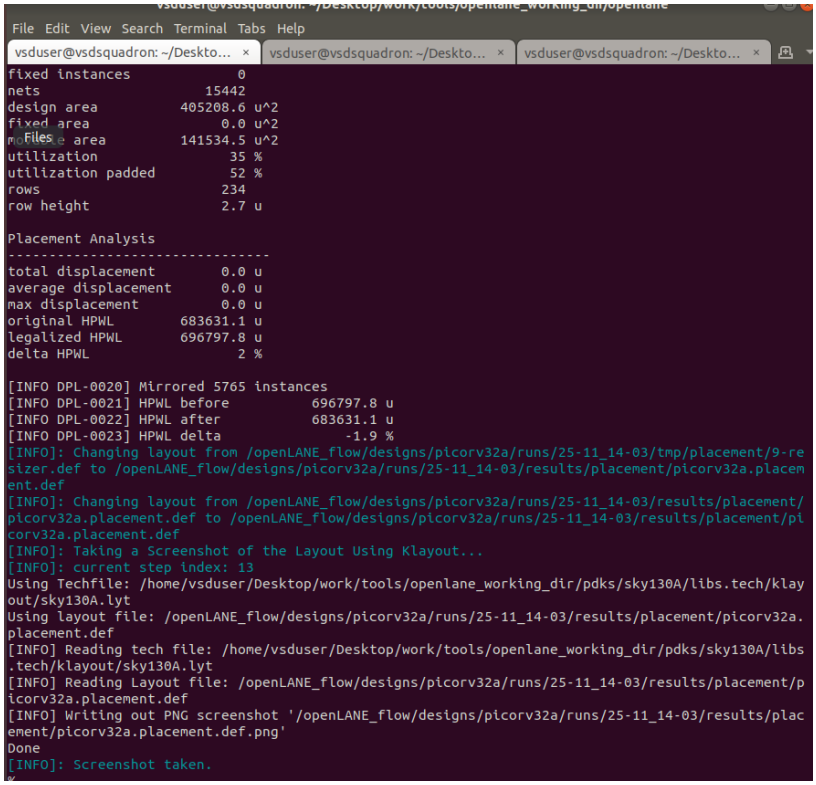


Placement stage completed with legal cell positions.

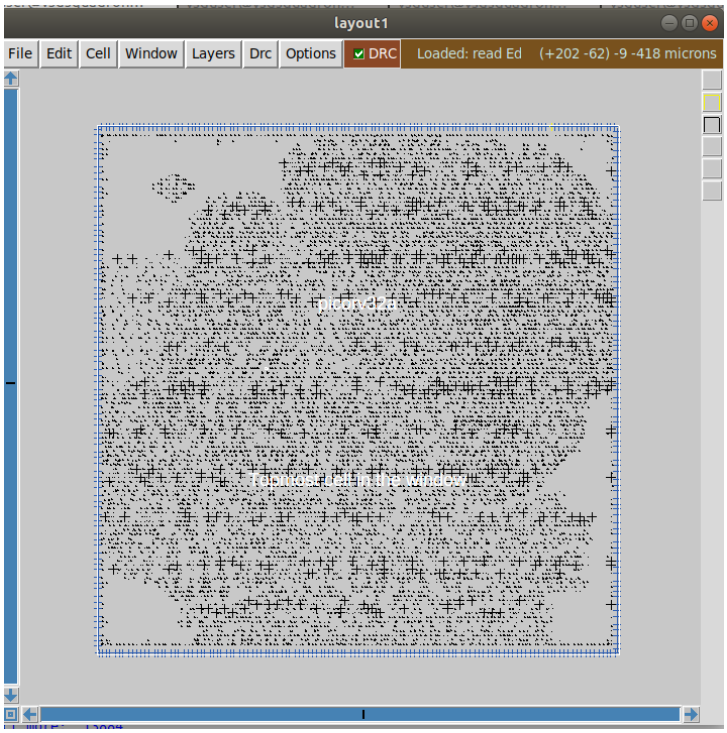


Placement running got completed

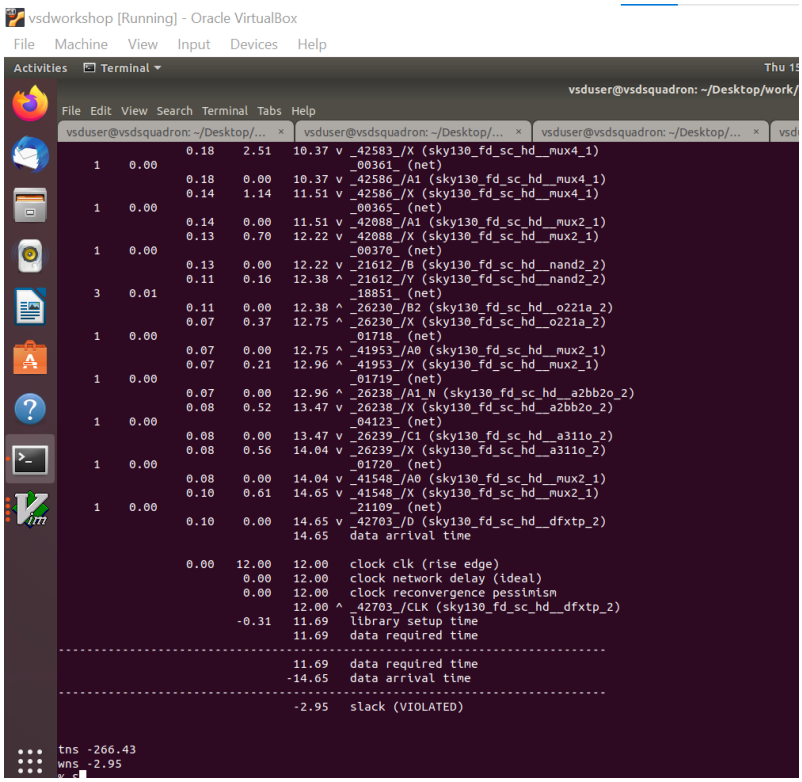
Placement visualization ensuring no overlaps.



Optimized placement



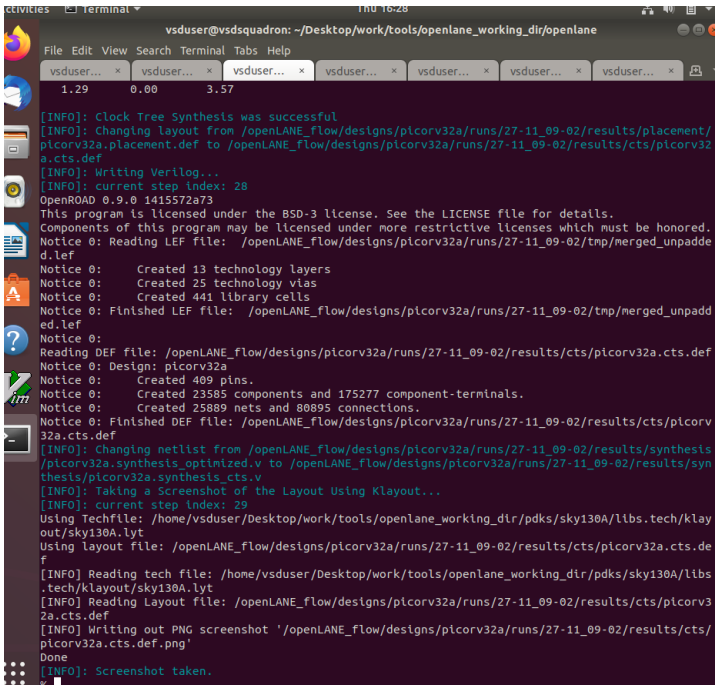
STA report generated.



Set ::env(SYNTH_MAX_FANOUT) 4

Increased the bufferibility of the cells by replacing the cells with higher drive strength

Clock Tree Synthesis (CTS) results displayed.



Specifications and timing constraints loaded.

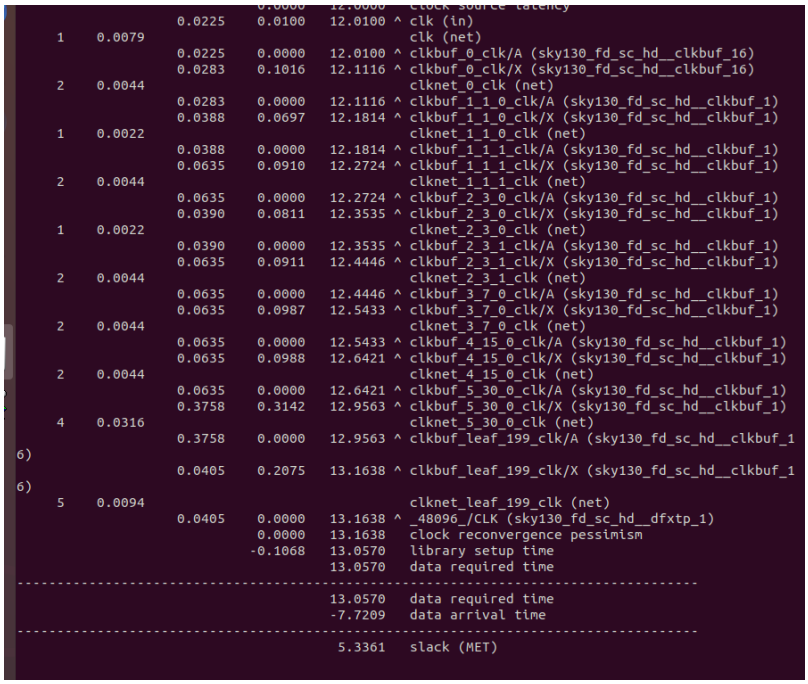
```
% echo $::env(LIB_SYNTH_COMPLETE)
/openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd__typical.lib
% echo $::env(CURRENT_TYPICAL)
can't read "::env(CURRENT_TYPICAL)": no such variable
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
% echo $::env(SYNTH_MAX_TRAN)
2.4730000000000003
% echo $::env(CTS_MAX_CAP)
1.53169
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd__clkbuf_1 sky130_fd_sc_hd__clkbuf_2 sky130_fd_sc_hd__clkbuf_4 sky130_fd_sc_hd__clkbuf_8
% echo $::env(CTS_ROOT_BUFFER)
sky130_fd_sc_hd__clkbuf_16
%
```

OpenROAD commands loaded for STA analysis.

```
read_lef read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged.lef
read_def read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
write_db pico_cts.db
read_db pico_cts.db
read_verilog /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_cts.v
read_liberty -max $::env(LIB_SLOWEST)
read_liberty -min $::env(LIB_FASTEST)
read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
set_propagated_clock [all_clocks]
report_checks -path_delay min_max -format full_clock_expanded digits 4
```

Slack violation detected post-CTS.

Timing fixed and slack met successfully.



```
                                                  clock source latency
                  0.0225    0.0100   12.0100 ^ clk (in)
     1    0.0079                              clk (net)
                  0.0225    0.0000   12.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd__clkbuf_16)
                  0.0283    0.1016   12.1116 ^ clkbuf_0_clk/X (sky130_fd_sc_hd__clkbuf_16)
     2    0.0044                              clknet_0_clk (net)
                  0.0283    0.0000   12.1116 ^ clkbuf_1_1_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0388    0.0697   12.1814 ^ clkbuf_1_1_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
     1    0.0022                              clknet_1_1_0_clk (net)
                  0.0388    0.0000   12.1814 ^ clkbuf_1_1_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0635    0.0910   12.2724 ^ clkbuf_1_1_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
     2    0.0044                              clknet_1_1_1_clk (net)
                  0.0635    0.0000   12.2724 ^ clkbuf_2_3_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0390    0.0811   12.3535 ^ clkbuf_2_3_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
     1    0.0022                              clknet_2_3_0_clk (net)
                  0.0390    0.0000   12.3535 ^ clkbuf_2_3_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0635    0.0911   12.4446 ^ clkbuf_2_3_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
     2    0.0044                              clknet_2_3_1_clk (net)
                  0.0635    0.0000   12.4446 ^ clkbuf_3_7_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0635    0.0987   12.5433 ^ clkbuf_3_7_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
     2    0.0044                              clknet_3_7_0_clk (net)
                  0.0635    0.0000   12.5433 ^ clkbuf_4_15_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.0635    0.0988   12.6421 ^ clkbuf_4_15_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
     2    0.0044                              clknet_4_15_0_clk (net)
                  0.0635    0.0000   12.6421 ^ clkbuf_5_30_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                  0.3758    0.3142   12.9563 ^ clkbuf_5_30_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
     4    0.0316                              clknet_5_30_0_clk (net)
                  0.3758    0.0000   12.9563 ^ clkbuf_leaf_199_clk/A (sky130_fd_sc_hd__clkbuf_1
6)
                  0.0405    0.2075   13.1638 ^ clkbuf_leaf_199_clk/X (sky130_fd_sc_hd__clkbuf_1
6)
     5    0.0094                              clknet_leaf_199_clk (net)
                  0.0405    0.0000   13.1638 ^ _48096_/CLK (sky130_fd_sc_hd__dfxtp_1)
                            0.0000   13.1638   clock reconvergence pessimism
                           -0.1068   13.0570   library setup time
                                     13.0570   data required time
-----------------------------------------------------------------------------
                                     13.0570   data required time
                                     -7.7209   data arrival time
-----------------------------------------------------------------------------
                                      5.3361   slack (MET)
```

PDN generation process started.

```
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
%
%
%
% gen_pdn
```

```
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on
a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 27491.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/floorplan/30-pdn.def
%
```

```
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 441 library cells
Notice 0: Finished LEF file:  /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadd
ed.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 23585 components and 175277 component-terminals.
Notice 0:     Created 25889 nets and 80895 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016]   config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/l
ibs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ****** INFO ******
Type: stdcell, grid
    Stdcell Rails
      Layer: met1 -  width: 0.480  pitch: 2.720  offset: 0.000
    Straps
      Layer: met4 -  width: 1.600  pitch: 153.600  offset: 16.320
      Layer: met5 -  width: 1.600  pitch: 153.180  offset: 16.650
    Connect: {met4 met5} {met1 met4}
Type: macro, macro_1
    Macro orientation: R0 R180 MX MY R90 R270 MXR90 MYR90
    Straps
    Connect: {met4_PIN_ver met5}
[INFO] [PDNG-0012] **** END INFO ****
```

PDN information showing power rails and pitch.

Routing stage initiated connecting all components.

```
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/28-11_11-41 in 0h18m22s
%
```