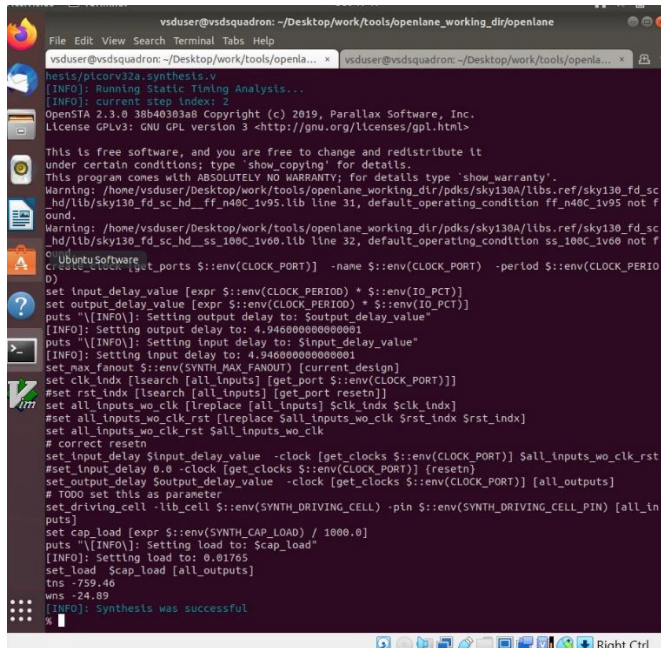


Digital VLSI SoC design and planning @ 21 Nov 2025 – 30 Nov 2025

Y Venkata Narendra Reddy

Venkatnarendra767@gmail.com

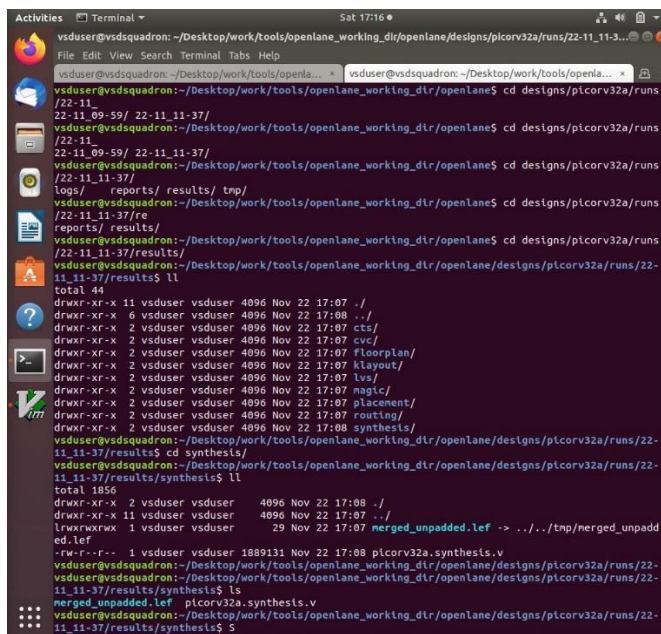
OpenLANE environment is set up and synthesis tool initialized for SKY130 PDK.



```
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane... vdsuser@vdsquadron: ~/Desktop/work/tools/openlane...
hests/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current_step_index: 2
OpenSTA 2.3.0 38b40303a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
Warning: /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc
_hd/lib/sky130_fd_sc_hd_ff_n40c_iv95.lib line 31, default_operating_condition ff_n40c_iv95 not f
ound.
Warning: /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc
_hd/lib/sky130_fd_sc_hd_ss_100c_iv60.lib line 32, default_operating_condition ss_100c_iv60 not f
ound.
c
UbuntuSoftware
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIO
D)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.940000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.940000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_idx [lsearch [all_inputs] [get_port rstn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] (resetn)
set output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_in
puts]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set load $cap_load [all_outputs]
tms -759.46
wms -24.89
[INFO]: Synthesis was successful
%
```

Synthesis completed showing total cell count and DFF statistics.



```
Activities Terminal Sat 17:16
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-11-11-37
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane... vdsuser@vdsquadron: ~/Desktop/work/tools/openlane...
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs
/22-11-11-37/
22-11-09-59/ 22-11-11-37/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs
/22-11-11-37/
22-11-09-59/ 22-11-11-37/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs
/22-11-11-37/
logs/ reports/ results/ tmp/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs
/22-11-11-37/
reports/ results/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/runs
/22-11-11-37/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results$ ll
total 44
drwxr-xr-x 11 vdsuser vdsuser 4096 Nov 22 17:07 ./
drwxr-xr-x 6 vdsuser vdsuser 4096 Nov 22 17:08 ../
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 cts/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 cvc/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 floorplan/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 layout/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 lvs/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 magic/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 placement/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:07 routing/
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:08 synthesis/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results$ cd synthesis/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results/synthesis$ ll
total 1856
drwxr-xr-x 2 vdsuser vdsuser 4096 Nov 22 17:08 ./
drwxr-xr-x 11 vdsuser vdsuser 4096 Nov 22 17:07 ../
lrwxrwxrwx 1 vdsuser vdsuser 29 Nov 22 17:07 merged_unpadded.lef -> ../../tmp/merged_unpadd
ed.lef
-rw-r--r-- 1 vdsuser vdsuser 1889131 Nov 22 17:08 picorv32a.synthesis.v
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results/synthesis$ cd synthesis/
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-
11-11-37/results/synthesis$ cd synthesis/
```

Synthesis completed.

Execution of run floorplan command generating required floorplan files.

System default settings.

```
# Floorplan defaults
set ::env(FP_IO_VMETAL) 3
set ::env(FP_IO_HMETAL) 4

set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
set ::env(FP_IO_HTHICKNESS_MULT) 2

set ::env(BOTTOM_MARGIN_MULT) 4
set ::env(TOP_MARGIN_MULT) 4
set ::env(LEFT_MARGIN_MULT) 12
set ::env(RIGHT_MARGIN_MULT) 12

set ::env(FP_HORIZONTAL_HALO) 10
set ::env(FP_VERTICAL_HALO) $::env(FP_HORIZONTAL_HALO)

set ::env(DSIGN_IS_CORE) 1
(END)
```

floorplan.

Run_floorplan (is the command used for the running the floorplan)

All floorplan run files created including DEF and config outputs.

```
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs

WARNING PSM-0030] vsrc location at (425.520um, 150.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 180.470um).
WARNING PSM-0030] vsrc location at (565.520um, 290.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 180.470um).
WARNING PSM-0030] vsrc location at (5.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 486.830um).
WARNING PSM-0030] vsrc location at (425.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 486.830um).
WARNING PSM-0030] vsrc location at (285.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 486.830um).
WARNING PSM-0030] vsrc location at (425.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 486.830um).
WARNING PSM-0030] vsrc location at (565.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 486.830um).
WARNING PSM-0030] vsrc location at (285.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 640.810um).
WARNING PSM-0030] vsrc location at (425.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 640.810um).
WARNING PSM-0030] vsrc location at (565.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 640.810um).
INFO PSM-0031] Number of nodes on net VPWR = 20800.
INFO PSM-0032] G matrix created successfully.
INFO PSM-0040] Connection between all PDN nodes established in net VPWR.
WARNING PSM-0016] voltage pad location (vsrc) file not specified, defaulting pad location to checkerboard pattern on core area.
WARNING PSM-0017] x direction bump pitch is not specified, defaulting to 140um.
WARNING PSM-0018] y direction bump pitch is not specified, defaulting to 140um.
WARNING PSM-0019] voltage on net VGG0 is not explicitly set.
WARNING PSM-0021] using voltage 0.000V for ground network.
INFO PSM-0026] Creating G matrix.
INFO PSM-0028] Extracting power stripes on net VGG0.
WARNING PSM-0030] vsrc location at (5.520um, 10.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 103.880um).
WARNING PSM-0030] vsrc location at (145.520um, 10.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 103.880um).
WARNING PSM-0030] vsrc location at (285.520um, 10.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.20um, 103.880um).
WARNING PSM-0030] vsrc location at (425.520um, 10.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
WARNING PSM-0030] vsrc location at (565.520um, 10.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 103.880um).
WARNING PSM-0030] vsrc location at (285.520um, 150.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
WARNING PSM-0030] vsrc location at (425.520um, 150.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
WARNING PSM-0030] vsrc location at (565.520um, 150.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 103.880um).
WARNING PSM-0030] vsrc location at (5.520um, 290.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 257.060um).
WARNING PSM-0030] vsrc location at (5.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
WARNING PSM-0030] vsrc location at (145.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
WARNING PSM-0030] vsrc location at (285.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
WARNING PSM-0030] vsrc location at (425.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
WARNING PSM-0030] vsrc location at (565.520um, 430.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 410.240um).
WARNING PSM-0030] vsrc location at (285.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
WARNING PSM-0030] vsrc location at (425.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
WARNING PSM-0030] vsrc location at (565.520um, 570.880um) and size <10.000um, is not located on a power stripe. Moving to closest stripe at (567.600um, 563.420um).
INFO PSM-0031] Number of nodes on net VGG0 = 19223.
INFO PSM-0032] G matrix created successfully.
INFO PSM-0040] Connection between all PDN nodes established in net VGG0.
[INFO] PDN generation was successful.
[INFO] Creating layout from /openLANE_flow/designs/gtcorv32a/runs/24-11-06-47/results/floorplan/gtcorv32a/floorplan.def to /openLANE_flow/designs/gtcorv32a/runs/24-11-06-47/tmp/
```

All the run files got created for the floorplan.

Generated floorplan DEF visualizing core boundaries and IO pin positions.

```

y130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd runs
/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ll
total 24
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:17 ./
drwxr-xr-x 4 vsduser docker  4096 Nov 22 15:29 ../
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 15:36 22-11_09-59/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 17:08 22-11_11-37/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 22:30 22-11_17-00/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:20 24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
24-11_06-47/
logs/ reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
24-11_06-47/
logs/ reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd
24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-
11_06-47$ ll
total 68
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:20 ./
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:17 ../
-rw-r--r-- 1 vsduser vsduser 4743 Nov 24 12:20 cmds.log
-rw-r--r-- 1 vsduser vsduser 21023 Nov 24 12:20 config.tcl
-rw-r--r-- 1 vsduser vsduser 241 Nov 24 12:18 error.log
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:17 logs/
-rw-r--r-- 1 vsduser vsduser 15 Nov 24 12:17 OPENLANE_VERSION
-rwxr-xr-x 1 vsduser vsduser 170 Jun 28 2021 PDK_SOURCES*
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:18 reports/
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:17 results/
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:19 tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-
11_06-47$ ls
cmds.log config.tcl error.log logs OPENLANE_VERSION PDK_SOURCES reports results tmp
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-
11_06-47$

```

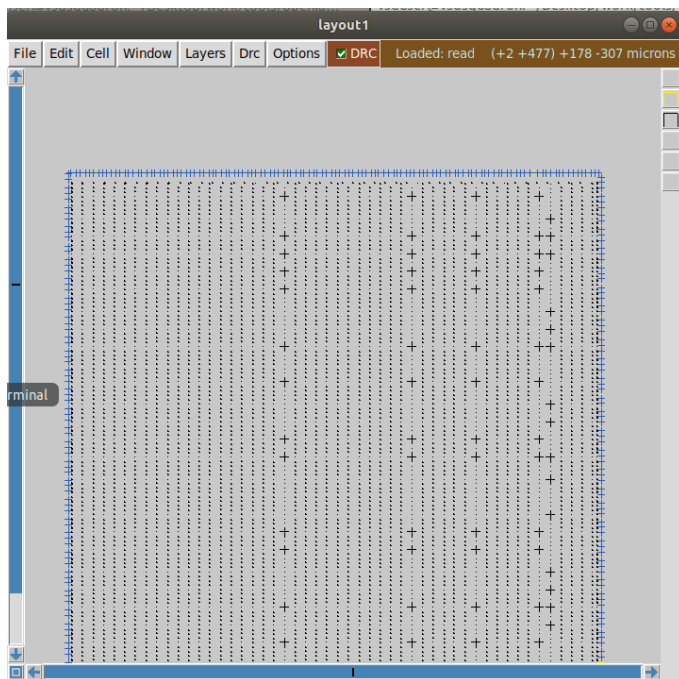
Cell rows and placement boundaries from floorplanning are shown.

```

VERSION 5.8 ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[" ;
DESIGN picorv32a ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 660685 671405 ) ;
ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_19 unithd 5520 62560 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_20 unithd 5520 65280 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_21 unithd 5520 68000 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_22 unithd 5520 70720 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_23 unithd 5520 73440 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_24 unithd 5520 76160 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_25 unithd 5520 78880 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_26 unithd 5520 81600 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_27 unithd 5520 84320 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_28 unithd 5520 87040 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_29 unithd 5520 89760 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_30 unithd 5520 92480 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_31 unithd 5520 95200 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_32 unithd 5520 97920 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_33 unithd 5520 100640 N DO 1412 BY 1 STEP 460 0 ;

```


created the floorplan.



Global placement running to arrange standard cells optimally.

```
picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def
1
% run_placement
```

```
vsduser@vsasquadron: ~/Desktop/work/tools/openlane... * vsduser@vsasquadron: ~/Desktop/work/tools/openlane... *
fixed instances 6354
nets 15449
design area 420473.3 u^2
fixed area 9141.3 u^2
movable area 147800.5 u^2
utilization 36 %
utilization padded 55 %
rows 238
row height 2.7 u

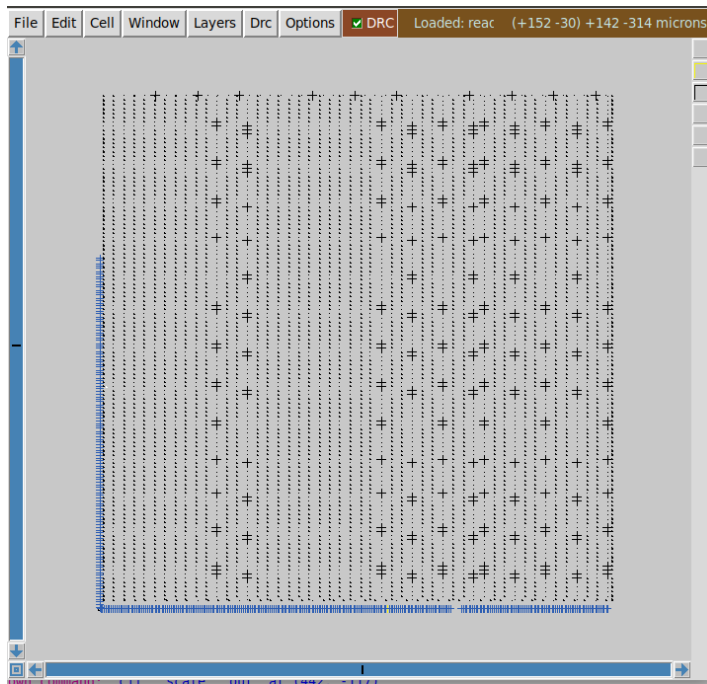
Placement Analysis
-----
total displacement 0.0 u
average displacement 0.0 u
max displacement 0.0 u
original HPWL 766080.0 u
legalized HPWL 779196.5 u
delta HPWL 2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before 779196.5 u
[INFO DPL-0022] HPWL after 766080.0 u
[INFO DPL-0023] HPWL delta -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-11_06-47/tmp/placement/9-re
sizer.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placem
ent.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/
picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/pl
icorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 13
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klay
out/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.
placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs
.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/p
icorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/plac
ement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
```

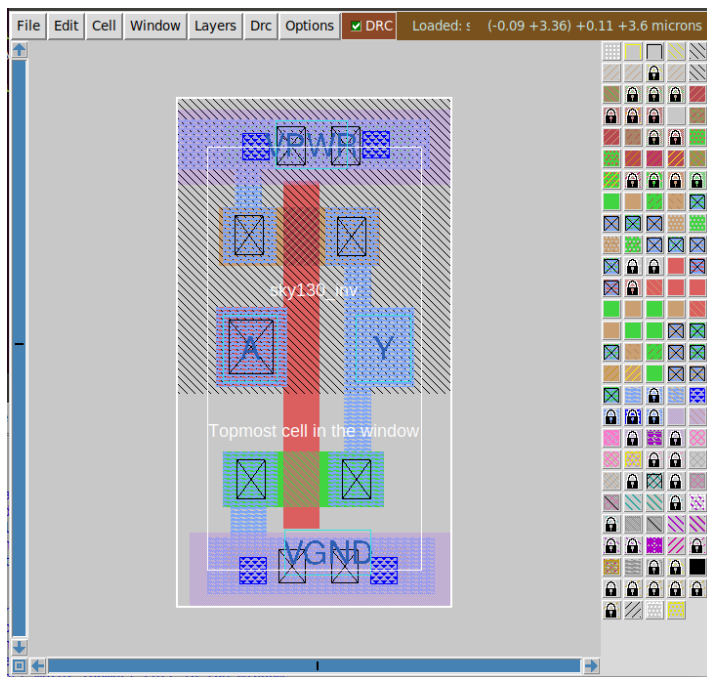
IO configuration set to 2 for improved pin distribution.

```
[INFO]: Screenshot taken.  
% set ::env(FP_IO_MODE) 2  
2  
% run_floorplan
```

Standard cells arrangement visible for placement and routing.



Flow for generating SPICE netlist of inverter shown.



Flow for spice of an inverter.

```
sky130_inv.spice (~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=0.01u
4 .include ./libs/pshort.lib
5 .include ./libs/nshort.lib
6
7 // .subckt sky130_inv A Y VPWR VGND
8 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23 ad=1443 pd=152 as=1517 ps=156
9 M1001 Y A VGND VGND nshort_model.0 w=35 l=23 ad=1435 ps=148 as=1365 ps=1461
10 VDD VPWR 0 3.3V
11 VSS VGND 0 0V
12 Va A VGND PULSE(0V 3.3V 0.01ns 2ns 4ns)
13 C0 A Y 0.85fF
14 C1 Y VPWR 0.11fF
15 C2 A VPWR 0.07fF
16 C3 Y 0 0.24fF
17 C4 VPWR 0 0.59fF
18
19 // .ends
20
21 .tran 1n 20n
22
23 .control
24 run
25 .endc
26 .end
```

Inverter schematic with PMOS/NMOS connections displayed.

```
Activities Terminal Mon 16:13
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Tabs Help
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane... vdsuser@vdsquadron: ~/Desktop/work/tools/openlane...
# .ends
unknown device type - error
Error on line 21 :
.tran 1 20n
unimplemented control card - error
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: va: no DC value, transient time 0 value used
ngspice 1 -> exit
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice
sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****

Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

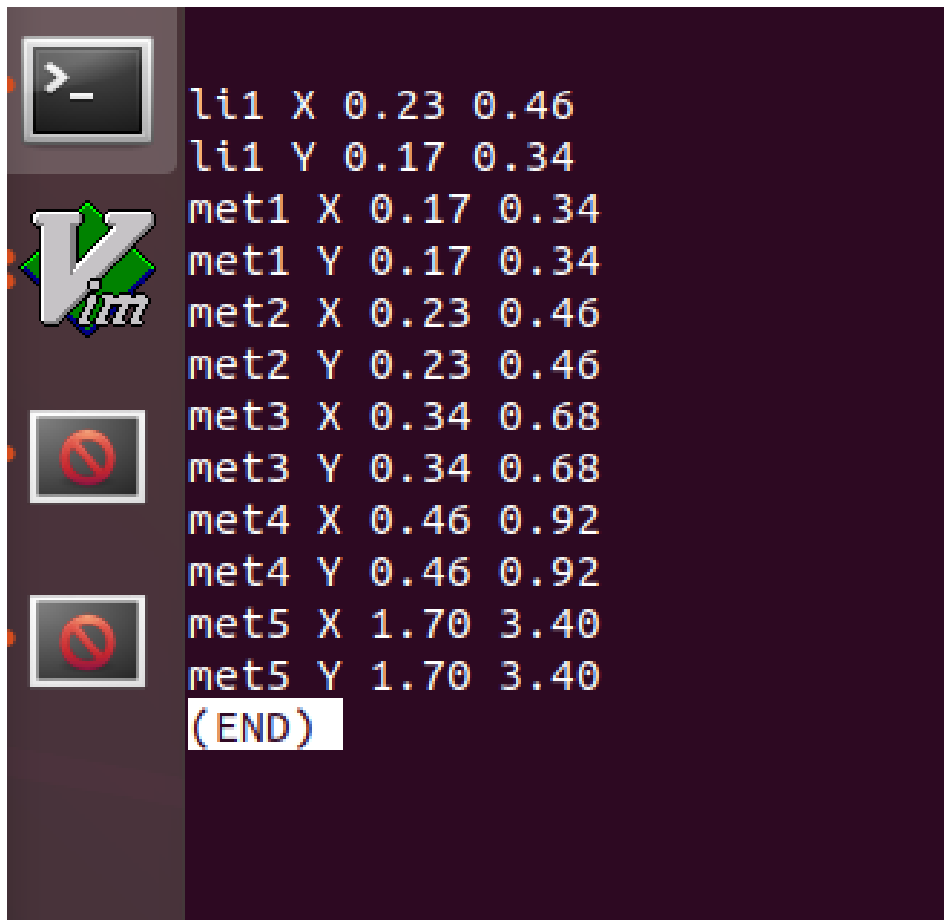
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: va: no DC value, transient time 0 value used

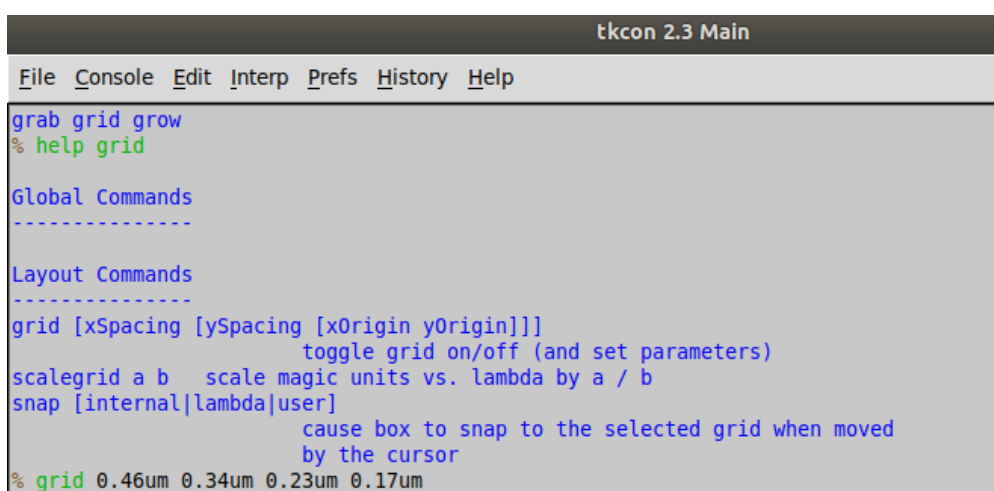
Initial Transient Solution
-----
Node          Voltage
----          -
y              3.3
a              0
vpwr           3.3
vgnd           0
va#branch      0
vss#branch     3.32378e-12
vdd#branch     -3.3238e-12

No. of Data Rows : 71
ngspice 1 -> S
```

Track information generated for metal routing alignment.



Track mapping showing metal layer pitches and routing lanes.



We will extract the left of this standard cell. And will include that left in the synthesis. This is the image of no of inv add in the design

```
File Edit View Search Terminal Tabs Help
vdsuser@vdsquadron: ~/Desktop/work/tool... x vdsuser@vdsquadron: ~/Desktop/work/tool... x vdsuser@vdsquadron: ~/Desktop/work/tool... x

sky130_fd_sc_hd__or2_2 1088
sky130_fd_sc_hd__or2b_2 25
sky130_fd_sc_hd__or3_2 68
sky130_fd_sc_hd__or3b_2 5
sky130_fd_sc_hd__or4_2 93
sky130_fd_sc_hd__or4b_2 6
sky130_fd_sc_hd__or4bb_2 2
sky130_vsdinv 1554

Chip area for module 'picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module 'picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: 2fc7fe1170, CPU: user 17.66s system 0.18s, MEM: 96.07 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 60% 2x abc (26 sec), 11% 33x opt_expr (5 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/25-11_13-01/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.3.0 38b40303a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_idx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] (resetn)
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tss 711.59
wns -23.89
[INFO]: Synthesis was successful
%
```

After we set some strategies

Set ::env(SYNTH_STRATEGY) "DELAY 1"

Set ::env(SYNTH_SIZING) 1

Floorplan run completed successfully.

```
File Edit View Search Terminal Tabs Help
vdsuser@vdsquadron: ~/Desktop/work/tool... x vdsuser@vdsquadron: ~/Desktop/work/tool... x vdsuser@vdsquadron: ~/Desktop/work/tool... x vdsuser@vdsquadron: ~/Desktop/work/tool... x

29. Executing Verilog backend.
Dumping module 'picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: 2c2e92beb8, CPU: user 19.30s system 0.19s, MEM: 96.89 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 65% 2x abc (36 sec), 9% 33x opt_expr (5 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/25-11_13-34/results/synthesis/picorv32a.synthesis.v to
thesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.3.0 38b40303a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_idx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] (resetn)
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tss 0.00
wns 0.00
[INFO]: Synthesis was successful
%
```

Placement stage completed with legal cell positions.

```
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vdsquadron: ~/Desktop... x vsduser@vdsquadron: ~/Desktop... x vsduser@vdsquadron: ~/Desktop... x
1 0.00 0.11 0.63 20.87 v _17708_/X (sky130_fd_sc_hd_or2_2)
12752_ (net)
0.13 0.66 21.53 v _17719_/B (sky130_fd_sc_hd_or2_2)
0.13 0.66 21.53 v _17719_/X (sky130_fd_sc_hd_or2_2)
2 0.01 0.13 0.00 21.53 v _17720_/B1 (sky130_fd_sc_hd_o21a_2)
0.06 0.24 21.77 v _17720_/X (sky130_fd_sc_hd_o21a_2)
01675_ (net)
0.06 0.00 21.77 v _25812_/A0 (sky130_fd_sc_hd_mux2_1)
0.10 0.61 22.38 v _25812_/X (sky130_fd_sc_hd_mux2_1)
01677_ (net)
1 0.00 0.10 0.00 22.38 v _26266_/A1 (sky130_fd_sc_hd_mux4_1)
0.15 1.11 23.49 v _26266_/X (sky130_fd_sc_hd_mux4_1)
01678_ (net)
1 0.00 0.15 0.00 23.49 v _25813_/A0 (sky130_fd_sc_hd_mux2_1)
0.12 0.66 24.15 v _25813_/X (sky130_fd_sc_hd_mux2_1)
02529_ (net)
1 0.00 0.12 0.00 24.15 v _13533_/B2 (sky130_fd_sc_hd_o221a_2)
0.07 0.44 24.59 v _13533_/X (sky130_fd_sc_hd_o221a_2)
03989_ (net)
1 0.00 0.07 0.00 24.59 v _27823_/D (sky130_fd_sc_hd_dfxtpt_2)
24.59 data arrival time
-----
0.00 24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _27823_/CLK (sky130_fd_sc_hd_dfxtpt_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-24.59 data arrival time
-----
-0.15 slack (VIOLATED)

wns -24.25
tns -702.94
[INFO]: Global placement was successful
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_05-29/tmp/floorplan/4-to
Placer.def to /openLANE_flow/designs/picorv32a/runs/27-11_05-29/tmp/placement/5-replace.def
[INFO]: Running Basic Macro Placement
[INFO]: current step index: 6
```

Placement running got completed

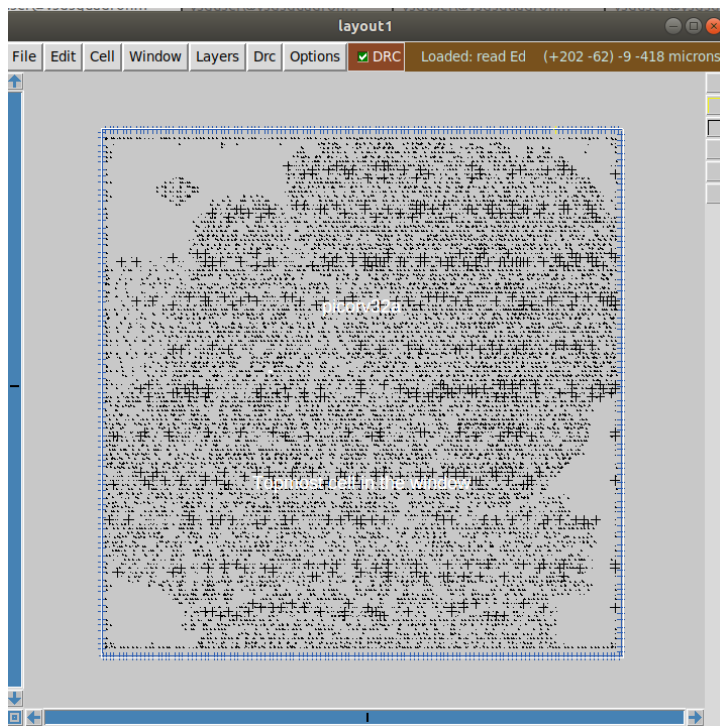
Placement visualization ensuring no overlaps.

```
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vdsquadron: ~/Desktop... x vsduser@vdsquadron: ~/Desktop... x vsduser@vdsquadron: ~/Desktop... x
fixed instances 0
nets 15442
design area 405208.6 u^2
fixed area 0.0 u^2
m_files area 141534.5 u^2
utilization 35 %
utilization padded 52 %
rows 234
row height 2.7 u

Placement Analysis
-----
total displacement 0.0 u
average displacement 0.0 u
max displacement 0.0 u
original HPWL 683631.1 u
legalized HPWL 696797.8 u
delta HPWL 2 %

[INFO DPL-0020] Mirrored 5765 instances
[INFO DPL-0021] HPWL before 696797.8 u
[INFO DPL-0022] HPWL after 683631.1 u
[INFO DPL-0023] HPWL delta -1.9 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/25-11_14-03/tmp/placement/9-re
sizer.def to /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/picorv32a.placem
ent.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/
picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/pl
icorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 13
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klay
out/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/picorv32a.
placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs
.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/p
icorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/plac
ement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
```

Optimized placement



STA report generated.

```
vswdworkshop [Running] - Oracle VirtualBox
File Machine View Input Devices Help

Activities Terminal
vswduser@vswdsquadron: ~/Desktop/work/

File Edit View Search Terminal Tabs Help
vswduser@vswdsquadron: ~/Desktop/work/

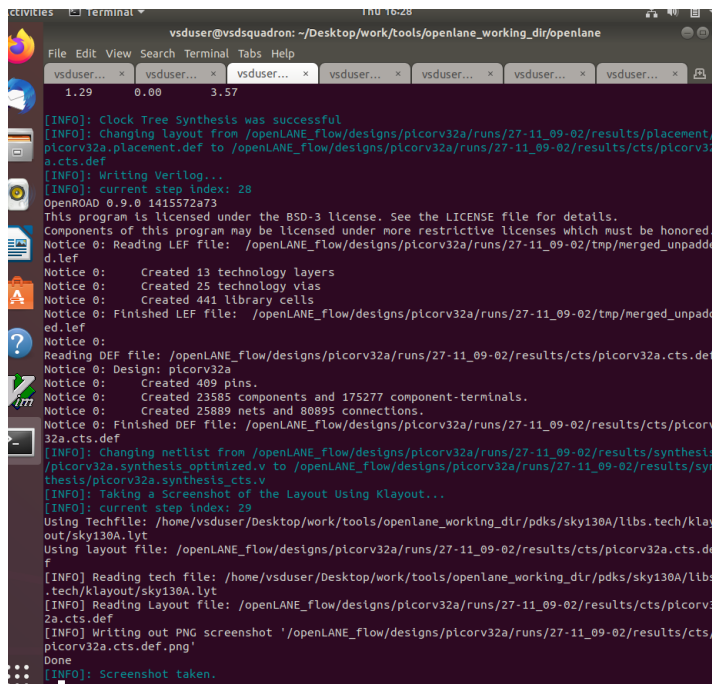
1 0.00 0.18 2.51 10.37 v _42583 /X (sky130_fd_sc_hd_mux4_1)
00361 (net)
0.18 0.00 10.37 v _42586 /A1 (sky130_fd_sc_hd_mux4_1)
0.14 1.14 11.51 v _42586 /X (sky130_fd_sc_hd_mux4_1)
00365 (net)
1 0.00 0.14 0.00 11.51 v _42088 /A1 (sky130_fd_sc_hd_mux2_1)
0.13 0.70 12.22 v _42088 /X (sky130_fd_sc_hd_mux2_1)
00370 (net)
1 0.00 0.13 0.00 12.22 v _21612 /B (sky130_fd_sc_hd_nand2_2)
0.11 0.10 12.38 ^ _21612 /Y (sky130_fd_sc_hd_nand2_2)
18851 (net)
3 0.01 0.11 0.00 12.38 ^ _26230 /B2 (sky130_fd_sc_hd_o221a_2)
0.07 0.37 12.75 ^ _26230 /X (sky130_fd_sc_hd_o221a_2)
01718 (net)
1 0.00 0.07 0.00 12.75 ^ _41953 /A0 (sky130_fd_sc_hd_mux2_1)
0.07 0.21 12.96 ^ _41953 /X (sky130_fd_sc_hd_mux2_1)
01719 (net)
1 0.00 0.07 0.00 12.96 ^ _26230 /A1_N (sky130_fd_sc_hd_a2bb2o_2)
0.08 0.52 13.47 v _26230 /X (sky130_fd_sc_hd_a2bb2o_2)
04123 (net)
1 0.00 0.08 0.00 13.47 v _26239 /C1 (sky130_fd_sc_hd_a311o_2)
0.08 0.56 14.04 v _26239 /X (sky130_fd_sc_hd_a311o_2)
01720 (net)
1 0.00 0.08 0.00 14.04 v _41548 /A0 (sky130_fd_sc_hd_mux2_1)
0.10 0.61 14.65 v _41548 /X (sky130_fd_sc_hd_mux2_1)
21109 (net)
1 0.00 0.10 0.00 14.65 v _42703 /D (sky130_fd_sc_hd_dfxt2_2)
14.65 data arrival time
-----
0.00 12.00 12.00 clock clk (rise edge)
0.00 12.00 clock network delay (ideal)
0.00 12.00 clock reconvergence pessimism
12.00 ^ _42703 /CLK (sky130_fd_sc_hd_dfxt2_2)
-0.31 11.69 library setup time
11.69 data required time
-----
11.69 data required time
-14.65 data arrival time
-----
-2.95 slack (VIOLATED)

tns -266.43
wts -2.95
rts -
```

Set ::env(SYNTH_MAX_FANOUT) 4

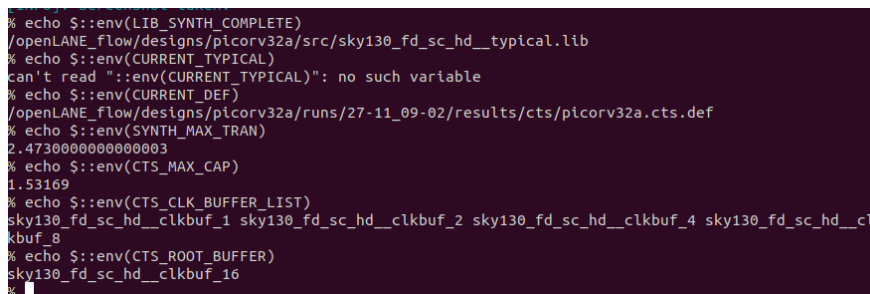
Increased the bufferability of the cells by replacing the cells with higher drive strength

Clock Tree Synthesis (CTS) results displayed.



```
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
1.29 0.00 3.57
[INFO]: Clock Tree Synthesis was successful
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO]: Writing Verilog...
[INFO]: current step index: 28
OpenROAD 0.9.0 141557270
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadded.lef
Notice 0: Reading DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 23885 components and 175277 component-terminals.
Notice 0: Created 25889 nets and 80895 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 29
Using Techfile: /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading layout file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
```

Specifications and timing constraints loaded.



```
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% echo $::env(LIB_SLOWEST)
/openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd__typical.lib
% echo $::env(CURRENT_TYPICAL)
can't read ":env(CURRENT_TYPICAL)": no such variable
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
% echo $::env(SYNTH_MAX_TRAN)
2.4730000000000003
% echo $::env(CTS_MAX_CAP)
1.53169
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd__clkbuf_1 sky130_fd_sc_hd__clkbuf_2 sky130_fd_sc_hd__clkbuf_4 sky130_fd_sc_hd__clkbuf_8
% echo $::env(CTS_ROOT_BUFFER)
sky130_fd_sc_hd__clkbuf_16
%
```

OpenROAD commands loaded for STA analysis.

```
read_lef read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged.lef
read_def read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
write_db pico_cts.db
read_db pico_cts.db
read_verilog /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_cts.v
read_liberty -max $::env(LIB_SLOWEST)
read_liberty -min $::env(LIB_FASTEST)
read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
set_propagated_clock [all_clocks]
report_checks -path_delay min_max -format full_clock_expanded digits 4
```

Slack violation detected post-CTS.

Timing fixed and slack met successfully.

					clock source latency
1	0.0079	0.0225	0.0100	12.0100	^ clk (in)
		0.0225	0.0000	12.0100	^ clk (net)
		0.0283	0.1016	12.1116	^ clkbuf_0_clk/A (sky130_fd_sc_hd__clkbuf_16)
2	0.0044			12.1116	^ clkbuf_0_clk/X (sky130_fd_sc_hd__clkbuf_16)
		0.0283	0.0000	12.1116	^ clknet_0_clk (net)
		0.0388	0.0697	12.1814	^ clkbuf_1_1_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
1	0.0022			12.1814	^ clkbuf_1_1_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0388	0.0000	12.1814	^ clknet_1_1_0_clk (net)
		0.0635	0.0910	12.2724	^ clkbuf_1_1_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
2	0.0044			12.2724	^ clkbuf_1_1_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0635	0.0000	12.2724	^ clknet_1_1_1_clk (net)
		0.0390	0.0811	12.3535	^ clkbuf_2_3_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
1	0.0022			12.3535	^ clkbuf_2_3_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0390	0.0000	12.3535	^ clknet_2_3_0_clk (net)
		0.0635	0.0911	12.4446	^ clkbuf_2_3_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
2	0.0044			12.4446	^ clkbuf_2_3_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0635	0.0000	12.4446	^ clknet_2_3_1_clk (net)
		0.0635	0.0987	12.5433	^ clkbuf_3_7_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
2	0.0044			12.5433	^ clkbuf_3_7_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0635	0.0000	12.5433	^ clknet_3_7_0_clk (net)
		0.0635	0.0000	12.6421	^ clkbuf_4_15_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
2	0.0044			12.6421	^ clkbuf_4_15_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.0635	0.0000	12.6421	^ clknet_4_15_0_clk (net)
		0.3758	0.3142	12.9563	^ clkbuf_5_30_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
4	0.0316			12.9563	^ clkbuf_5_30_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
		0.3758	0.0000	12.9563	^ clknet_5_30_0_clk (net)
6)					^ clkbuf_leaf_199_clk/A (sky130_fd_sc_hd__clkbuf_1)
6)		0.0405	0.2075	13.1638	^ clkbuf_leaf_199_clk/X (sky130_fd_sc_hd__clkbuf_1)
5	0.0094				^ clknet_leaf_199_clk (net)
		0.0405	0.0000	13.1638	^ _48096_/CLK (sky130_fd_sc_hd__dfxtp_1)
			0.0000	13.1638	^ clock reconvergence pessimism
			-0.1068	13.0570	library setup time
				13.0570	data required time
				13.0570	data required time
				-7.7209	data arrival time
				5.3361	slack (MET)

PDN generation process started.

```
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
%
%
%
%
% gen_pdn
```

```
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on
a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 27491.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/floorplan/30-pdn.def
%
```

```
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadd
ed.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 23585 components and 175277 component-terminals.
Notice 0: Created 25889 nets and 80895 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/l
ibs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0009] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Type: stdcell, grid
Stdcell Rails
Layer: met1 - width: 0.480 pitch: 2.720 offset: 0.000
Straps
Layer: met4 - width: 1.600 pitch: 153.600 offset: 16.320
Layer: met5 - width: 1.600 pitch: 153.180 offset: 16.650
Connect: {met4 met5} {met1 met4}
Type: macro, macro_1
Macro orientation: R0 R180 MX MY R90 R270 MXR90 MYR90
Straps
Connect: {met4_PIN_ver met5}
[INFO] [PDNG-0012] **** END INFO ****
```


PDN information showing power rails and pitch.

Routing stage initiated connecting all components.

```
[INFO]: Calculating Runtime From the Start...  
[INFO]: Routing completed for picorv32a/28-11_11-41 in 0h18m22s  
%
```