

Digital VLSI SoC design and planning @ 21 Nov 2025 – 30 Nov 2025

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OpenLANE environment is set up and synthesis tool initialized for SKY130 PDK.

Synthesis completed showing total cell count and DFF statistics.

Synthesis completed.

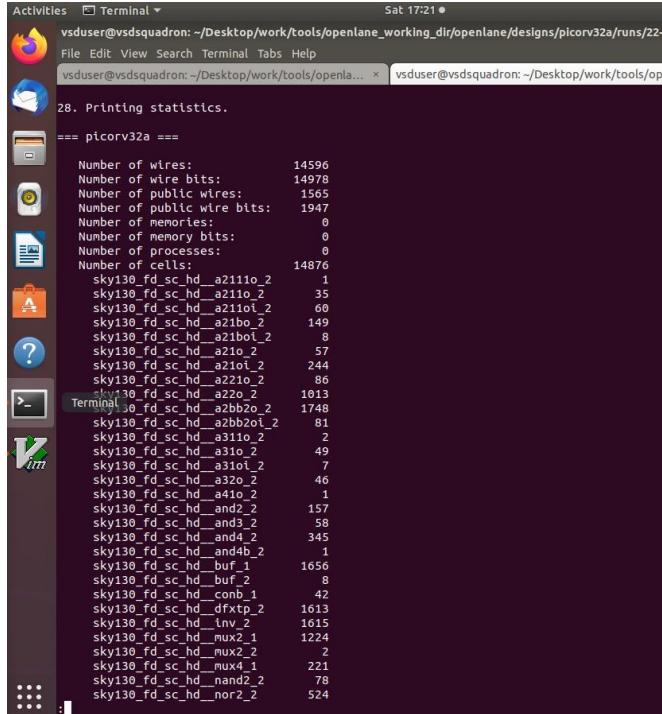
No of cells = 14876

DFF=1613 (D-flipflops)

DFF Ratio = (no of FF/ Total no of Cells) *100

Ratio=10.8%

Floorplan stage begins showing switches used for configuring layout.



```
Activities Terminal Sat 17:21 ●
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/22-1
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane... x vsduser@vsdsquadron: ~/Desktop/work/tools/open...
28. Printing statistics.

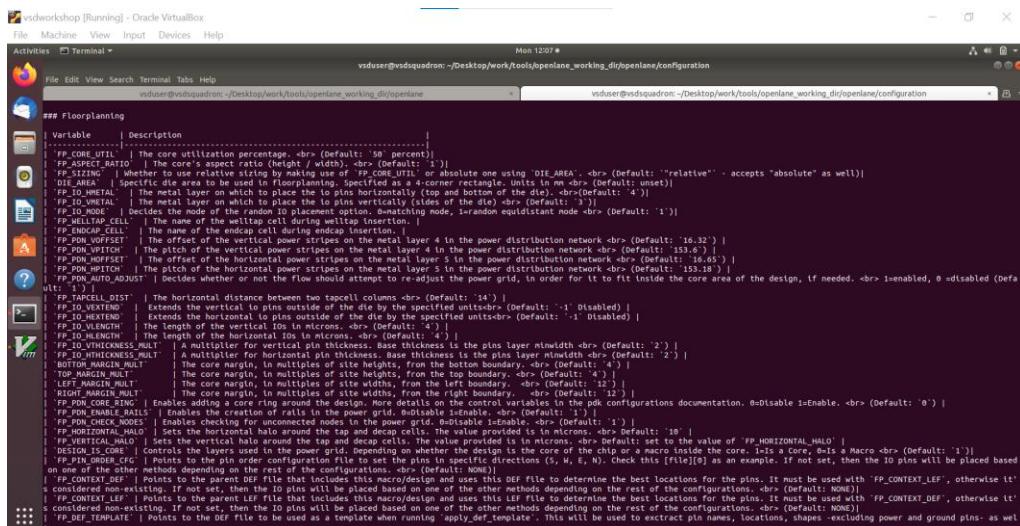
== picorv32a ==

Number of Wires: 14596
Number of wire bits: 14978
Number of public wires: 1565
Number of public wire bits: 1947
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 14876
    sky130_fd_sc_hd_a211o_2 1
    sky130_fd_sc_hd_a211o_2 35
    sky130_fd_sc_hd_a211o_2 66
    sky130_fd_sc_hd_a21b0_2 149
    sky130_fd_sc_hd_a21b0_2 8
    sky130_fd_sc_hd_a21o_2 57
    sky130_fd_sc_hd_a21o_2 244
    sky130_fd_sc_hd_a221o_2 86
    sky130_fd_sc_hd_a22o_2 1013
    sky130_fd_sc_hd_a2bb2o_2 1748
    sky130_fd_sc_hd_a2bb2o_2 81
    sky130_fd_sc_hd_a311o_2 2
    sky130_fd_sc_hd_a311o_2 49
    sky130_fd_sc_hd_a31o_2 7
    sky130_fd_sc_hd_a32o_2 46
    sky130_fd_sc_hd_a41o_2 1
    sky130_fd_sc_hd_and2_2 157
    sky130_fd_sc_hd_and3_2 58
    sky130_fd_sc_hd_and4_2 345
    sky130_fd_sc_hd_and4b_2 1
    sky130_fd_sc_hd_buf_1 1656
    sky130_fd_sc_hd_buf_2 8
    sky130_fd_sc_hd_corb_1 42
    sky130_fd_sc_hd_dfxtp_2 1613
    sky130_fd_sc_hd_inv_2 1615
    sky130_fd_sc_hd_mux2_1 1224
    sky130_fd_sc_hd_mux2_2 2
    sky130_fd_sc_hd_mux4_1 221
    sky130_fd_sc_hd_nand2_2 78
    sky130_fd_sc_hd_nor2_2 524
```

Floorplan

This are the switches used in the floorplan.

Default floorplan settings such as aspect ratio and utilization displayed.



```
Activities Terminal Mon 12:07 ●
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration x vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration
## Floorplanning

## Variable Description
#CORE_UTIL | The core utilization percentage. <br> (Default: 50 percent)
#ASPECT_RATIO | The core's aspect ratio (height / width). <br> (Default: 1')
#SIZING | Whether to use relative sizing by making use of 'FP_UTIL' instead of absolute values. This includes using 'OIE_AREA'. <br> (Default: "relative" - accepts "absolute" as well)
#IO_PLACEMENT | The placement of the IO pins. Options include using a 4-corner rectangle, units in nm or 'unset'. <br> (Default: unset)
#IO_Metal | The metal layer on which to place the IO pins horizontally (top and bottom of the die). <br> (Default: 4')
#IO_VMETAL | The metal layer on which to place the IO pins vertically (sides of the die). <br> (Default: 3')
#WELTAP_CELL | The name of the weltap cell during weltap insertion. <br> (Default: '')
#ENCAP_CELL | The name of the encap cell during endcap insertion. <br> (Default: '')
#PON_OFFSET | The offset from the power distribution network layer 4 in the power distribution network. <br> (Default: 16.32') |
#PON_VPITCH | The pitch of the vertical power stripes on the metal layer 4 in the power distribution network. <br> (Default: 153.6') |
#PON_HOFFSET | The offset of the pitch of the horizontal power stripes on the metal layer 5 in the power distribution network. <br> (Default: 16.65') |
#PON_AUTO_ADJUST | Indicates whether or not the router will attempt to re-adjust the power grid, in order for it to fit inside the core area of the design, if needed. <br> 1=enabled, 0 =disabled (Defa ult: 1')
#CELL_DIST | The horizontal distance between two topcell columns. <br> (Default: '1')
#IO_VEXTEND | Extends the vertical to pins outside of the die by the specified units. <br> (Default: '-1' Disabled) |
#IO_HORIZONTAL | Extends the horizontal to pins outside of the die by the specified units. <br> (Default: '-1' Disabled) |
#IO_VLENGTH | The length of the vertical extension of the IO pins in microns. <br> (Default: '1')
#IO_VTHICKNESS | A multiplier for vertical pin thickness. Base thickness is the pins layer linewidth. <br> (Default: '2') |
#IO_HTHICKNESS | A multiplier for horizontal pin thickness. Base thickness is the pins layer linewidth. <br> (Default: '2') |
#IO_MARGIN | The core margin, in multiples of site widths, from the top boundary. <br> (Default: '4') |
#TOP_MARGIN_MULT | The core margin, in multiples of site heights, from the top boundary. <br> (Default: '4') |
#LEFT_MARGIN_MULT | The core margin, in multiples of site widths, from the left boundary. <br> (Default: '12') |
#RIGHT_MARGIN_MULT | The core margin, in multiples of site heights, from the right boundary. <br> (Default: '12') |
#PON_CORE_RING | Enables adding a core ring around the design. More details on the control variables in the pdk configurations documentation. <b>=Disable</b> isEnable. <br> (Default: '0') |
#PON_ENABLE_RAILS | Enables the creation of rails in the power grid. <b>=Disable</b> isEnable. <br> (Default: '0') |
#PON_VHORIZONTAL | Sets the vertical halo around the vertical decaps. The value provided is in microns. <br> (Default: '1') |
#PON_HORIZONTAL | Sets the horizontal halo around the tap and decap cells. The value provided is in microns. <br> (Default: '10') |
#VERTICAL_HALO | Sets the vertical halo around the tap and decap cells. The value provided is in microns. <br> (Default: set to the value of '#HORIZONTAL_HALO' |
#HORIZONTAL_HALO | Sets the horizontal halo around the tap and decap cells. The value provided is in microns. <br> (Default: set to the value of '#VERTICAL_HALO' |
#PIN_ORDER_CFG | Points to the pin order configuration file to set the pins in specific directions (S, W, E, N). Check this [file]@[] as an example. If not set, then the IO pins will be placed based on one of the other methods depending on the rest of the configurations. <br> (Default: NONE) |
#CONTEXT_DEF | Points to the context DEF file to determine the best locations for the pins. It must be used with 'FP_CONTEXT_LEF', otherwise it's considered non-existing. If not set, then the IO pins will be placed based on one of the other methods depending on the rest of the configurations. <br> (Default: NONE) |
#CONTEXT_LEF | Points to the parent LEF file that includes this macro/design and uses this LEF file to determine the best locations for the pins. It must be used with 'FP_CONTEXT_DEF', otherwise it's considered non-existing. If not set, then the IO pins will be placed based on one of the other methods depending on the rest of the configurations. <br> (Default: NONE) |
#DEF_TEMPLATE | Points to the DEF file to be used as a template when running apply_def_template. This will be used to extract pin names, locations, shapes -excluding power and ground pins- as well
```

Execution of run_floorplan command generating required floorplan files.

System default settings.

```
# Floorplan defaults
set ::env(FP_IO_VMETAL) 3
set ::env(FP_IO_HMETAL) 4

set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
set ::env(FP_IO_HTHICKNESS_MULT) 2

set ::env(BOTTOM_MARGIN_MULT) 4
set ::env(TOP_MARGIN_MULT) 4
set ::env(LEFT_MARGIN_MULT) 12
set ::env(RIGHT_MARGIN_MULT) 12

set ::env(FP_HORIZONTAL_HALO) 10
set ::env(FP_VERTICAL_HALO) ${::env(FP_HORIZONTAL_HALO)}

set ::env(DESIGN_IS_CORE) 1
(END)
```

floorplan.

Run_floorplan (is the command used for the running the floorplan)

All floorplan run files created including DEF and config outputs.

```
File Edit View Search Terminal Tabs Help vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
```

```
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ./openlane/runs/24-11_96-47/tmp/floorplan
WARNING PSM-0037] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 180.470um).
WARNING PSM-0038] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 180.470um).
WARNING PSM-0039] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 333.650um).
WARNING PSM-0040] Vsrc location at (145.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 103.880um).
WARNING PSM-0041] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 486.830um).
WARNING PSM-0042] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 486.830um).
WARNING PSM-0043] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 486.830um).
WARNING PSM-0044] Vsrc location at (425.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 333.650um).
WARNING PSM-0045] Vsrc location at (285.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 333.650um).
WARNING PSM-0046] Vsrc location at (285.520um, 370.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 640.810um).
WARNING PSM-0047] Vsrc location at (425.520um, 370.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 640.810um).
WARNING PSM-0048] Vsrc location at (425.520um, 510.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
INFO PSM-0031] Number of nodes on net VPHB is 20800.
INFO PSM-0037] G matrix created successfully.
INFO PSM-0040] Connection between all PDN nodes established in net VPHB.
WARNING PSM-0038] Vsrc location at (145.520um, 10.880um) and size not specified, defaulting pad location to checkerboard pattern on core area.
WARNING PSM-0039] X direction bump pitch is not specified, defaulting to 140um.
WARNING PSM-0040] Y direction bump pitch is not specified, defaulting to 140um.
WARNING PSM-0041] Using voltage 0.000V for ground network.
WARNING PSM-0021] Using voltage 0.000V for ground network.
INFO PSM-0026] Creating G matrix.
INFO PSM-0028] Extracting point stripes on net VDDC.
WARNING PSM-0030] Vsrc location at (5.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 103.880um).
WARNING PSM-0031] Vsrc location at (145.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 103.880um).
WARNING PSM-0032] Vsrc location at (285.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
WARNING PSM-0033] Vsrc location at (425.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
WARNING PSM-0034] Vsrc location at (565.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 103.880um).
WARNING PSM-0035] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
WARNING PSM-0036] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
WARNING PSM-0037] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 103.880um).
WARNING PSM-0038] Vsrc location at (285.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
WARNING PSM-0039] Vsrc location at (425.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
WARNING PSM-0040] Vsrc location at (285.520um, 370.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
WARNING PSM-0041] Vsrc location at (425.520um, 370.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
WARNING PSM-0042] Vsrc location at (285.520um, 510.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
WARNING PSM-0043] Vsrc location at (425.520um, 510.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
INFO PSM-0037] G matrix created successfully.
INFO PSM-0040] Connection between all PDN nodes established in net VDDC.
INFO PSM-0041] PDN generation was successful.
INFO PSM-0042] Changing layout from /openlane_flow/designs/plcorv32a/runs/24-11_96-47/results/floorplan/plcorv32a.floorplan.def to /openlane_flow/designs/plcorv32a/runs/24-11_96-47/tmp/floorplan
```

All the run files got created for the floorplan.

Generated floorplan DEF visualizing core boundaries and IO pin positions.

```

y130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a$ cd runs
/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs$ ll
total 24
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:17 .
drwxr-xr-x 4 vsduser docker 4096 Nov 22 15:29 ..
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 15:36 22-11_09-59/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 17:08 22-11_11-37/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 22 22:30 22-11_17-00/
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:20 24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs$ cd
24-11_06-47/
logs/ reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs$ cd
24-11_06-47/
logs/ reports/ results/ tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs$ cd
24-11_06-47/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs/24-
11_06-47$ ll
total 68
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:20 .
drwxr-xr-x 6 vsduser vsduser 4096 Nov 24 12:17 ..
-rw-r--r-- 1 vsduser vsduser 4743 Nov 24 12:20 cmds.log
-rw-r--r-- 1 vsduser vsduser 21023 Nov 24 12:20 config.tcl
-rw-r--r-- 1 vsduser vsduser 241 Nov 24 12:18 error.log
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:17 logs/
-rw-r--r-- 1 vsduser vsduser 15 Nov 24 12:17 OPENLANE_VERSION
-rwxr-xr-x 1 vsduser vsduser 170 Jun 28 2021 PDK_SOURCES*
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:18 reports/
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:17 results/
drwxr-xr-x 11 vsduser vsduser 4096 Nov 24 12:19 tmp/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picrv32a/runs/24-
11_06-47$ ls
cmds.log config.tcl error.log logs OPENLANE_VERSION PDK_SOURCES reports results tmp

```

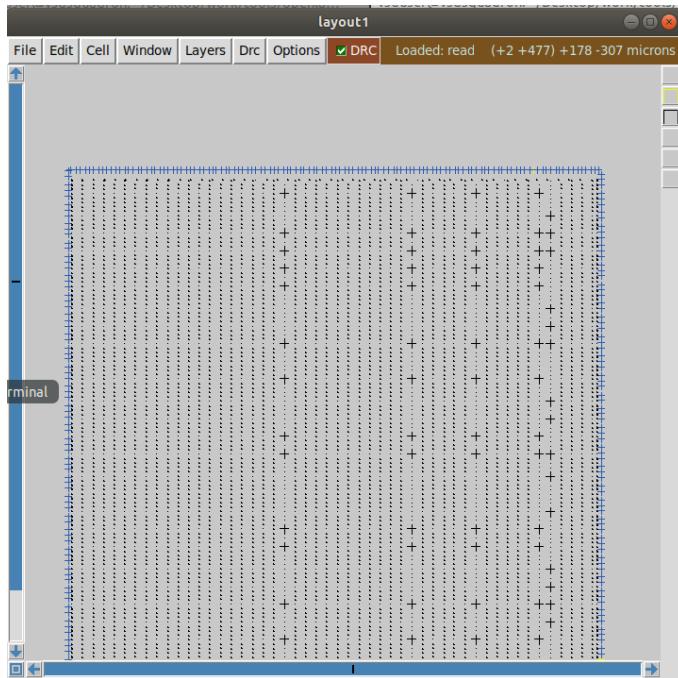
Cell rows and placement boundaries from floorplanning are shown.

```

VERSION 5.8 ;
DIVIDERCHAR "/";
BUSBITCHARS "[]";
DESIGN picrv32a ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 660685 671405 ) ;
ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_19 unithd 5520 62560 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_20 unithd 5520 65280 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_21 unithd 5520 68000 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_22 unithd 5520 70720 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_23 unithd 5520 73440 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_24 unithd 5520 76160 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_25 unithd 5520 78880 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_26 unithd 5520 81600 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_27 unithd 5520 84320 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_28 unithd 5520 87040 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_29 unithd 5520 89760 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_30 unithd 5520 92480 FS DO 1412 BY 1 STEP 460 0 ;
ROW ROW_31 unithd 5520 95200 N DO 1412 BY 1 STEP 460 0 ;
ROW ROW_32 unithd 5520 97920 FS DO 1412 BY 1 STEP 460 0 ;

```

created the floorplan.



Global placement running to arrange standard cells optimally.

```
picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/def
1
% run_placement
```

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlan... x vsduser@vsdsquadron:~/Desktop/work/tools/openlan... x
fixed instances          6354
nets                      15449
design area      426473.3 u^2
fixed area        9141.3 u^2
movable area     147800.5 u^2
utilization       36 %
utilization padded   55 %
rows                  238
row height           2.7 u

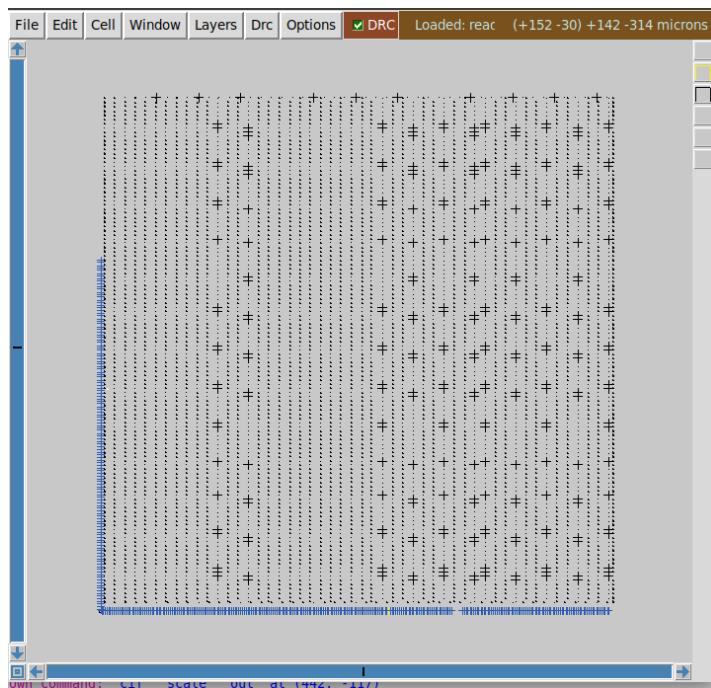
Placement Analysis
-----
total displacement      0.0 u
average displacement    0.0 u
max displacement        0.0 u
original HPWL      766080.0 u
legalized HPWL     779196.5 u
delta HPWL            2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after      766080.0 u
[INFO DPL-0023] HPWL delta     -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-11_06-47/tmp/placement/9-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def
[INFO]: Taking a screenshot of the Layout Using Klayout...
[INFO]: current step index: 13
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def
[INFO]: Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO]: Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def
[INFO]: Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-11_06-47/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
```

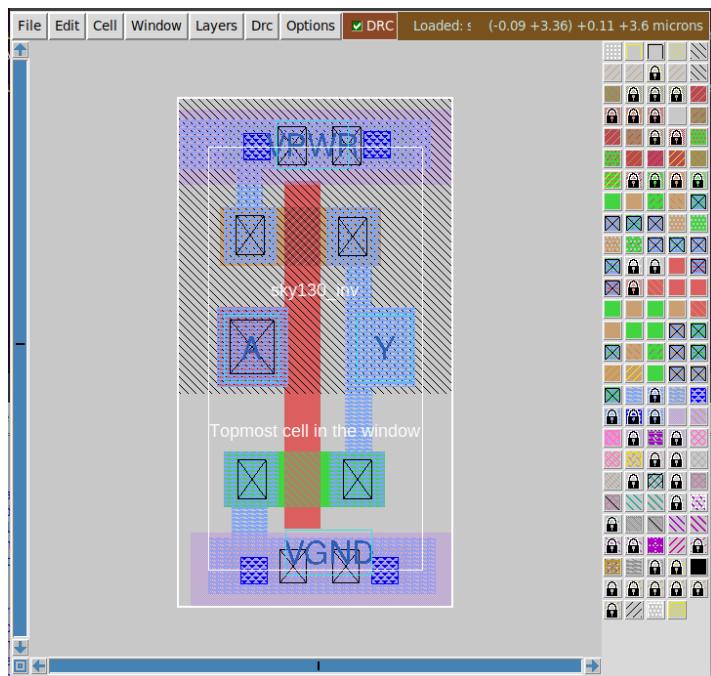
IO configuration set to 2 for improved pin distribution.

```
[INFO]: SCREENSHOT TAKEN.  
% set ::env(FP_IO_MODE) 2  
2  
% run_floorplan
```

Standard cells arrangement visible for placement and routing.



Flow for generating SPICE netlist of inverter shown.



Flow for spice of an inverter.

```

sky130_inv.spice (-/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=0.01u
4 .include ./libs/pshort.lib
5 .include ./libs/nshort.lib
6
7 // .subckt sky130_inv A Y VPWR VGND
8 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23 ad=1443 pd=152 as=1517 ps=156
9 M1001 Y A VGND VGND nshort_model.0 w=35 l=23 ad=1435 ps=148 as=1365 ps=1481
10 VDD VPWR 0 3.3v
11 VSS VGND 0 0v
12 Va A VGND PULSE(0V 3.3V 0.01ns 2ns 4ns)
13 C0 A Y 0.05fF
14 C1 Y VPWR 0.11fF
15 C2 A VPWR 0.07fF
16 C3 Y 0 0.24fF
17 C4 VPWR 0 0.59fF
18
19 // .ends
20
21 .tran 1n 20n
22
23 .control
24 run
25 .endc
26 .end

```

Inverter schematic with PMOS/NMOS connections displayed.

```

Activities Terminal Mon 16:13 ●
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane... x vsduser@vsdsquadron:~/Desktop/work/tools/openlane... x
# .ends
unknown device type - error
Error on line 21 :
    .tran 1 20n
unimplemented control card - error
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

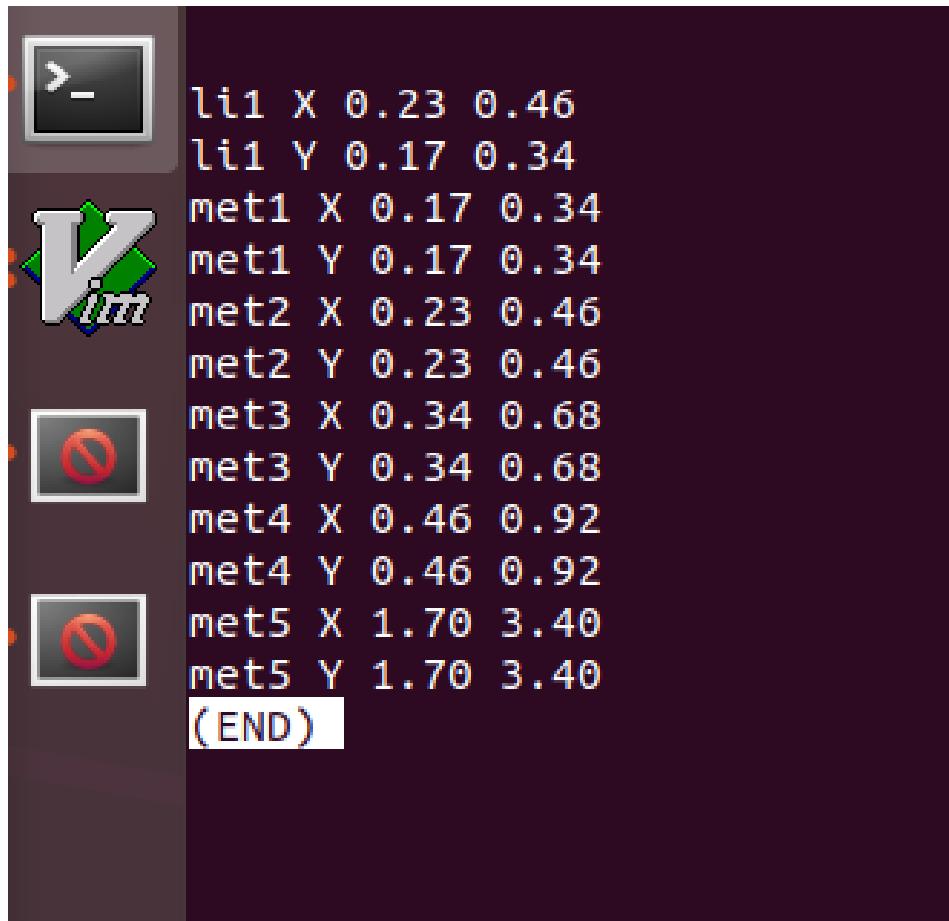
Warning: va: no DC value, transient time 0 value used
ngspice: 1 -> exit
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice
sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
***** 

Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
----          -----
y              3.3
a              0
vpwr           3.3
vgnd           0
va#branch     0
vss#branch    3.32378e-12
vdd#branch    -3.3238e-12

No. of Data Rows : 71
ngspice 1 -> 5

```

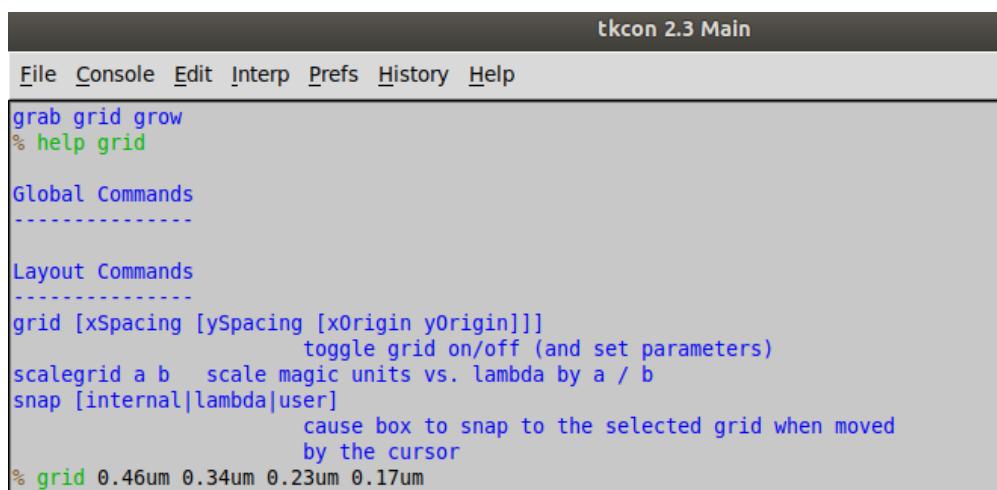
Track information generated for metal routing alignment.



The screenshot shows a terminal window running Vim. The buffer contains a list of track coordinates:

```
li1 X 0.23 0.46
li1 Y 0.17 0.34
met1 X 0.17 0.34
met1 Y 0.17 0.34
met2 X 0.23 0.46
met2 Y 0.23 0.46
met3 X 0.34 0.68
met3 Y 0.34 0.68
met4 X 0.46 0.92
met4 Y 0.46 0.92
met5 X 1.70 3.40
met5 Y 1.70 3.40
(END)
```

Track mapping showing metal layer pitches and routing lanes.



The screenshot shows the tkcon 2.3 Main interface. The menu bar includes File, Console, Edit, Interp, Prefs, History, and Help. The console window displays the following text:

```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
grab grid grow
% help grid

Global Commands
-----
Layout Commands
-----
grid [xSpacing [ySpacing [xOrigin yOrigin]]]
    toggle grid on/off (and set parameters)
scalegrid a b    scale magic units vs. lambda by a / b
snap [internal|lambda|user]
    cause box to snap to the selected grid when moved
    by the cursor
% grid 0.46um 0.34um 0.23um 0.17um
```

We will extracted the lef of this standard cell. And will include that lef in the synthesis. This the image of no of inv add in the design

```

File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron:~/Desktop/work/tool... x vsduser@vsdsquadron:~/Desktop/work/tool... x vsduser@vsdsquadron:~/Desktop/work/tool... x
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module 'picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module 'picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: 2fc7fe1170, CPU: user 17.66s system 0.18s, MEM: 96.07 MB peak
Yosys 0.9+3621 (git hash: 84e9f7a7, gcc 8.3.1 -fPIC -O5)
Time spent: 65% 2x abc (36 sec), 9% 33x opt_expr (5 sec), ...
[INFO]: Changing netlist from 8 to /openLANE_flow/designs/picorv32a/runs/25-11_13-01/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current_step index: 2
OpenSTA 2.3.0 38b40393a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set Input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(I_O_PCT)]
set Output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(O_PCT)]
puts "[INFO]: Setting output delay to: $Output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "[INFO]: Setting input delay to: $Input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk $rst_indx $rst_indx
# correct reset
set_input_delay $Input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $Output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TDDI cell as parameter
set_driving_cell_lth_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
%

```

After we set some strategies

Set ::env(SYNTH_STRATEGY) "DELAY 1"

Set ::env(SYNTH_SIZING) 1

Floorplan run completed successfully.

```

File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron:~/Desktop/work/tool... x vsduser@vsdsquadron:~/Desktop/work/tool... x vsduser@vsdsquadron:~/Desktop/work/tool... x vsduser@vsdsquadron:~/Desktop/work/tool... x
29. Executing Verilog backend.
Dumping module 'picorv32a'.

Warnings: 307 unique messages, 287 total
End of script. Logfile hash: 2ce92bbb, CPU: user 19.30s system 0.19s, MEM: 96.89 MB peak
Yosys 0.9+3621 (git hash: 84e9f7a7, gcc 8.3.1 -fPIC -O5)
Time spent: 65% 2x abc (36 sec), 9% 33x opt_expr (5 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/25-11_13-34/results/synthesis/picorv32a.synthesis.v to
thesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current_step index: 7
OpenSTA 2.3.0 38b40393a8 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set Input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(I_O_PCT)]
set Output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(O_PCT)]
puts "[INFO]: Setting output delay to: $Output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "[INFO]: Setting input delay to: $Input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk $rst_indx $rst_indx
# correct reset
set_input_delay $Input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $Output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TDDI cell as parameter
set_driving_cell_lth_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
%
```

Placement stage completed with legal cell positions.

```
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop... x vsduser@vsdsquadron: ~/Desktop... x vsduser@vsdsquadron: ~/Desktop... x
1 0.00      0.11  0.63  20.87 v _17708/_X (sky130_fd_sc_hd__or2_2)
           0.11  0.00  20.87 v _17719/_B (sky130_fd_sc_hd__or2_2)
           0.13  0.66  21.53 v _17719/_X (sky130_fd_sc_hd__or2_2)
2 0.01      0.13  0.00  21.53 v _17720/_B1 (sky130_fd_sc_hd__o21a_2)
           0.06  0.24  21.77 v _17720/_X (sky130_fd_sc_hd__o21a_2)
           0.13  0.00  21.77 v _17720/_B1 (sky130_fd_sc_hd__o21a_2)
2 0.00      0.06  0.00  21.77 v _25812/_A0 (sky130_fd_sc_hd__mux2_1)
           0.10  0.61  22.38 v _25812/_X (sky130_fd_sc_hd__mux2_1)
           0.10  0.00  22.38 v _26266/_A1 (sky130_fd_sc_hd__mux4_1)
           0.15  1.11  23.49 v _26266/_X (sky130_fd_sc_hd__mux4_1)
1 0.00      0.15  0.00  23.49 v _25813/_A0 (sky130_fd_sc_hd__mux2_1)
           0.12  0.66  24.15 v _25813/_X (sky130_fd_sc_hd__mux2_1)
1 0.00      0.12  0.00  24.15 v _13533/_B2 (sky130_fd_sc_hd__o221a_2)
           0.07  0.44  24.59 v _13533/_X (sky130_fd_sc_hd__o221a_2)
1 0.00      0.07  0.00  24.59 v _27823/_D (sky130_fd_sc_hd__dfxtp_2)
           0.07  0.00  24.59 data arrival time
           0.00  24.73  24.73 clock clk (rise edge)
           0.00  24.73  24.73 clock network delay (ideal)
           0.00  24.73  24.73 clock reconvergence pessimism
           -0.29 24.44  24.44 ^ _27823/_CLK (sky130_fd_sc_hd__dfxtp_2)
           -0.29 24.44  24.44 library setup time
           -0.29 24.44  24.44 data required time
           -0.29 24.44  24.44 data required time
           -0.29 24.44  24.44 data arrival time
           -0.15 slack (VIOLATED)

wns -24.25
tns -702.94
[INFO]: Global placement was successful
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_05-29/tmp/floorplan/4-io
Placer.def to /openLANE_flow/designs/picorv32a/runs/27-11_05-29/tmp/placement/5-replace.def
[INFO]: Running Basic Macro Placement
[INFO]: current step index: 6
```

Placement running got completed

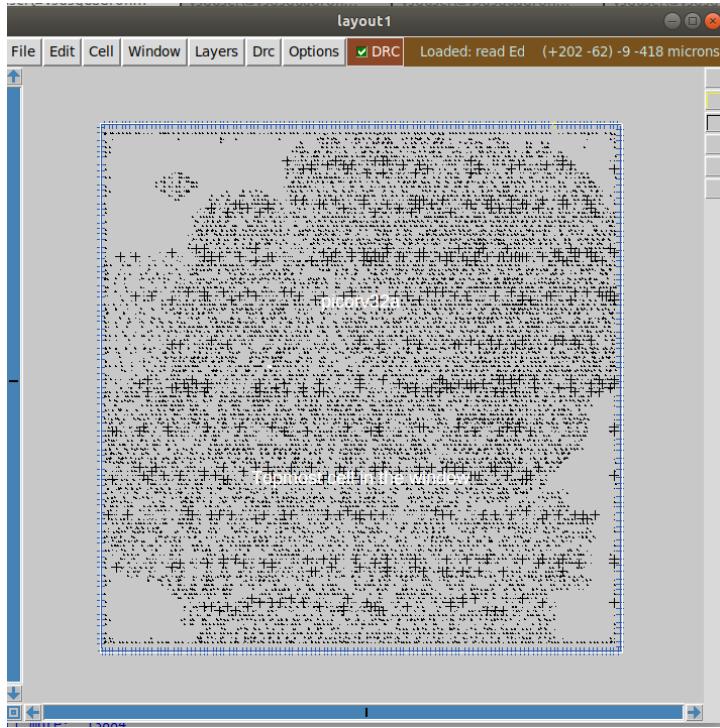
Placement visualization ensuring no overlaps.

```
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop... x vsduser@vsdsquadron: ~/Desktop... x vsduser@vsdsquadron: ~/Desktop... x
fixed instances      0
nets                15442
design area         405208.6 u^2
fixed area          0.0 u^2
area               141534.5 u^2
utilization         35 %
utilization padded 52 %
rows                234
row height          2.7 u

Placement Analysis
-----
total displacement   0.0 u
average displacement 0.0 u
max displacement    0.0 u
original HPWL       683631.1 u
legalized HPWL       696797.8 u
delta HPWL           2 %

[INFO DPL-0020] Mirrored 5765 instances
[INFO DPL-0021] HPWL before      696797.8 u
[INFO DPL-0022] HPWL after       683631.1 u
[INFO DPL-0023] HPWL delta      -1.9 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/25-11_14-03/tmp/placement/9-re
sizer.def to /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/picorv32a.placem
ent.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/
picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/pi
corv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 13
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klay
out/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/picorv32a.
placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs
.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/placement/p
icorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/25-11_14-03/results/plac
ement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
```

Optimized placement



STA report generated.

```
vsdworkshop [Running] - Oracle VirtualBox
File Machine View Input Devices Help
Activities Terminal Thu 15
vsduser@vsdsquadron: ~/Desktop/work/
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron:~/Desktop/... x vsduser@vsdsquadron:~/Desktop/... x vsduser@vsdsquadron:~/Desktop/... x vsduser@vsdsquadron:~/Desktop/...
  0.18 2.51 10.37 v _42583/_X (sky130_fd_sc_hd_mux4_1)
  0.18 0.00 10.37 v _42586/_A1 (sky130_fd_sc_hd_mux4_1)
  0.14 1.14 11.51 v _42586/_X (sky130_fd_sc_hd_mux4_1)
  0.14 0.00 11.51 v _42688/_A1 (sky130_fd_sc_hd_mux2_1)
  0.13 0.78 12.22 v _42688/_X (sky130_fd_sc_hd_mux2_1)
  0.13 0.00 12.22 v _21612/_B (sky130_fd_sc_hd_nand2_2)
  0.11 0.16 12.38 ^ _21612/_Y (sky130_fd_sc_hd_nand2_2)
  0.11 0.00 12.38 ^ _26230/_B2 (sky130_fd_sc_hd_o2z1a_2)
  0.07 0.37 12.75 ^ _26230/_X (sky130_fd_sc_hd_o2z1a_2)
  0.07 0.00 12.75 ^ _41953/_A0 (sky130_fd_sc_hd_mux2_1)
  0.07 0.21 12.96 ^ _41953/_X (sky130_fd_sc_hd_mux2_1)
  0.07 0.00 12.96 ^ _26238/_A1_N (sky130_fd_sc_hd_a2bb2o_2)
  0.08 0.52 13.47 v _26238/_X (sky130_fd_sc_hd_a2bb2o_2)
  0.08 0.00 13.47 v _26239/_C1 (sky130_fd_sc_hd_a311o_2)
  0.08 0.56 14.04 v _26239/_X (sky130_fd_sc_hd_a311o_2)
  0.08 0.00 14.04 v _41548/_A0 (sky130_fd_sc_hd_mux2_1)
  0.10 0.61 14.65 v _41548/_X (sky130_fd_sc_hd_mux2_1)
  0.10 0.00 14.65 v _42703/_D (sky130_fd_sc_hd_dfxtp_2)
  14.65 data arrival time

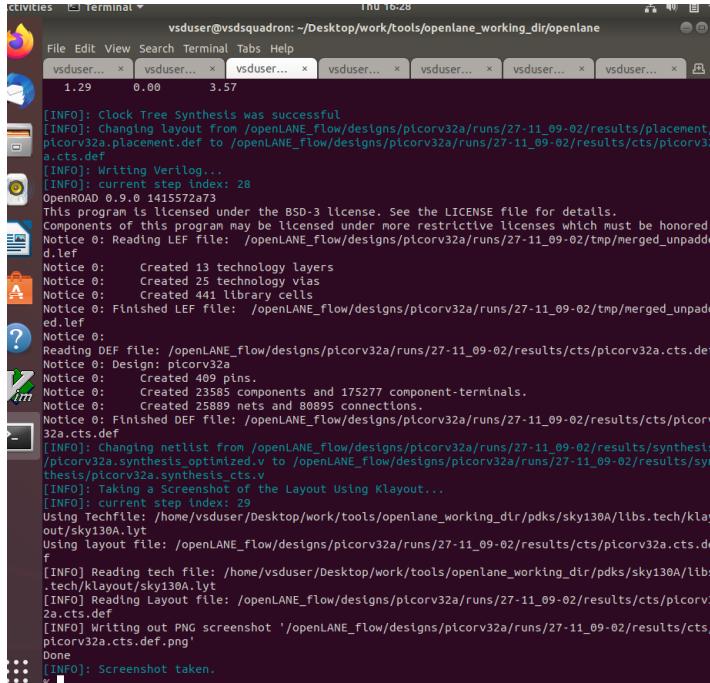
  0.00 12.00 12.00 clock clk (rise edge)
  0.00 12.00 clock network delay (ideal)
  0.00 12.00 clock reconvergence pessimism
  12.00 ^ _42703/_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.31 11.69 library setup time
  11.69 data required time
-14.65 data arrival time
-----+-----+
  11.69 data required time
-14.65 data arrival time
-----+-----+
-2.95 slack (VIOLATED)

tns -266.43
wns -2.95
as -
```

Set ::env(_SYNTH_MAX_FANOUT) 4

Increased the bufferability of the cells by replacing the cells with higher drive strength

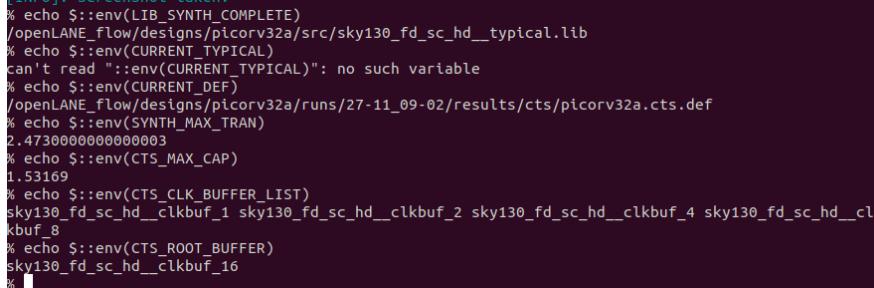
Clock Tree Synthesis (CTS) results displayed.



```
File Edit View Search Terminal Tabs Help
vsduser... x vsduser... x vsduser... x vsduser... x vsduser... x vsduser... x
1.29 0.00 3.57

[INFO]: Clock Tree Synthesis was successful
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO]: Writing Verilog...
[INFO]: current step index: 28
OpenROAD 0.9.0 1415f572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vlas
Notice 0: Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadded.lef
Notice 0: Reading DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 23585 components and 175277 component-terminals.
Notice 0: Created 25889 nets and 80895 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 29
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/lbs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/lbs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
```

Specifications and timing constraints loaded.



```
% echo ::env(LIB_SYNTH_COMPLETE)
/openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd__typical.lib
% echo ::env(CURRENT_TYPICAL)
can't read "::env(CURRENT_TYPICAL)": no such variable
% echo ::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
% echo ::env(SYNTH_MAX_TRAN)
2.4730000000000003
% echo ::env(CTS_MAX_CAP)
1.53169
% echo ::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd__clkbuf_1 sky130_fd_sc_hd__clkbuf_2 sky130_fd_sc_hd__clkbuf_4 sky130_fd_sc_hd__clkbuf_8
% echo ::env(CTS_ROOT_BUFFER)
sky130_fd_sc_hd__clkbuf_16
%
```

OpenROAD commands loaded for STA analysis.

```
read_lef read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged.lef
read_def read_def /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
write_db pico_cts.db
read_db pico_cts.db
read_verilog /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/synthesis/picorv32a.synthesis_cts.v
read_liberty -max ::env(LIB_SLOWEST)
read_liberty -min ::env(LIB_FASTEST)
read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
set_propagated_clock [all_clocks]
report_checks -path_delay min_max -format full_clock_expanded digits 4
```

Slack violation detected post-CTS.

Timing fixed and slack met successfully.

```
0.0000 12.0000  clock source latency
 0.0225  0.0100 12.0100 ^ clk (ln)
                           clk (net)
 1  0.0079   0.0225  0.0000 12.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd__clkbuf_16)
                           0.0283  0.1016 12.1116 ^ clkbuf_0_clk/X (sky130_fd_sc_hd__clkbuf_16)
                           clknet_0_clk (net)
 2  0.0044   0.0283  0.0000 12.1116 ^ clkbuf_1_1_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0388  0.0697 12.1814 ^ clkbuf_1_1_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_1_1_0_clk (net)
 1  0.0022   0.0388  0.0000 12.1814 ^ clkbuf_1_1_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0635  0.0910 12.2724 ^ clkbuf_1_1_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_1_1_1_clk (net)
 2  0.0044   0.0635  0.0000 12.2724 ^ clkbuf_2_3_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0390  0.0811 12.3535 ^ clkbuf_2_3_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_2_3_0_clk (net)
 1  0.0022   0.0390  0.0000 12.3535 ^ clkbuf_2_3_1_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0635  0.0911 12.4446 ^ clkbuf_2_3_1_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_2_3_1_clk (net)
 2  0.0044   0.0635  0.0000 12.4446 ^ clkbuf_3_7_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0635  0.0987 12.5433 ^ clkbuf_3_7_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_3_7_0_clk (net)
 2  0.0044   0.0635  0.0000 12.5433 ^ clkbuf_4_15_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0635  0.0988 12.6421 ^ clkbuf_4_15_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_4_15_0_clk (net)
 2  0.0044   0.0635  0.0000 12.6421 ^ clkbuf_5_30_0_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.3758  0.3142 12.9563 ^ clkbuf_5_30_0_clk/X (sky130_fd_sc_hd__clkbuf_1)
                           clknet_5_30_0_clk (net)
 4  0.0316   0.3758  0.0000 12.9563 ^ clkbuf_leaf_199_clk/A (sky130_fd_sc_hd__clkbuf_1)
                           0.0405  0.2075 13.1638 ^ clkbuf_leaf_199_clk/X (sky130_fd_sc_hd__clkbuf_1)
 6)   0.0094   0.0405          clknet_leaf_199_clk (net)
                           0.0000 13.1638 ^ _48896/_CLK (sky130_fd_sc_hd__dfxtp_1)
                           0.0000 13.1638          clock reconvergence pessimism
                           -0.1068 13.0570          library setup time
                           13.0570          data required time
-----+
                           13.0570          data required time
                           -7.7209          data arrival time
-----+
                           5.3361          slack (MET)
```

PDN generation process started.

```
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
%
%
%
% gen_pdn
```

```
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on
a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 27491.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def to /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/floorplan/30-pdn.def
```

```
Notice 0:      Created 13 technology layers
Notice 0:      Created 25 technology vias
Notice 0:      Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:      Created 499 pins.
Notice 0:      Created 23585 components and 175277 component-terminals.
Notice 0:      Created 25889 nets and 80895 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/27-11_09-02/results/cts/picorv
32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsuser/Desktop/work/tools/openLane_working_dir/pdks/sky130A/l
bs_tech/openlane/config_pdn.tcl
[INFO] [PDNG-0088] Design Name is picorv32a
[INFO] [PDNG-0089] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Type: stdcell, grid
  Stdcell Ralls
    Layer: met1 - width: 0.480  pitch: 2.720  offset: 0.000
    Straps
      Layer: met4 - width: 1.600  pitch: 153.600  offset: 16.320
      Layer: Met5 - width: 1.600  pitch: 153.180  offset: 16.650
      Connect: {met4 met5} {neti met4}
Type: macro, Macro_1
  Macro orientation: R0 R180 MX M90 R270 MXR90 MYR90
  Straps
  Connect: {met4_PIN_ver met5}
[INFO] [PDNG-0012] **** END INFO ****
```

PDN information showing power rails and pitch.

Routing stage initiated connecting all components.

```
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/28-11_11-41 in 0h18m22s
%
```