# Performance Comparision of 8- Bit Multiplier Architectures using Nexys 4 DDR


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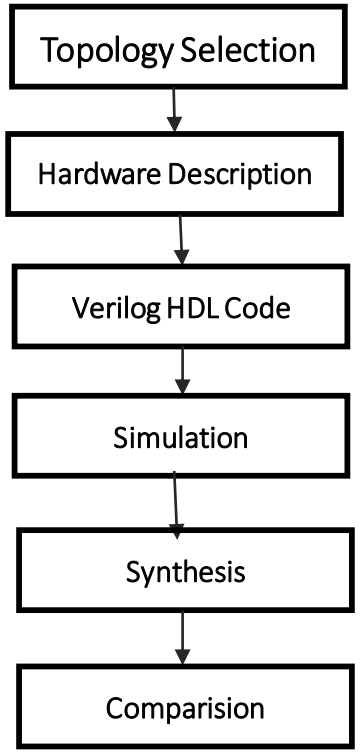
# TALK FLOW

- Objective
- Research Gap
- Literature Review
- Methodology
- Results
- References

# OBJECTIVE

- The main objective is to design multipliers to find the product of two 32-bit numbers and then synthesize them on a Nexys 4 DDR, FPGA board and to compare them in different aspects.

**Work Flow:**



# RESEARCH GAP

- **Vedic Multiplier** employs Vedic mathematics to efficiently perform multiplication operations. Its algorithm, often based on methods like the "Urdhva-Tiryak" (Vertically and Diagonally) method, breaks down the multiplication process into simpler steps. In this algorithm, the multiplicands are split into smaller parts, crosswise multiplications are performed, and the results are summed to obtain the final product.

- **Booth Multiplier** reduces the number of partial product additions required compared to conventional multiplication algorithms like Long Multiplication. Its algorithm employs a technique that exploits patterns in the multiplicand and multiplier to minimize the number of additions. It reduces the number of partial products and additions required, resulting in faster multiplication operations and reduced hardware complexity.

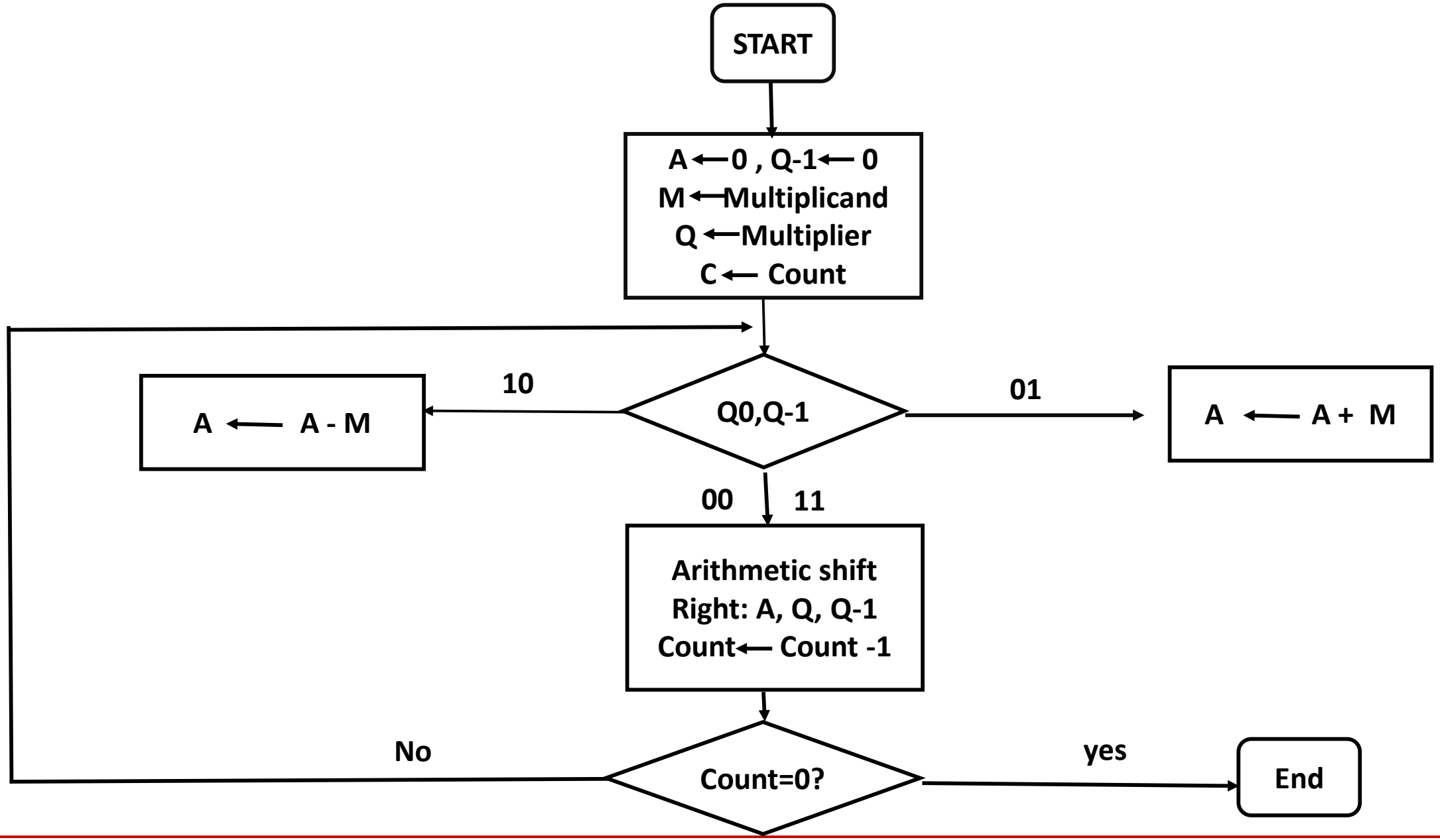
- **Wallace Tree Multiplier** prioritize speed by partial product reduction. They generate all possible partial products form the binary multiplication, but then efficiently reduce them in stages using a tree structure of full and half adders. It combines partial products with the same weight (bit position) while progressing upwards, minimizing the number of rows of products to be summed in the final stage.

- There isn't much research comparing how Wallace tree multipliers perform against other multipliers like Booth and Vedic. We will focus on comparing these three to see which one works best in different aspect.

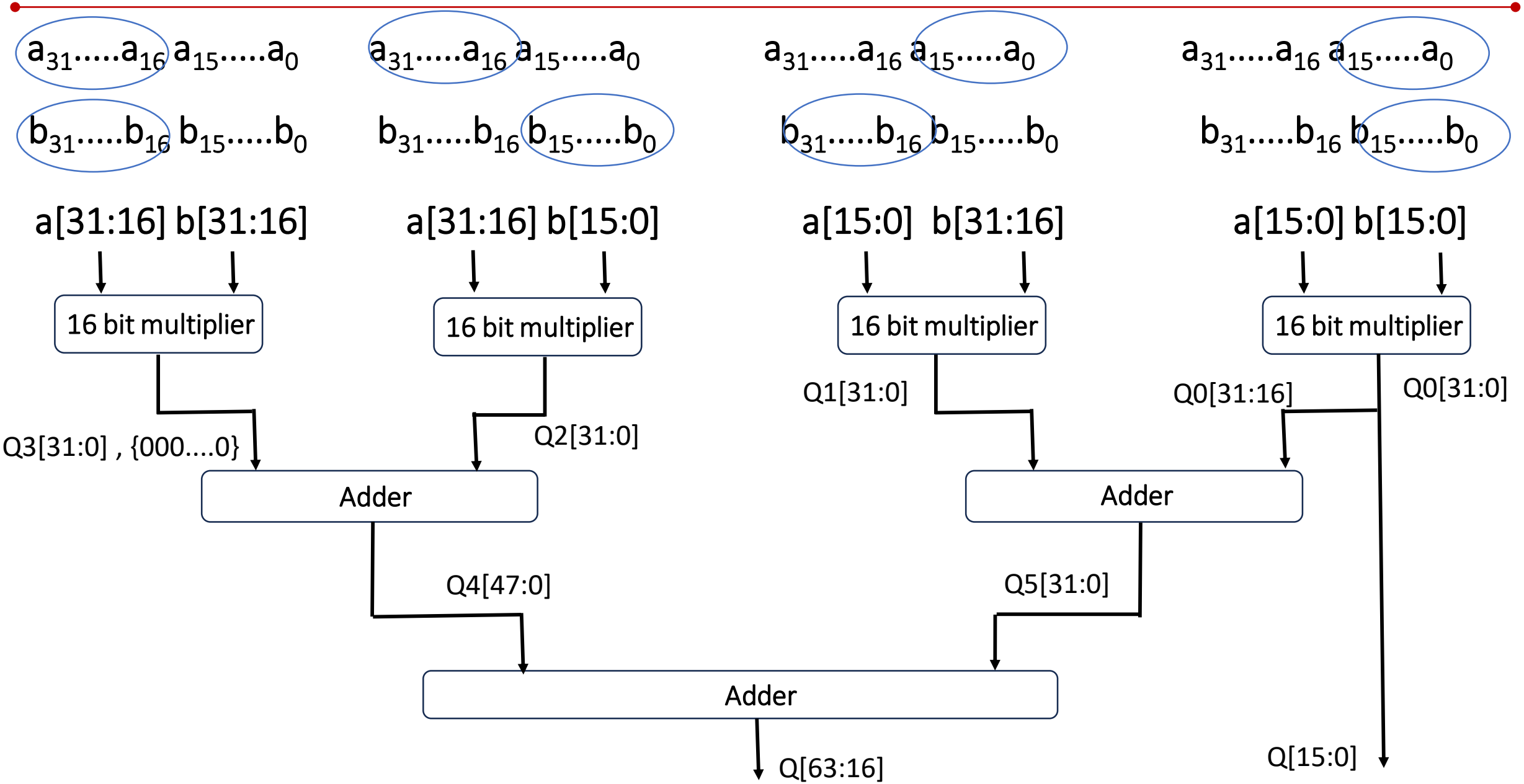
# LITERATURE REVIEW

| RESEARCH PAPER | MULTIPLIERS USED | Board | Result |
|---|---|---|---|
| **A REVIEW ON COMPARATIVE PERFORMANCE ANALYSIS OF DIFFERENT DIGITAL MULTIPLIERS BY Vikas Kaushik and Himanshi Saini[1]** | Array Multiplier (AM), Booth Multiplier (BM) & Vedic Multiplier (VM) | Spartan 2 with the device name as xc2s15-6cs144 | In terms of Delay, BM is low, VM is medium and AM is high. In terms of Chip Area, BM and VM is low, AM is high. In terms of Power, BM is low, VM is medium and AM is high. |
| **COMPARATIVE ANALYSIS AND FPGA IMPLEMENTATION OF VEDIC AND BOOTH MULTIPLIER BY PARUL AGRAWAL & RAHUL SINHA[2]** | Vedic Multiplier(VM) & Booth Multiplier(BM) | Spartan 6 with the device name as Xc6slx45, package csg324 | The delay in 4 bit VM was observed as 9.81 ns and for BM it was 10.8ns. As the bit number increases to 8/16 bits, the delay in VM becomes more pronounced compared to BM. |
| **PERFORMANCE COMPARISON REVIEW OF 32-BIT MULTIPLIER DESIGNS BY KELLY LIEW SUET & SWEE LO HAI HIUNG[3]** | Array Multiplier (AM), Dadda Multiplier (DM) & Radix-4 Boot Encoding multipliers (REM) | Kintex-7 with XC7K325T, Package FBG676. | In terms of Delay, DM is low, REM is medium and AM is high. In terms of Chip Area, REM is low, AM is moderate and DM is high. |

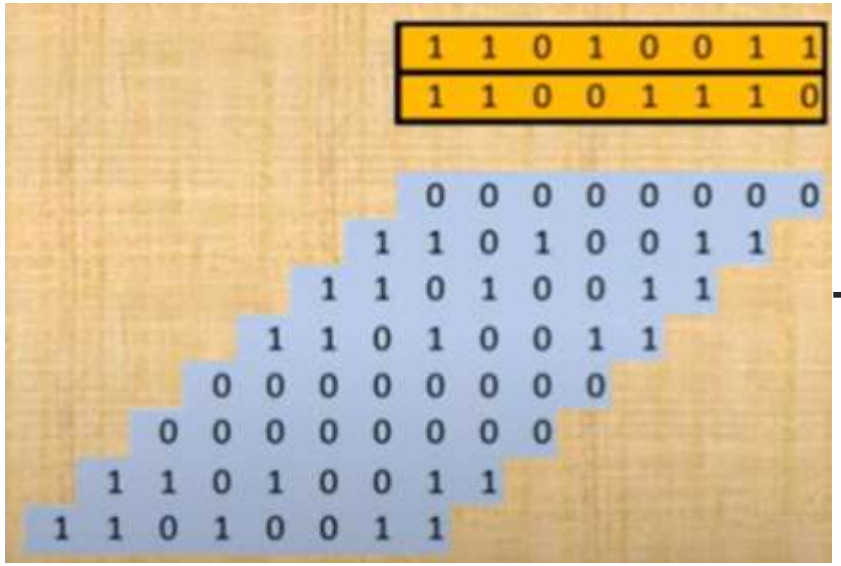
# BOOTH MULTIPLIER

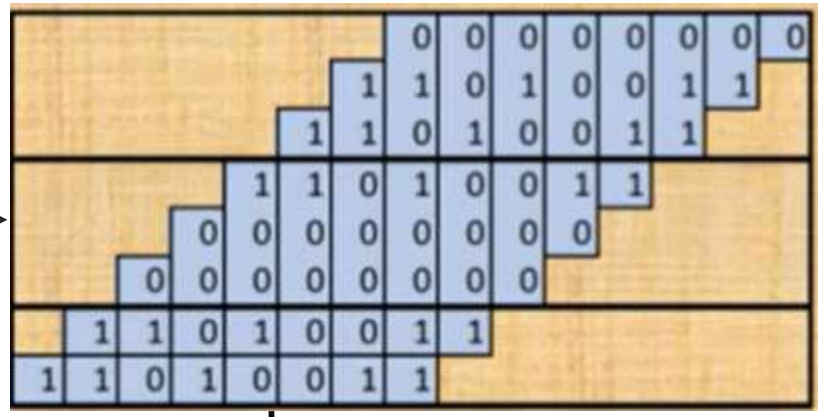


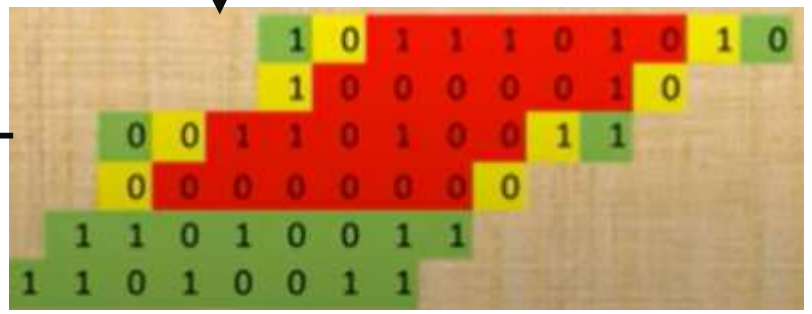
# VEDIC MULTIPLIER

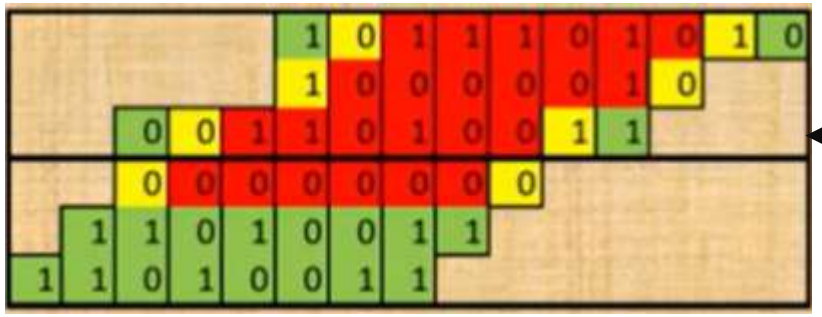


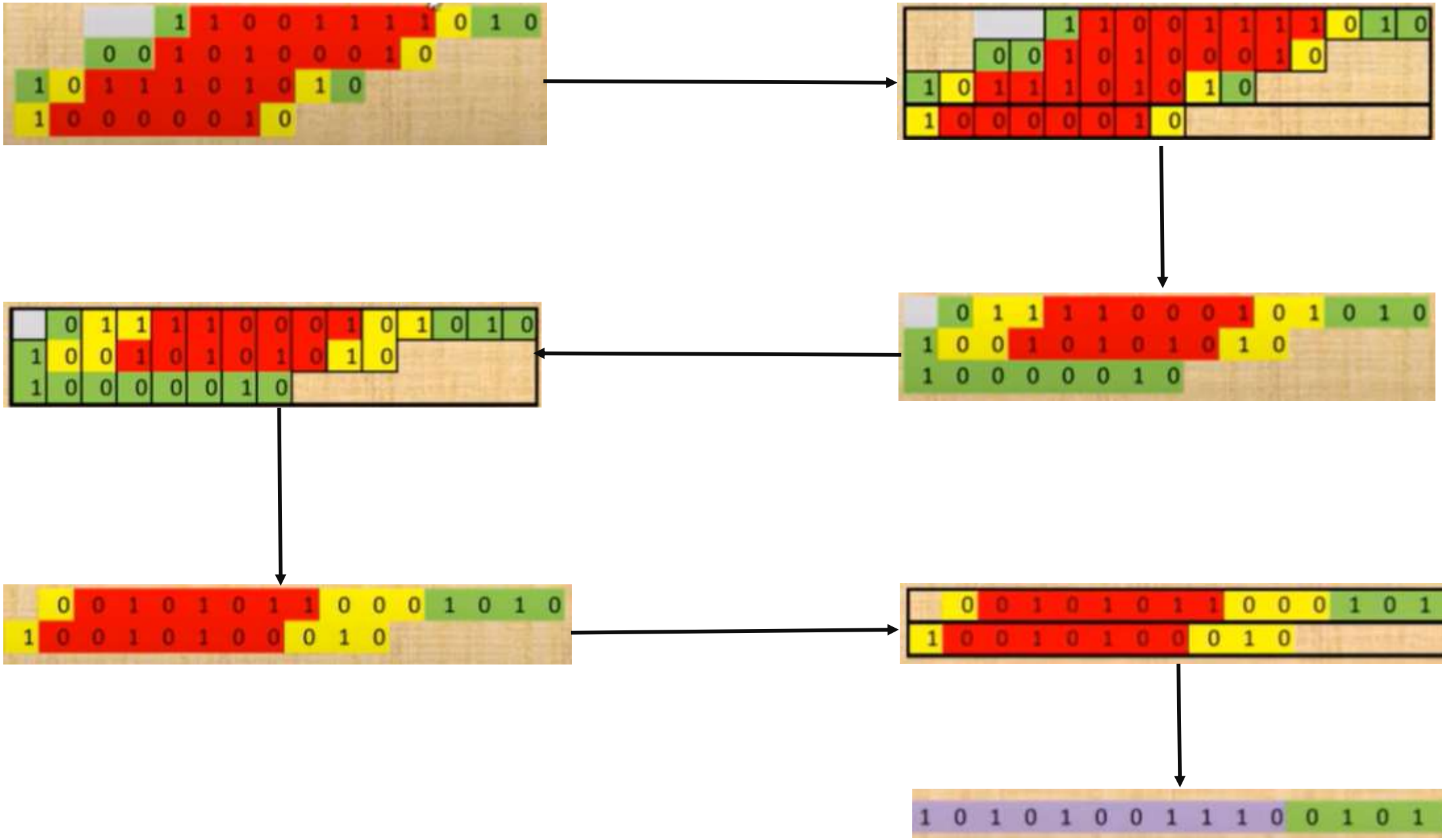
# WALLACE MULTIPLIER



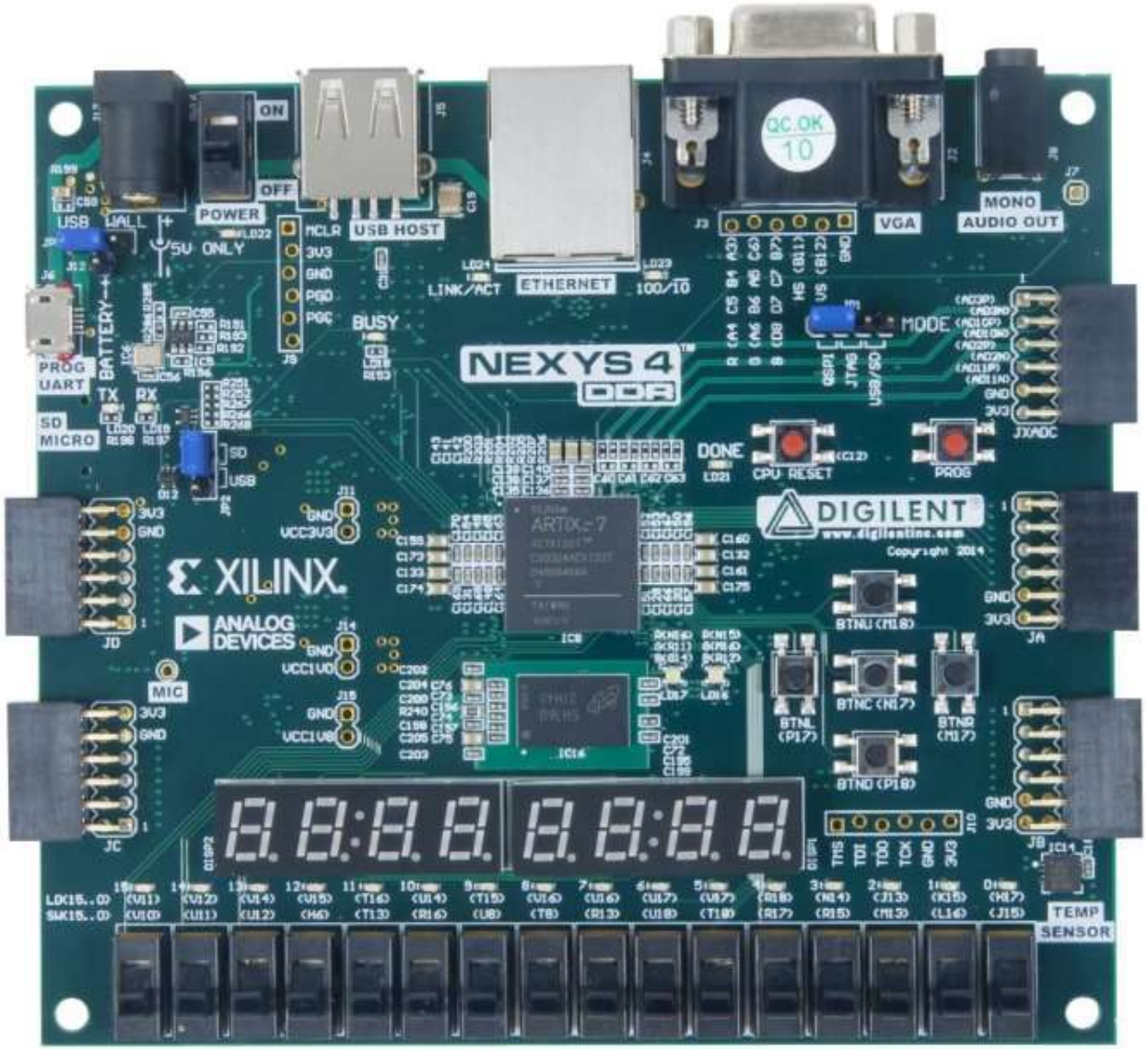



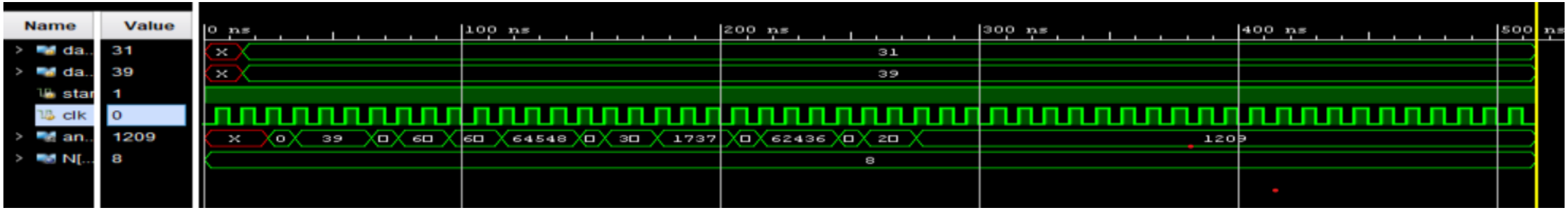


# NEXYS 4 DRR

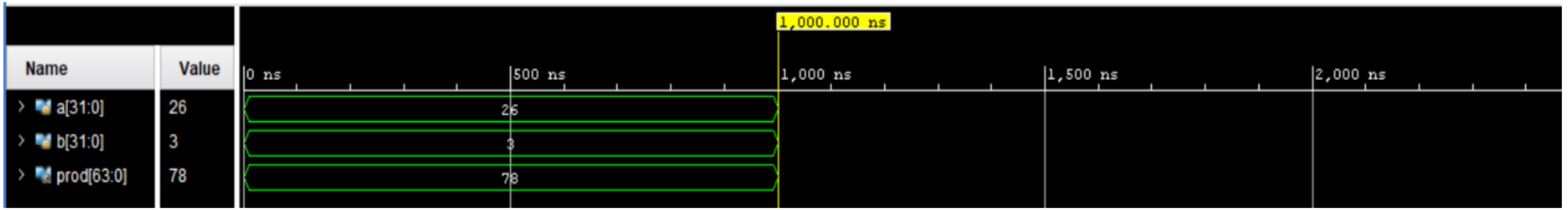

NEXYS 4
DDR
DIGILENT
XILINX
ANALOG DEVICES
POWER
ON
OFF
USB
WALL
5V ONLY
USB HOST
ETHERNET
LINK/ACT
100/10
VGA
MONO
AUDIO OUT
PROG
UART
TX
RX
SD
MICRO
BUSY
MODE
DONE
CPU RESET
PROG
MIC
BTNU (M18)
BTNC (N17)
BTNL (P17)
BTNR (M17)
BTND (P18)
TEMP
SENSOR
JXADC
JA
JB
JC
JD

# SIMULATION RESULTS

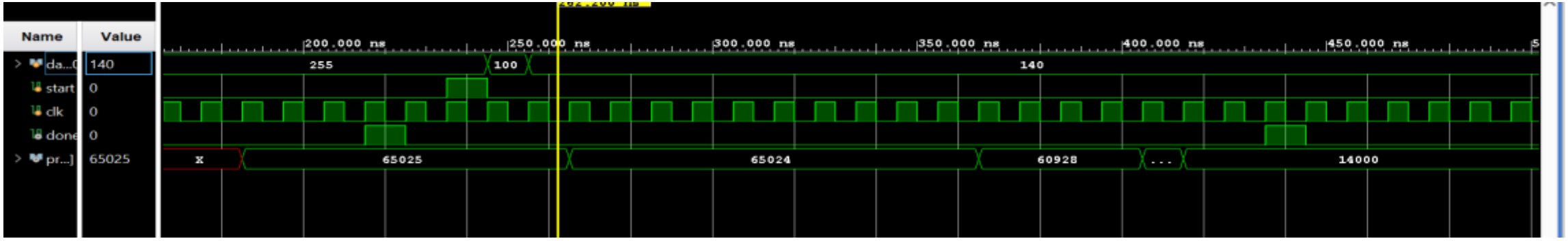
## Booth Multiplier:




## Wallace Tree Multiplier:

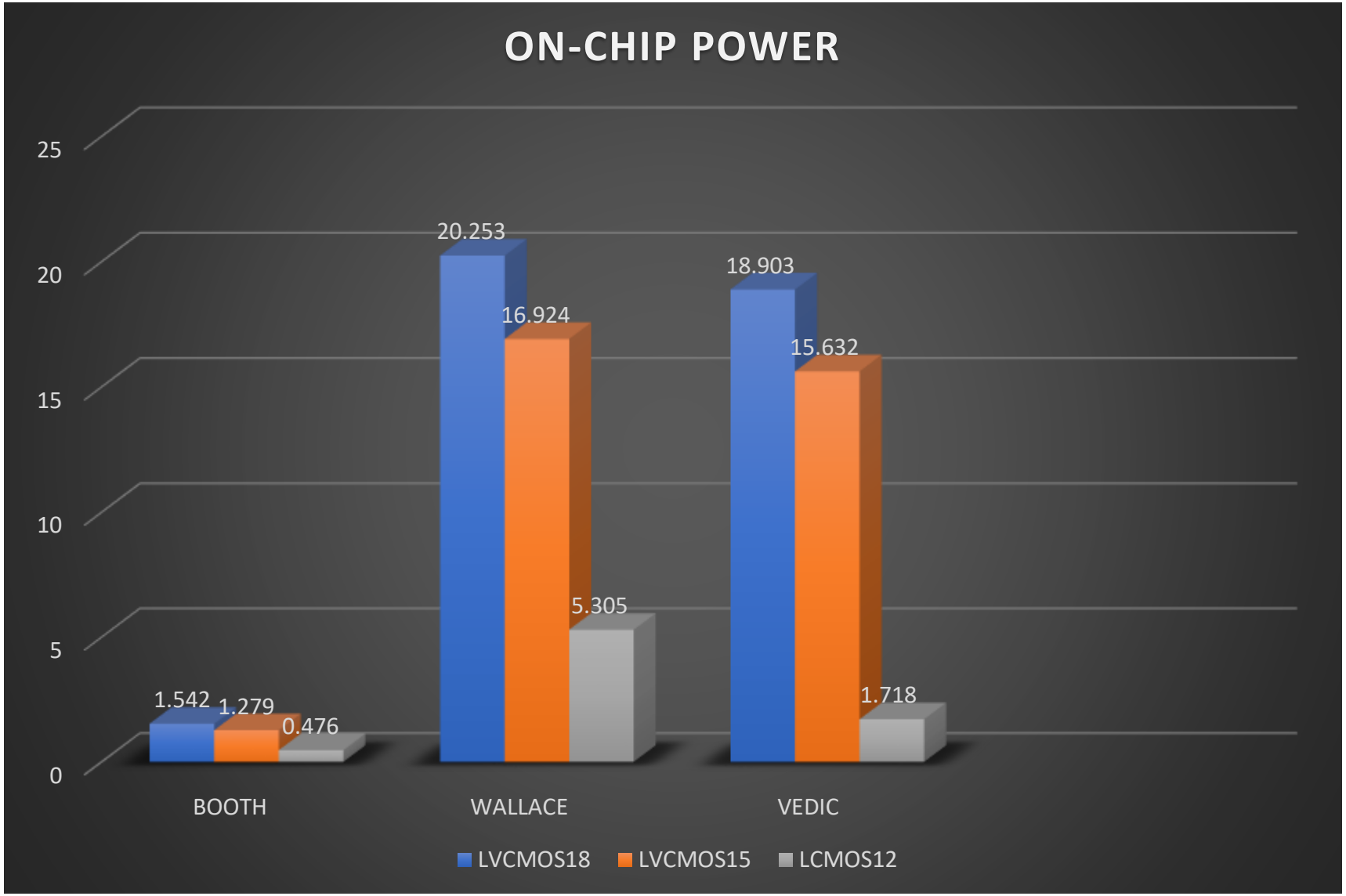



## Vedic Multiplier:



# ON-CHIP POWER COMPARISON

| | LVCMOS18 | LVCMOS15 | LVCMOS12 |
|---|---|---|---|
| **BOOTH MULTIPLIER** | 1.542W | 1.279W | 0.476W |
| **WALLACE TREE MULTIPLIER** | 20.2630W | 16.924W | 5.305W |
| **VEDIC MULTIPIER** | 18.903W | 15.632W | 1.718W |


ON-CHIP POWER
25
20
15
10
5
0
20.253
16.924
5.305
18.903
15.632
1.718
1.542
1.279
0.476
BOOTH
WALLACE
VEDIC
LVCMOS18
LVCMOS15
LCMOS12

# UTILIZATION REPORT OF BOOTH

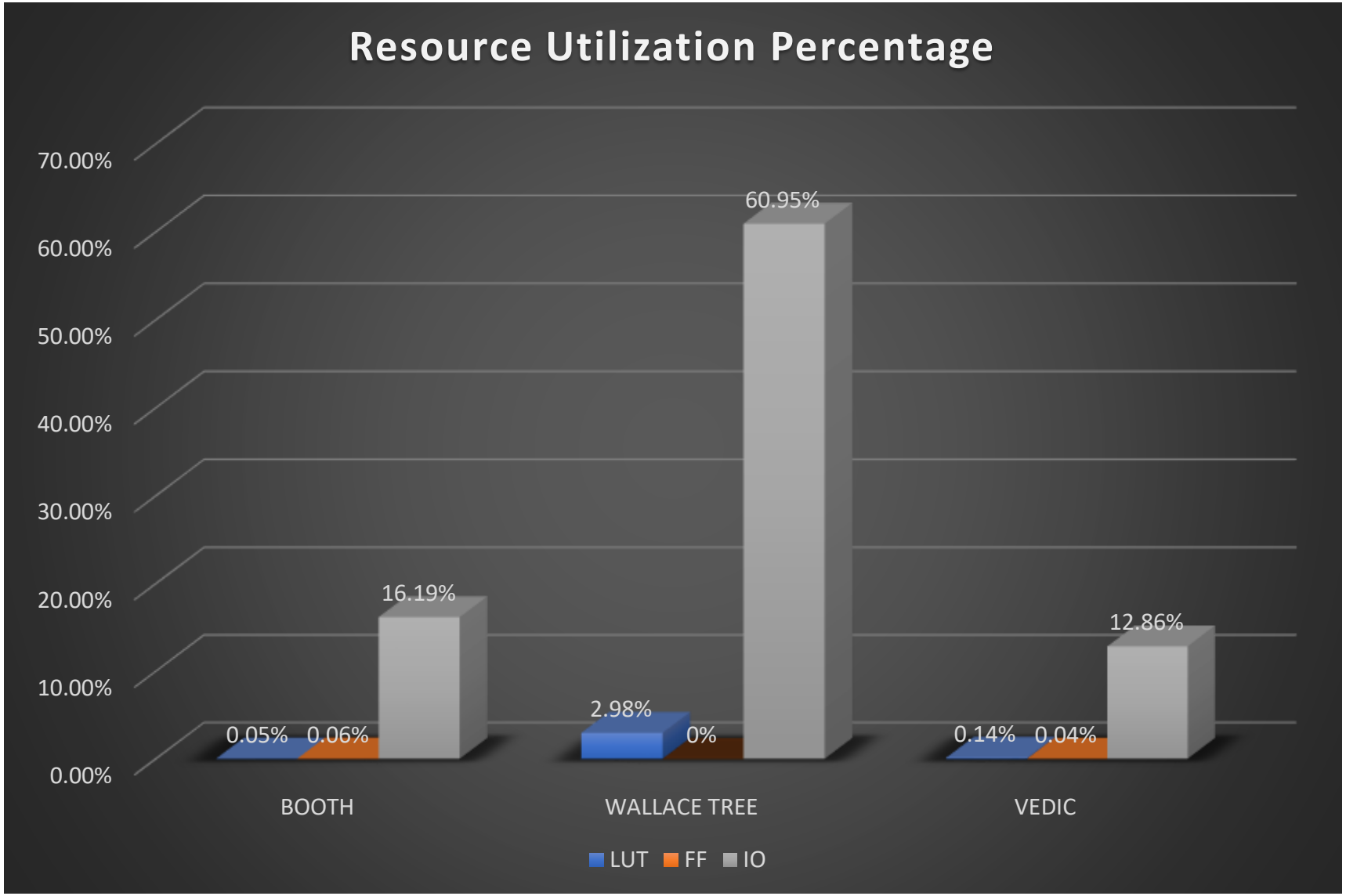
| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| **LUT** | 33 | 63400 | 0.05 |
| **FF** | 70 | 126800 | 0.06 |
| **IO** | 34 | 210 | 16.19 |

# UTILIZATION REPORT OF VEDIC

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| **LUT** | 91 | 63400 | 0.14 |
| **FF** | 53 | 126800 | 0.04 |
| **IO** | 27 | 210 | 12.86 |

# UTILIZATION REPORT OF WALLACE TREE

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| **LUT** | 1891 | 63400 | 2.98 |
| **FF** | 0 | 126800 | 0 |
| **IO** | 128 | 210 | 60.95 |


Resource Utilization Percentage
70.00%
60.00%
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
0.05%
0.06%
16.19%
2.98%
0%
60.95%
0.14%
0.04%
12.86%
BOOTH
WALLACE TREE
VEDIC
LUT
FF
IO

# REFERENCES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[2]. Agrawal, P. and Sinha, R., 2015. Comparative analysis and FPGA implementation of Vedic multiplier for various bit lengths using different adders. *International Journal of Innovative Research in Computer and Communication Engineering*, *3*(10), p.29.

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# Thank You