**UART – Hardware communication protocol design**

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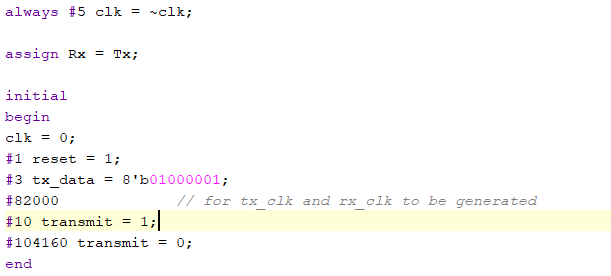
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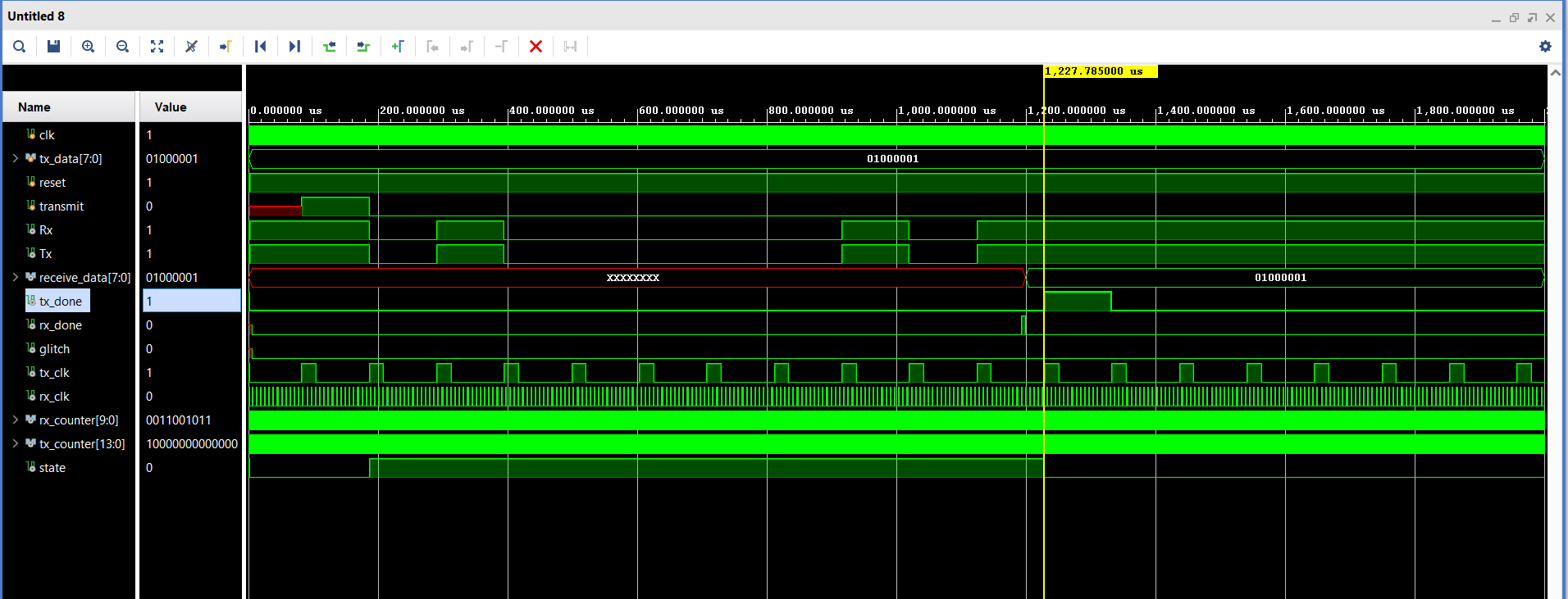
**SAMPLE OUTPUTS**

1. Sample testbench and the corresponding output for **uart module** :

Testbench :

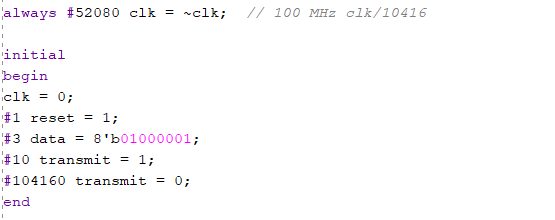


Output :

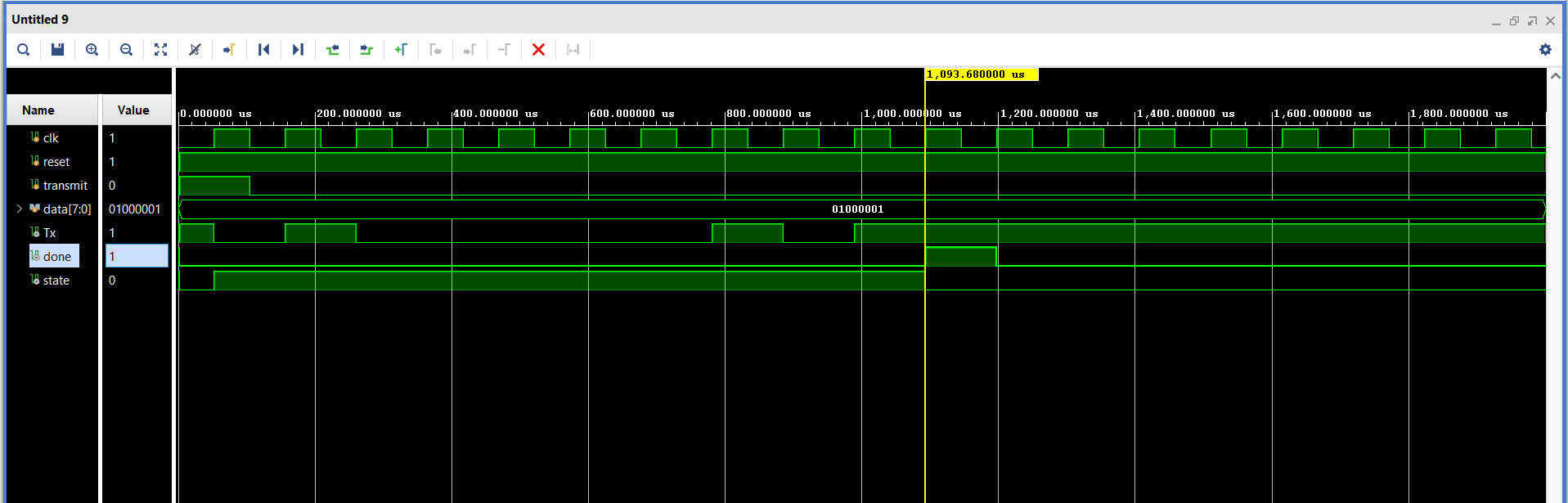


1. Sample Testbench and corresponding output for uart\_transmitter (**uart\_tx**) module :

Test Bench:

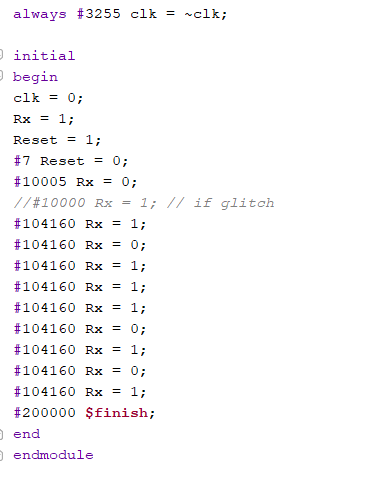


Output:

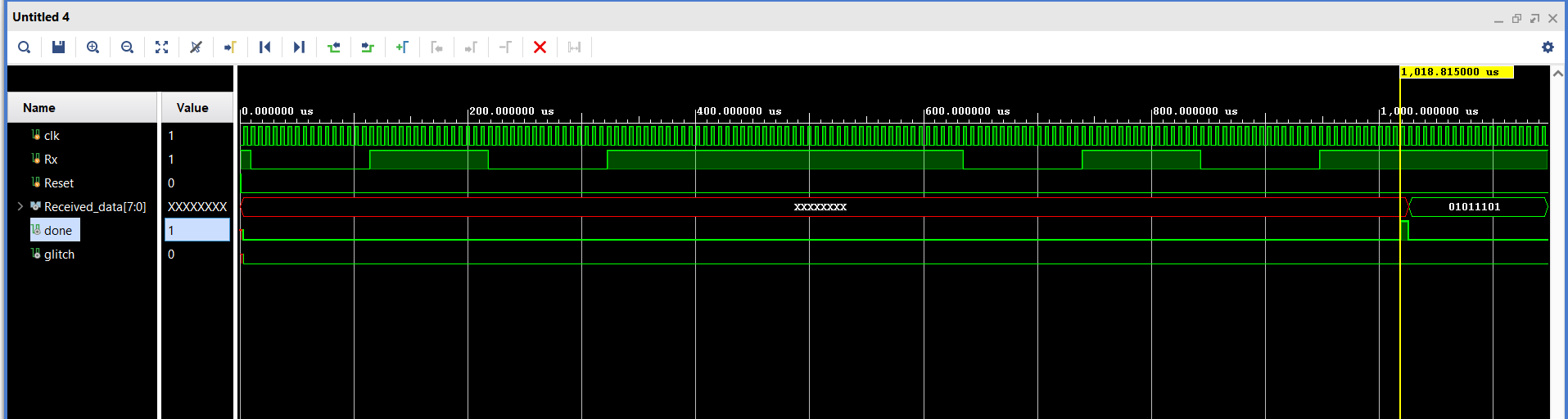


1. Sample Testbench and corresponding output for uart\_receiver (**uart\_rx**) module: (**without glitch**)

Testbench:

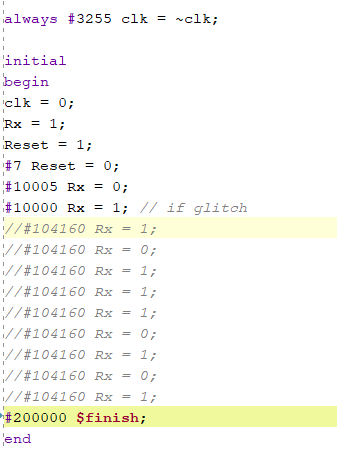


Output :



1. Sample Testbench and corresponding output for the **uart\_rx** module **with a glitch** :

Test bench:



Output :

