Product Description

The **PE26100** is an ultra-high efficiency 4-Level step-down and step-up converter for single cell Li-ion and Li-polymer batteries charging application. It can deliver up to 5A charging current in regulation mode and in divide-by-3 charge pump mode. It can configure into dual ICs operation for 9A charging current in regulation mode and in divide-by-3 or divide-by-2 charge pump mode.

A wide input range of 4.5 V to 18 V input to support both USB and wireless inputs.

In reverse step-up mode, the output is programmable from 4.8 V to 16 V in 100 mV step with programmable output current limit up to 1.7 A.

The PE26100 comes in a 4.695mm x 2.925mm 77pin WLCSP package. The overall solution for a single IC solution is 70mm^2 (140mm^2 for dual IC solution) with 1mm z-height.

Features

- Proprietary architecture enables industry leading efficiency at 9A charging current in a low-profile solution.
- Wide input voltage range, from 4.5 V to 18 V, supports fast charging of single Li-Ion cells from USB and wireless input.
- Low EMI fixed-frequency operation under heavy load conditions.
- Input and output current and voltage, IC temperature monitoring and telemetry via I^{2}C.
- Full protection including input and output UVLO, input and output OVP, input and output OCP and IC over-temperature with fault and warning status.
- Supports Divide-by-3, Step-down and Step-up regulating modes.
- Dual external disconnect switch control.
- Paralleled operation.

Typical Applications

- Smart Phone
- Tablet
- Portable electronics

Efficiency

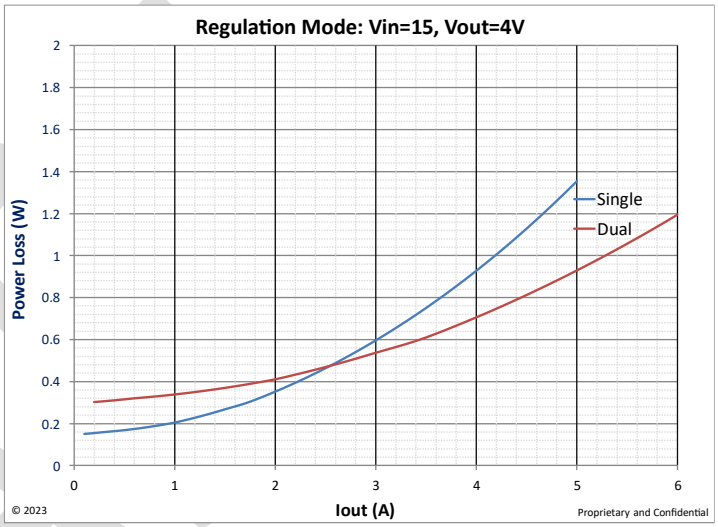

Figure 1. Power Loss vs Charging Current

Simplified Application

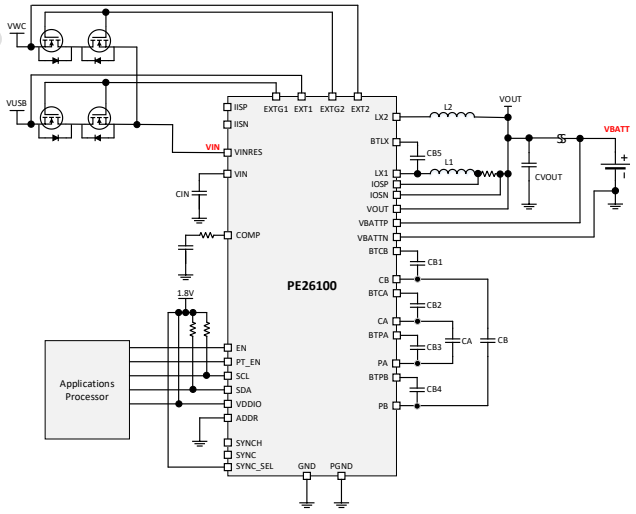

Figure 2. Application Schematic (Single IC Solution with Internal Current Sense)

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ESD Precautions and Absolute Maximums

Exceeding absolute maximum ratings listed in Table 2 may cause permanent damage. Operation should be restricted to the limits in Table 2. Operation between operating range maximum and absolute maximum may reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 1.

PARAMETER	CONDITION	MAX	UNITS
Human-Body Model, all pins	Joint JEDEC/ESDA Human Body Model (JS-001-2017)	1500	V
Charged Device Model, all pins	Joint JEDEC/ESDA Charged Device Model (JS-002-2018)	500	V

Table 1. ESD Tolerance

Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Input Voltage VIN, VINRES, IISP, IISN to PGND	-0.3	21	V
EXT1, EXT2, EXTG1, EXTG2 to PGND	-0.3	28	V
Battery Voltage VOUT to PGND	-0.3	5.5	V
VBATTP, VBATTN, IOSP, IOSN to GND	-0.3	5.5	V
BTLX to LX1, BTCA to CA, BTCB to CB, BTPA to PA, BTPB to PB	-0.3	5.5	V
CA, CB, PA, PB to PGND	-0.3	TBD	V
LX1, LX2 to PGND	-0.3	TBD	V
EN, PT_EN, SDA, SCL, ADDR, VDDIO, SYNC_SEL, SYNC, SYNCH, COMP to GND	-0.3	VBATT+0.3	V
Storage Temperature	-65.0	150.0	°C
Junction Temperature	-40.0	150.0	°C
Operating Bump or Lead Temperature		260.0	°C

Table 2. Absolute Maximum Ratings

Recommended Operating Conditions

Table 3 lists the recommended operating conditions for the PE26100. Devices should not be operated outside the operating conditions listed below.

PARAMETER	MIN	MAX	UNITS
EXT1, EXT2 Voltage Range, Relative to GND	4.5	18	V
VOUT Voltage Range, Relative to GND	3.2	4.55	V
VIN Voltage in Step-down Mode	VOUT + 0.2	18[1]	V
VIN Voltage in Reverse Step-up Mode	4.8	16	V
Junction Temperature Range, TJ	-40.0	125.0	°C
Ambient Temperature Range, TA	-40.0	85.0	°C
Note 1: VIN operation at 18V reduces the IC lifetime. For 10-year IC operating lifetime, limit max VIN operation to 16V or below.			

Table 3. Recommended Operating Conditions

Package Thermal Characteristics[1]

Table 4 lists the thermal characteristics of the chip.

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Junction Temperature	Measured at max ambient temperature (TA) and max power dissipation.		150.0	°C
Junction-to-Case Top Thermal Resistance (ΘJT)	JEDEC JESD51-12-01 and JESD15-3	TBD		°C/W
Junction-to-Board Thermal Resistance (ΘJC)	JEDEC JESD51-12-01 and JESD15-3	TBD		°C/W
Junction-to-Air Thermal Resistance (ΘJA)	JEDEC JESD51-12-01 and JESD15-3	TBD		°C/W
Note 1: Package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-12. See also pSemi Application Note 57, *Thermal Characterization*.				

Table 4. Package Thermal Characteristics

Electrical Characteristics

Table 5 provides the PE26100 key electrical specifications at the following specifications, unless otherwise noted.

VIN = 4.5V to 18V, TA=TJ = -40ºC to +85ºC, VOUT = 3.2V to 4.2V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input and Battery Voltage Range						
VIN Voltage Range	VIN	CP_2x/3x = 0 Divide-by-3 Charge Pump Mode		VOUT*3		V
		CP_2x/3x = 1 Divide-by-2 Charge Pump Mode (to be hidden from customer datasheet version until function is validated)		VOUT*2		V
	VIN	MLC_3L/4L = 0 4L Step-down Regulation Mode	VOUT +0.2		18	V
	VIN	MLC_3L/4L = 1 3L Step-down Regulation Mode (to be hidden from customer datasheet version until function is validated)	VOUT +0.2		11	V
	VIN	Reverse Step-up Mode	4.8		16	V
VOUT Voltage Range	VOUT	Fast Charge/Constant Current Mode	3.2		4.55	V
VOUT Input Under-voltage Lockout (UVLO) Threshold High	$V_{OUT-UVLO\_H}$	Input Rising			3.19	V
VOUT Input Under-voltage Lockout (UVLO) Threshold Low	$V_{OUT-UVLO\_L}$	Input Falling	3			V
Under-voltage Lockout (UVLO) Hysteresis	V_{UVLO_HYST}			100		mV
VIN Under-Voltage Protection	V_{IN-UV}			VOUT-1.2		V
Input Over-Voltage Protection (OVP)	V_{IN-OVP}	MLC_3L/4L bit = 0 Step-Down Regulation in 4L Mode	19.5			V
		MLC_3L/4L bit = 1 Step-Down Regulation in 3L Mode	12.5			V
Supply Current						
VOUT Shutdown Supply Current	I_{SHDN_VOUT}	EN = GND		10	20	µA
VOUT Standby Supply Current	I_{STBY_VOUT}	EN = Logic High, IC_EN bit = 1 EXTG_EN bit and PT_EN bit = 0		3		mA
Output Current						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum VOUT Charging Current	I_{LOAD_VOUT}				5	A
Minimum VOUT Current in reverse step-up mode			-3.5			A
Maximum Output Current in Reverse Step-up Operation	I_{LOAD_VIN}	OTG = 5V @ 1.5Amax (same spec in A series) WLC = 9V/10V @ 1.7Amax (maybe lower in A series)	1.7			A
Reverse Step-up Soft Start Timeout				10		ms
Gate Drive Specification EXTG1, EXTG2						
Gate ON Voltage		EXTGx=ON, V_EXTG = 5V (0) or 9V (1)		VIN + V_EXTG		V
Gate Pull up Current				50		µA
Gate Pull down Resistance		EXTGx=OFF		50		Ω
		EN=0		1		MΩ
Telemetry						
VIN ADC Resolution				20		mV
VBATT ADC Resolution				5		mV
VIN ADC Full Scale Accuracy			-2		+2	%
VBATT ADC Full Scale Accuracy		TA=25°C	TBD		TBD	%
		TA=0 to 70°C	TBD		TBD	%
		TA=-40C to 85°C	-2		+2	%
IIN ADC Resolution With Internal Current Sense Resistor				40 (TBD)		mA
IIN ADC Resolution With External Current Sense Resistor		Voltage across input current sense resistor With 10mΩ current sense resistor, the resolution in current is 20mA.		200		µV
IOUT ADC resolution		Voltage across input current sense resistor With 4mΩ current sense resistor, the resolution in current is 25mA.		100		µV
IIN ADC Full Scale Accuracy With Internal Current Sense Resistor		TA=25°C	TBD		TBD	%
		TA=0 to 70°C	-2		2	%
		TA=-40C to 85°C	-4		+4	%
IIN ADC Full Scale Accuracy With External Current Sense Resistor			-2		+2	%
IOUT ADC Accuracy		IOUT = 3A, 4mΩ	-5		+5	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Junction Temperature Resolution				5		°C
Temperature Accuracy		TA=25°C	-5		+5	°C
ADC Sample Time		For all ADC inputs		TBD		ms
VBATTP Leakage Current		Pin Voltage = 4.35V, EN=Logic, IC_EN bit=1		1	2	µA
VBATTN Leakage Current		Pin Voltage = ±0.25V, EN=Logic, IC_EN bit=1	-2		2	µA
Thermal Parameters						
Thermal Shutdown Threshold	TSD			160		°C
Thermal Shutdown Hysteresis	TSD_hyst			25		°C
Logic Levels EN, PT_EN, ADDR						
Input High Voltage	V_{IH_IO}		1.35			V
Input Low Voltage	V_{IL_IO}				0.45	V
Input Current		Pin Voltage = 1.8 V			1	µA
I²C SERIAL INTERFACE (VDDIO, SCL, SDA) SDA & SCL pulled up externally to 1.8V with 1.2kΩ resistors						
VDDIO Input Voltage Range			1.62	1.8	1.98	V
VDDIO Under-voltage Lockout (UVLO) Threshold High	$V_{DDIO-UVLO\_H}$	VDDIO Rising			1.61	V
VDDIO Under-voltage Lockout (UVLO) Threshold Low	$V_{DDIO-UVLO\_L}$	VDDIO Falling	TBD			V
VDDIO Supply Current					TBD	µA
SDA, SCL Input High Voltage	V_{IH}		1.35			V
SDA, SCL Input Low Voltage	V_{IL}				0.4	V
SDA, SCL Input Hysteresis	V_{HYS}			0.09		V
SDA, SCL Input Current	I_{SCL}, I_{SDA}				1	µA
SDA Output Low Level	V_{OL}	I_{SDA} = 2 mA			0.4	V
I²C Interface Initial Wait Time		Initial wait time from EN logic high to 1st I²C command accepted	1			ms
SDA, SCL Pin Capacitance	$C_{I/O}$				10	pF
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD AND FAST MODE						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	F_{SCL}	Standard mode			100	kHz
		Fast mode			400	kHz
		Fast mode plus			1	MHz
Clock Low Period	t_{LOW}	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
Clock High Period	t_{HIGH}	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
BUS Free Time between a STOP and a START condition	t_{BUF}	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Standard mode	4.7			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Hold Time for a Repeated START condition	$t_{HD:STA}$	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Setup Time of STOP condition	$t_{SU:STO}$	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Data Setup Time	$t_{SU:DAT}$	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
Data Hold Time	t_{HD_DAT}	Standard mode	0			µs
		Fast mode	0			µs
		Fast mode plus	0			ns
Rise Time of SCL Signal	t_{RCL}	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode			300	ns
		Fast mode	4		300	ns
		Fast mode plus			120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of SDA Signal	t_{FDA}	Standard mode			300	ns
		Fast mode	4		300	ns
		Fast mode plus	20		120	ns
Data Valid Time	t_{VD}	Standard mode			3.45	µs
		Fast mode			900	ns
		Fast mode plus			450	ns
Data Valid Acknowledge Time	t_{VDA}	Standard mode			3.45	µs
		Fast mode			900	ns
		Fast mode plus			450	ns
Capacitive Load for SDA and SCL	C_{BUS}	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF
Notes: 1.						

Table 5. Electrical Characteristics

PE26100 Pin Information

This section provides pin configuration information for the PE26100. Figure 3 shows the pin map of this device. Table 6 provides a description for each pin.

Pin Configuration

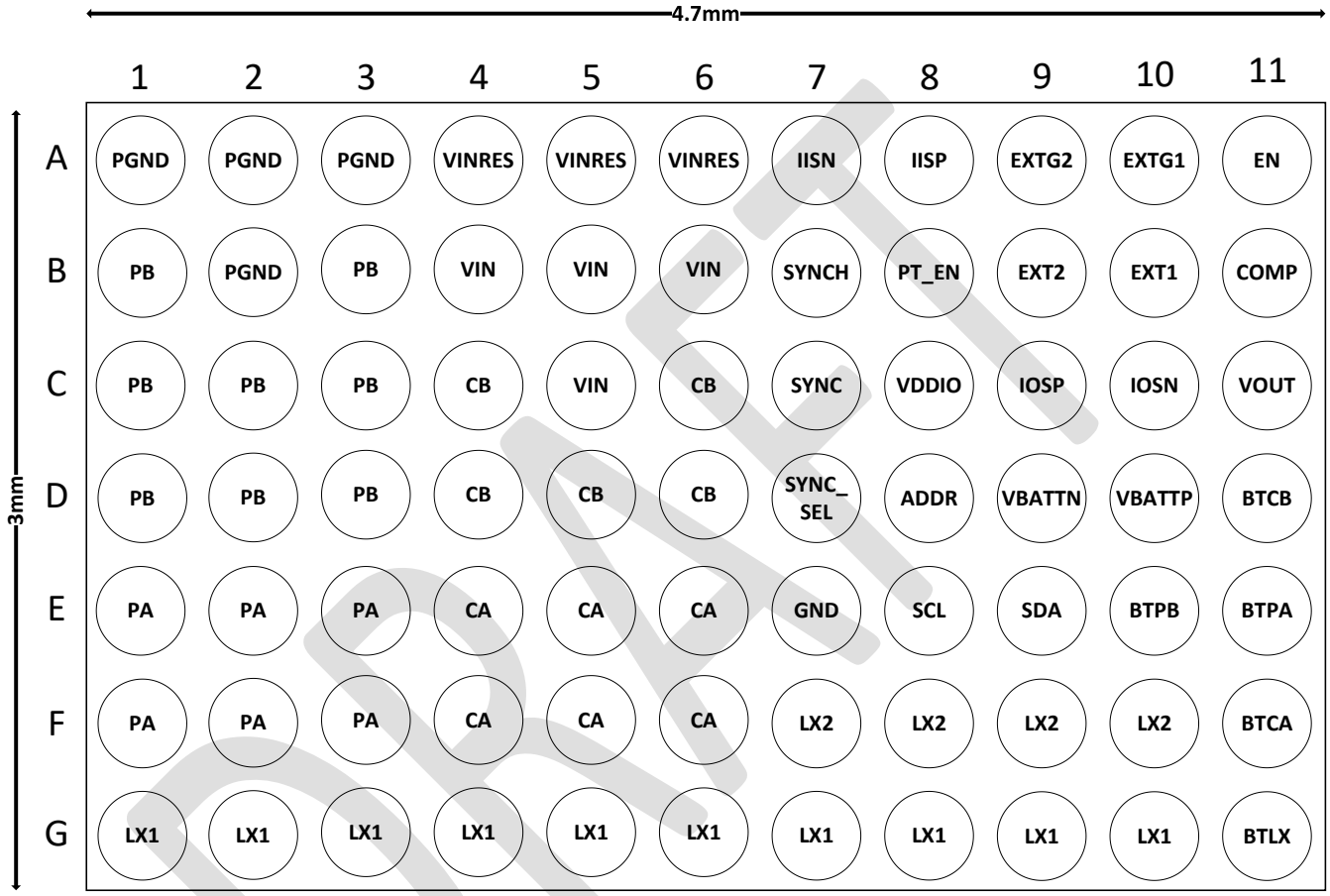


Figure 3. PE26100Top View (Bumps Down)
For reference only, Subject to Change

Pin Descriptions (For reference only, subject to change)

PIN NUMBER	NAME	DESCRIPTION
A1, A2, A3, B2	PGND	Power ground must tie externally to system ground plane. High current path.
A4, A5, A6	VINRES	Internal input current sense resistor pin, connect to USB or Wireless output through external B-B FET. If internal input current sense resistor is not used, then leave VINRES pin floating.
A7	IISN	Input current sense negative pin. Connect to negative side of external input current sense resistor and VIN pin. Leave pin floating when not using external input current sense resistor.
A8	IISP	Input current sense positive pin. Connect to positive side of external input current sense resistor. Leave pin floating when not using external input current sense resistor.
A9	EXTG2	External Gate Drive 2. Connect to external B-B FET gate pin.
A10	EXTG1	External Gate Drive 1. Connect to external B-B FET gate pin.
A11	EN (RESETb)	IC enable input pin. Logic high to enable IC. A logic low on this pin disables IC and resets the registers.
B1, B3, C1, C2, C3, D1, D2, D3	PB	Flying capacitor CB phase node. Connect CB fly capacitor between CB and PB pins.
B4, B5, B6, C5	VIN	IC input voltage pin. Connect input decoupling capacitors to this pin. Do not connect directly to USB or Wireless output through external B-B FET when internal input current sense resistor is used. If internal input current sense resistor is not used, then short VIN pin to VINRES pin.
B7	SYNCH	IC synchronization pin to synchronize master and slave PE26100. Connect to the SYNCH pin of the other PE26100.
B8	PT_EN	Power train enable input pin. Logic high to enable power train. A logic low on this pin disables power train. This pin has an 'AND' function with PT_EN bit.
B9	EXT2	External FET Input 2. Connect to external B-B FET input pin.
B10	EXT1	External FET Input 1. Connect to external B-B FET input pin.
B11	COMP	Compensation Pin.
C4, C6, D4, D5, D6	CB	Flying capacitor CB terminal. Connect CB fly capacitor between CB and PB pins.
C7	SYNC	IC synchronization pin to synchronize master and slave PE26100. Connect to the SYNC pin of the other PE26100.
C8	VDDIO	Digital logic reference pin. Connect this to 1.8V or I^2C pull up voltage.
C9	IOSP	Output current sense positive pin. Connect to positive side of external output current sense resistor in series with L1 inductor used in step down regulation mode.
C10	IOSN	Output current sense negative pin. Connect to negative side of external output current sense resistor in series with L1 inductor used in step down regulation mode..
C11	VOUT	Output voltage pin. Connect to positive terminal of battery pack. This pin biases the part and is required for the IC to function.

D7	SYNC_SEL	IC synchronization pin to set PE26100 to master or slave setting. Connect to logic high for master, connect to logic low for slave.
D8	ADDR	Set lower three bits of the I^2C slave address. Logic low= '010', Logic high= '101', pin floating = '111'
D9	VBATTN	Battery voltage negative remote sense point. Connect to negative terminal of battery pack. Tie to VBATTP pin and connect to VOUT or GND when remote sense is not used.
D10	VBATTP	Battery voltage positive remote sense point. Connect to positive terminal of battery pack. Tie to VBATTN pin and connect to VOUT or GND when remote sense is not used.
D11	BTCB	Bootstrap capacitor pin. Connect a 22nF capacitor between BTCB and CB pins.
E1, E2, E3, F1, F2, F3,	PA	Flying capacitor CA phase node. Connect CA fly capacitor between CA and PA pins.
E4, E5, E6, F4, F5, F6	CA	Flying capacitor CA terminal. Connect CA fly capacitor between CA and PA pins.
E7	GND	Analog Ground.
E8	SCL	Serial clock for I^2C bus.
E9	SDA	Serial data for I^2C bus.
E10	BTPB	Bootstrap capacitor pin. Connect a 22nF capacitor between BTPB and PB pins.
E11	BTPA	Bootstrap capacitor pin. Connect a 22nF capacitor between BTPA and PA pins.
F7, F8, F9, F10	LX2	Switching Node for CP mode. Connect to an external inductor.
F11	BTCA	Bootstrap capacitor pin. Connect a 22nF capacitor between BTCA and CA pins.
G1, G2, G3, G4, G5, G6, G7, G8, G9, G10	LX1	Switching Node. Connect to an external inductor.
G11	BTLX	Bootstrap capacitor pin. Connect a 22nF capacitor between BTLX and LX1 pins.

Table 6. Pin Descriptions

Application Circuit

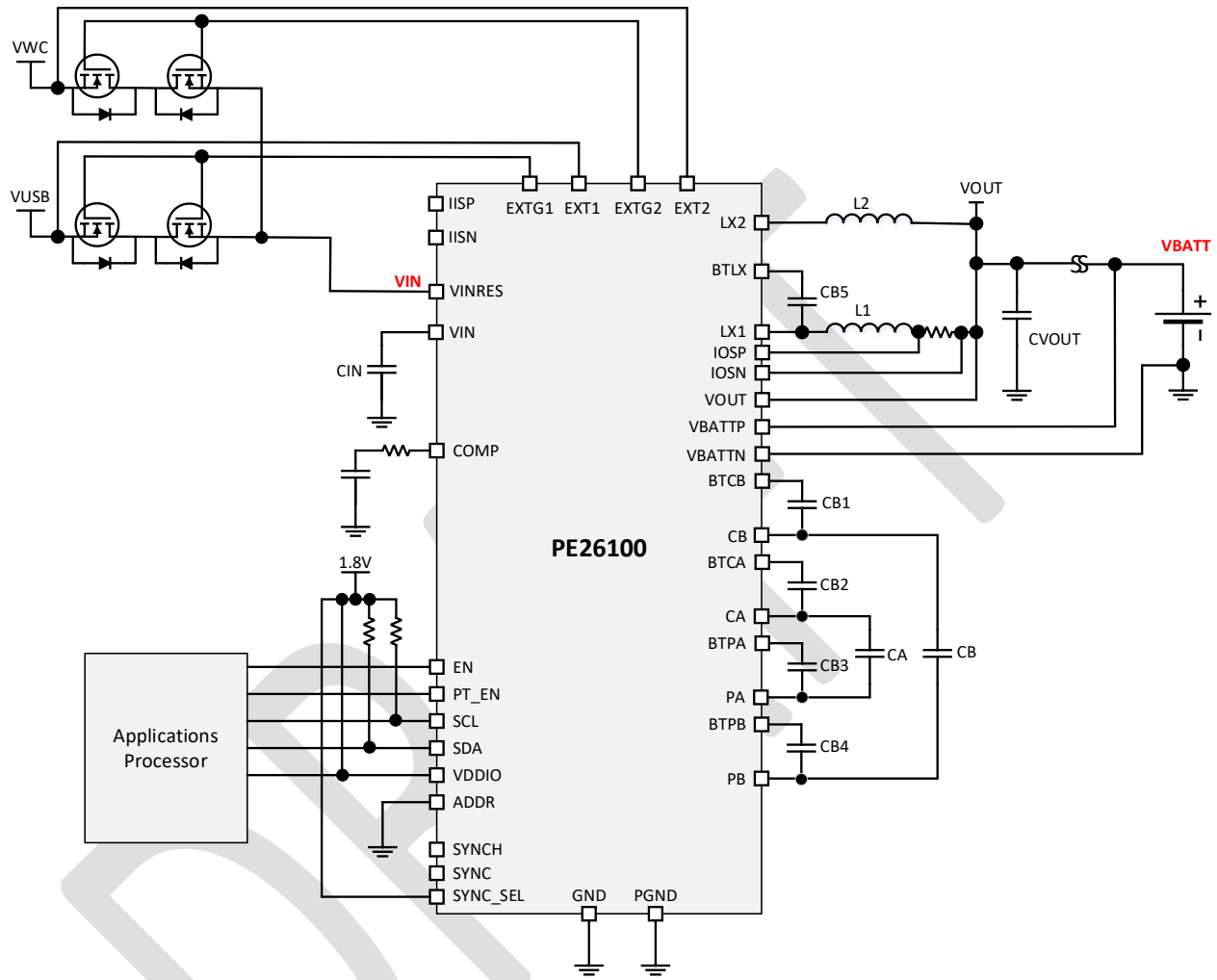


Figure 4. Application Circuit (Single IC solution with internal input current sense)

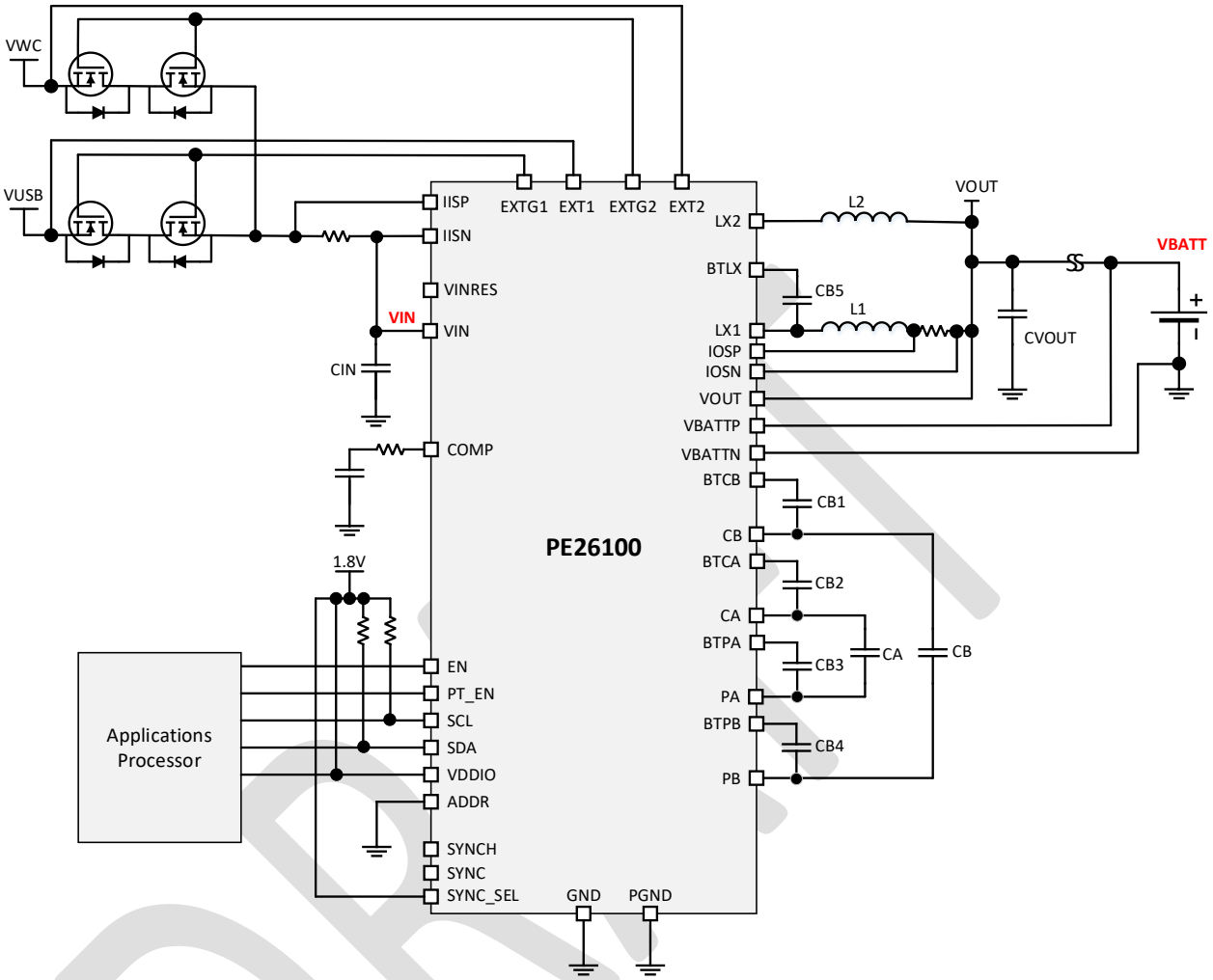


Figure 5. Application Circuit (Single IC solution with external input current sense resistor)

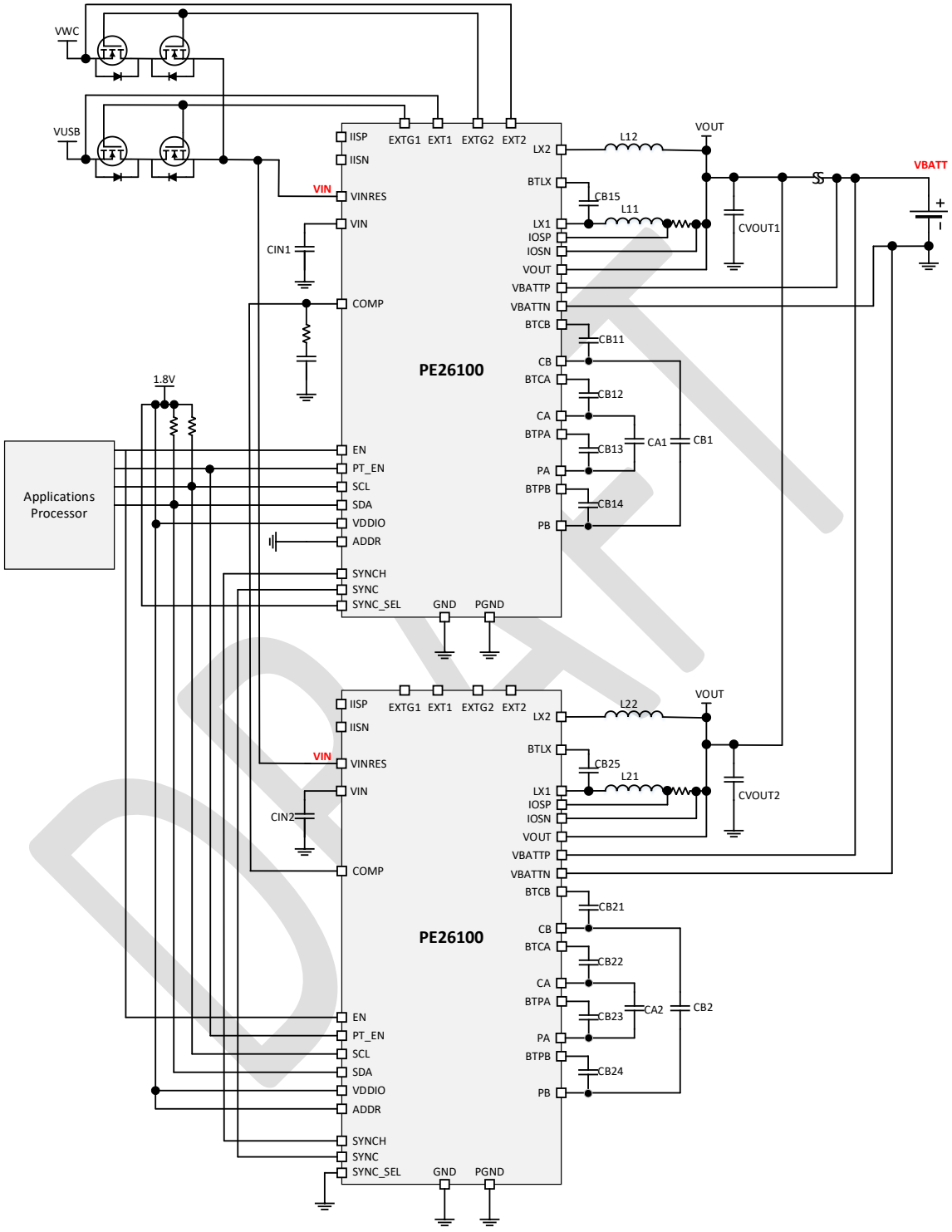


Figure 6. Application Circuit (Dual IC solution with internal input current sense)

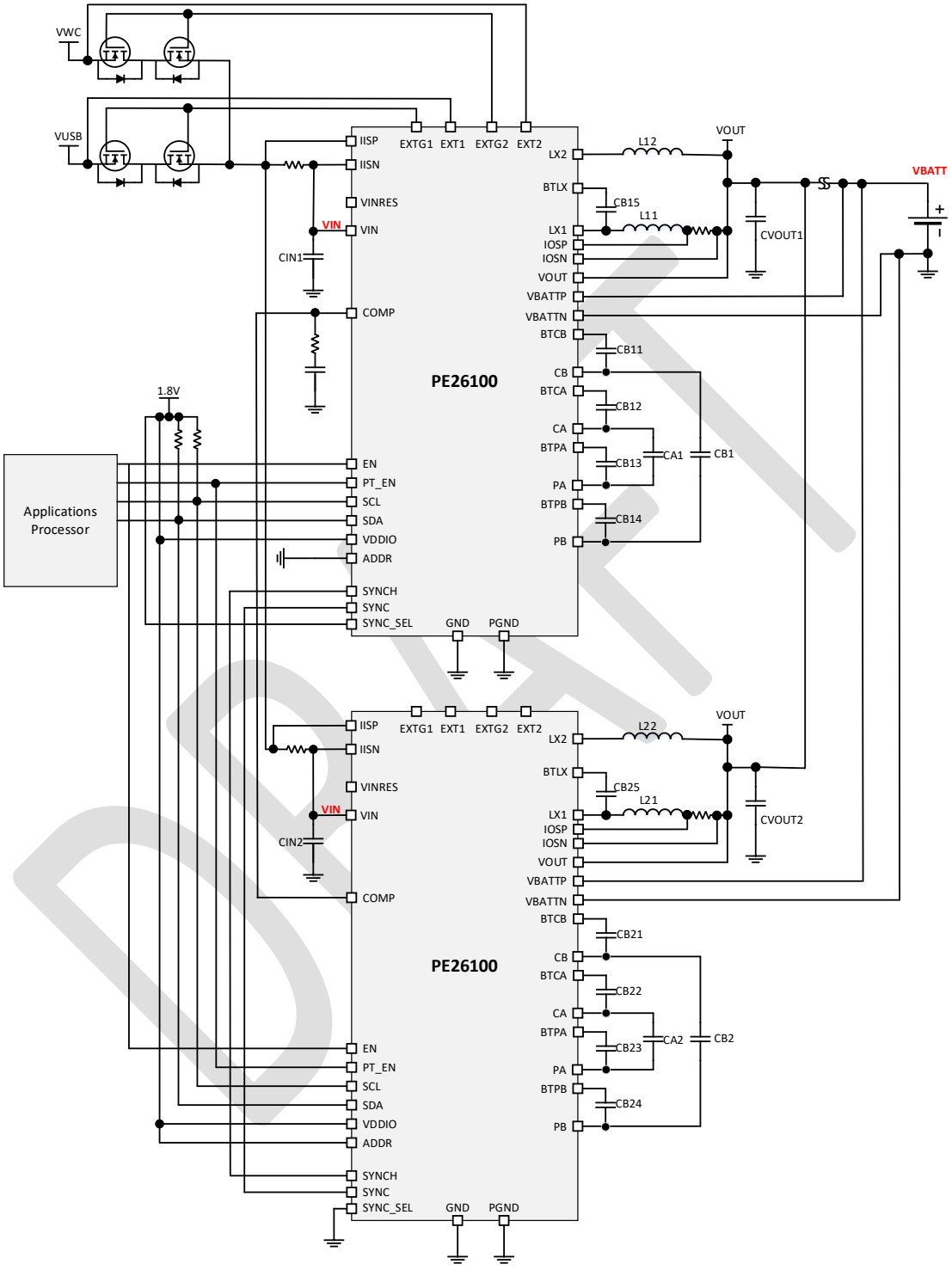


Figure 7. Application Circuit (Dual IC solution with external input current sense resistors)

Functional Block Diagram

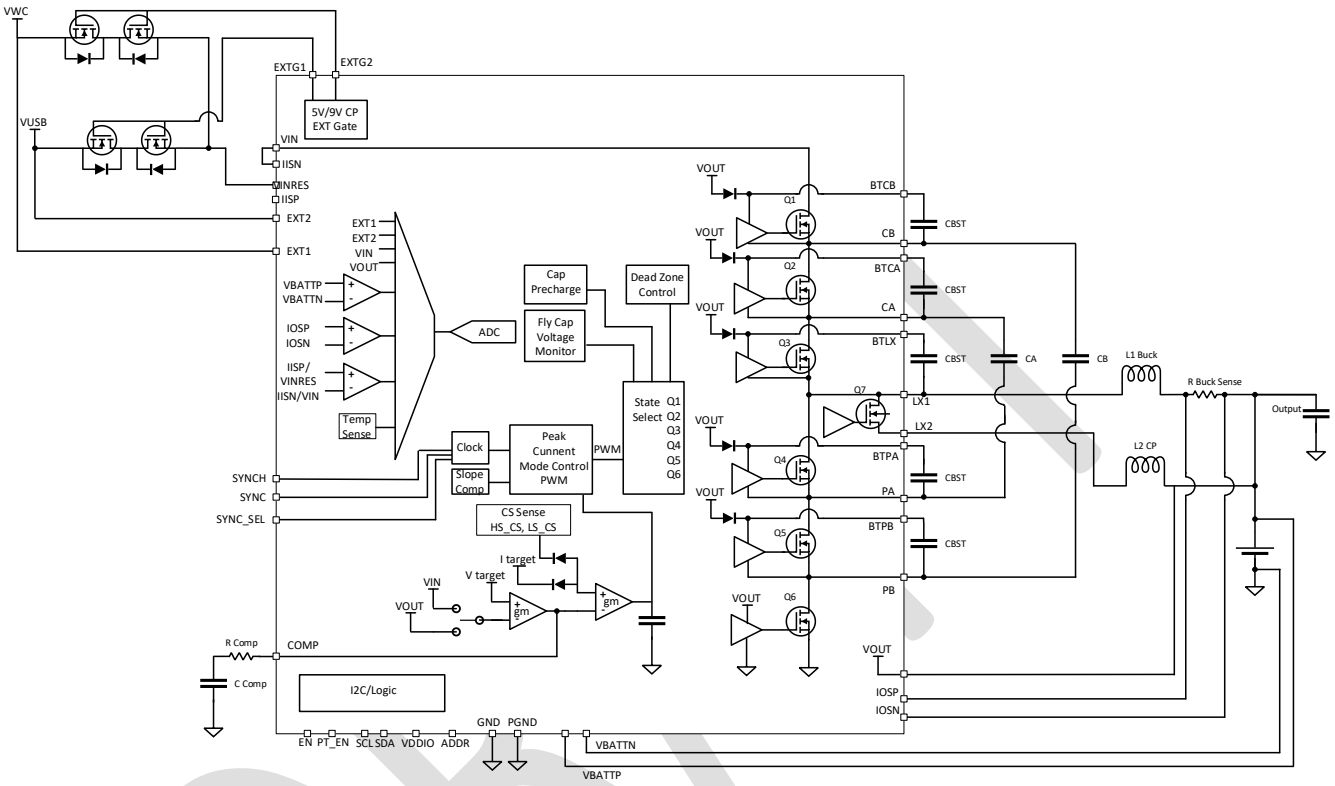


Figure 8. Functional Block Diagram

Detailed Description

The PE26100 uses a proprietary multilevel charge pump technology to deliver superior efficiency in a fully integrated solution. The PE26100 internal bias is provided by the system battery connected to VOUT pin. The charging input can be either USB or wireless input by the external FET register control in PE26100.

The PE26100 can program to three different operating modes: Step-Down Regulation mode, Step-Down Divide-by-3 Charge Pump mode and Reverse Step-Up mode.

In Step-Down Regulation mode, which is set by PT_OPER[1:0] = 00, the PE26100 sets as a multilevel step-down regulator to support USB-PD or fixed input charging. During the Constant-Current (CC) phase, the maximum charging current is limited by the settings in IOUT_MAX and IIN_MAX registers. When the input current does not reach the setting in IIN_MAX register, the charge current is set to the setting in IOUT_MAX register. If the input current reaches the setting in IIN_MAX register, then the charge current throttles and maintains input current at IIN_MAX setting. This allows maximum charging current while ensuring charge current does not go above battery maximum current rating and input current does not trip adapter over-current protection. During Constant-Voltage (CV) phase, the CV regulation is set by VOUT_REG and VBATT_REG registers. VOUT_REG senses at VOUT single-wire sense pin, and VBATT_REG senses at VBATTP and VBATTN differential sense pins. The CV regulates to the lower of the two settings. If VOUT sense voltage reaches VOUT_REG first, then CV is regulated to VOUT_REG. If VBATTP sense voltage reaches VBATT_REG first, then CV is regulated to VBATT_REG. This provides a fast battery top off while prevent pack or cell voltage above safety limit.

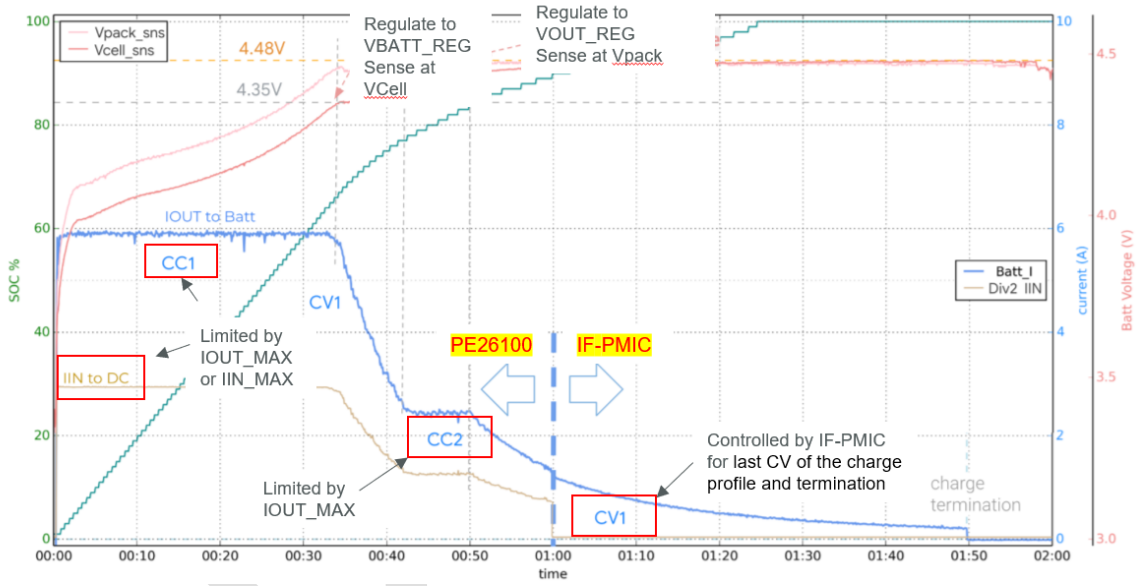


Figure 9. PE26100 Charging Function Diagram in Step Down Regulation Mode
PE26100 covers CCn and CVn in fast charging region, charge termination covered by IF_PMIC
(Temporary example, will be updated)

In Step-down Divide-by-3 Charge Pump Mode, which is set by PT_OPER[1:0] = 01, the PE26100 sets as a divide-by-3 step-down charge divider to support USB-PPS or programmable input charging. The PE26100 gives the voltage and current control to the USB-PPS adapter, and ignore all settings in IOUT_MAX, VOUT_REG and VBATT_REG. It only monitors IIN_MAX setting and shutdown power train and disconnect external FET when IIN current exceeds IIN_MAX setting. The output current is up to 10A in dual IC operation and 5A in single IC operation.

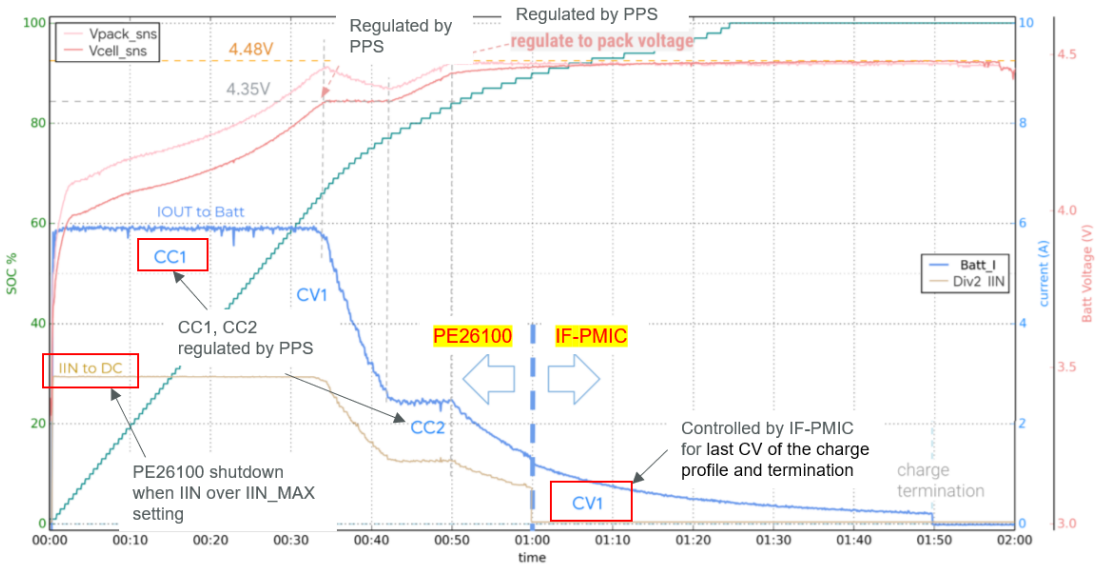


Figure 10. PE26100 Charging Function Diagram in Step Down Divide by 3 Charge Pump Mode
CC and CV regulated by PPS adapter
PE26100 covers CCn and CVn in fast charging region, charge termination covered by IF_PMIC
(Temporary example, will be updated)

In Reverse Step-Up mode, which is set by PT_OPER[1:0] = 10/11, the PE26100 sets as a multilevel step-up regulator to power peripheral device(s) connected to USB or wireless input. The PE26100 takes power from system battery and regulates VIN pin to VOUT_REG programmable setting of 4.8V to 16V. The VIN output current limit is set by IIN_MAX register.

IC, External FET and Power Train Enable

To enable the IC, both EN pin and IC_EN bit must set to logic high (1). When either EN pin or IC_EN bit is logic low, the IC is disable. After IC enables, the POR status bit sets to 1 to indicate IC has a fresh power up.

The PE26100 provides gate driver to control two external N-channel MOSFETs and sense inputs to monitor source input voltage at each FET. The external FETs are controlled by V_EXTG, EXTG_EN and EXTGX[1:0] register bits. V_EXTG bit sets the gate drive voltage and can be set to 9V or 5V. The EXTGX[1:0] bits select which FET(s) to turn on. The EXTG_EN bit enables the gate driver to turn on the selected FET(s). The external FET can be turn on or off independently from other IC operation except when the IC is disable. The EXT_EN_IND status bit set to 1 when external FET is enabled. When a fault is detected and triggers a shutdown, the external FET is turn off automatically. If EXT1 or EXT2 detects an OVP, then the respected FET would not turn on from off mode.

Only enable the power train after all the registers have been initialized and have the target input external FET turn on. Sufficient time based on capacitance on the power path should be given between external FET on time to power train on time to minimize in-rush current. Then set both PT_EN pin and PT_EN bit to logic high (1) to turn on the power train. When either PT_EN pin or PT_EN pin is logic low, the power train is off. In dual IC operation, turn on the slave IC power train first before the master IC. The COMP, SYNC and SYNCH pins from two ICs gate the power train and synchronize the operation. SYNC_SEL pin sets the IC to master mode or slave mode. IC internal fault and programmable fault detection shuts down power train operation when fault is detected.

Initialization and Power Up Sequence, Fault Handling

The following sections show the PE26100 initialization and power up sequence and fault handling for the three different operating modes.

Step-Down Regulation Mode Initialization and Power Up Sequence

The initialization and power up sequence below uses EXT1 as an example. The same sequence applies to EXT2 with the only change in EXTGX bit and related EXT2 register settings.

1. Pull EN to logic high and then set IC_EN bit=1 at 100us(TBD) after EN is logic high to enable IC.
2. IC startup from POR stage, POR bit reports 1 indicating fresh IC startup. Read POR bit to confirm IC is enabled.
3. Set FREQUENCY register to desired setting. In dual IC operation, set both ICs to the same frequency setting.
4. Set VOUT_REG register to target regulation voltage on VOUT sense pin in CV operation.
5. Set VBATT_REG register to target regulation voltage on VBATTP sense pin in CV operation.
6. Set IOUT_MAX register to target maximum charger current in CC operation.
7. Set IIN_MAX register to a value below adapter current limit.
8. Set FAULT and WARNING registers to desired setting. Each Fault and Warning enables at different time based on IC status and operating mode. Details listed in table 7.
9. Set WATCHDOG register to desired setting.
10. Set MODE register with the following:
    a. V_EXTG=1 for 9V gate drive (value depended on selection of external FET)
    b. EXTGX[1:0]=00 for EXT1.
    c. PT_OPER[1:0]=00 for step-down regulation mode.
    d. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - STEP_DN bit=1 for power train setup in step-down regulation mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
11. Set EXTG_EN bit=1 to enable external EXT1 FET. In dual IC operation, the external FETs are controlled by the master IC.
    a. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - EXT_EN_IND bit=1 to indicate external FET is enabled.
    - STEP_DN bit=1 for power train setup in step-down regulation mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
    b. If EXT1 or VIN pin detects OVP event, then IC_STATUS1 and IC_STATUS2 would report:
    IC_STATUS1 readback:
    - SHDN bit=1 to indicate fault shutdown event.
    - IC_OVP bit=1 when EXT1 or VIN OVP triggers IC internal OVP threshold (17V); otherwise, IC_OVP bit=0.
    - Read FLT_STATUS1 register. Either or both VIN_OV_FLT and EXT1_OV_FLT bits=1 depending on fault threshold settings and timing on OVP event.
    IC_STATUS2 readback:
    - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault.

- STEP_DN bit=1 for power train setup in step-down regulation mode.
- REG_SET bit=1 to indicate new register value(s) entered.
To re-enable EXT1 FET after SHDN fault, cycle EXTG_EN bit.

12. Set PT_EN=1 and pull PT_EN pin to logic high to enable power train. In dual IC operation, turn on the slave IC power train first before the master IC.

    a. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - PT_EN_IND bit=1 to indicate power train is enabled.
    - EXT_EN_IND bit=1 to indicate external FET is enabled.
    - STEP_DN bit=1 for power train setup in step-down regulation mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
    - PGOOD bit=1 to indicate power train is ready and charging battery.
    Read ADC registers and STATUS registers and reset watchdog timer if enabled periodically to check IC status during charging operation.

    b. Under any fault event:
    IC_STATUS1 readback:
    - SHDN bit=1 to indicate fault shutdown event.
    - Check IC_STATUS1, FLT_STATUS1 and FLT_STATUS2 register to check for which fault event(s) trigger.
    IC_STATUS2 readback:
    - PT_EN_IND bit=1 to indicate power train is set to enable but it is off due to fault(s).
    - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault(s).
    - STEP_DN bit=1 for power train setup in step-down regulation mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
    - PGOOD bit=0 to indicate power train is off.
    To re-enable power train, repeat step 11 by cycling EXTG_EN bit and then repeat step 12 by cycling PT_EN bit or PT_EN pin.

Step-Down Divide-by-3 Charge Pump Mode Initialization and Power Up Sequence for

The initialization and power up sequence below uses EXT1 as an example. The same sequence applies to EXT2 with the only change in EXTGX bit and related EXT2 register settings.

1. Pull EN to logic high and then set IC_EN bit=1 at 100us(TBD) after EN is logic high to enable IC.
2. IC startup from POR stage, POR bit reports 1 indicating fresh IC startup. Read POR bit to confirm IC is enabled.
3. Set FREQUENCY register to desired setting. In dual IC operation, set both ICs to the same frequency setting.
4. Set IIN_MAX register to a value below adapter current limit. VOUT_REG, VBATT_REG and IOUT_MAX registers are not used in step-down divide-by-3 charge pump mode. Voltage and current regulation in step-down divide-by-3 charge pump mode is controlled by the PPS adapter.
5. Set FAULT and WARNING registers to desired setting. Each Fault and Warning enables at different time based on IC status and operating mode. Details listed in table 7.
6. Set WATCHDOG register to desired setting.
7. Set MODE register with the following:
    a. V_EXTG=1 for 9V gate drive (value depended on selection of external FET)
    b. EXTGX[1:0]=00 for EXT1.
    c. PT_OPER[1:0]=01 for step-down divide-by-3 charge pump mode.

d. Read IC_STATUS1 and IC_STATUS2 registers.
IC_STATUS1 should read back 0x00 with no fault condition.
IC_STATUS2 readback:
- CHRPUMP bit=1 for power train setup in step-down divide-by-3 charge pump mode.
- REG_SET bit=1 to indicate new register value(s) entered.

8. Set EXTG_EN bit=1 to enable external EXT1 FET. In dual IC operation, the external FETs are controlled by the master IC.

   a. Read IC_STATUS1 and IC_STATUS2 registers.
   IC_STATUS1 should read back 0x00 with no fault condition.
   IC_STATUS2 readback:
   - EXT_EN_IND bit=1 to indicate external FET is enabled.
   - CHRPUMP bit=1 for power train setup in step-down divide-by-3 charge pump mode.
   - REG_SET bit=1 to indicate new register value(s) entered.

   b. If EXT1 or VIN pin detects OVP event, then IC_STATUS1 and IC_STATUS2 would report:
   IC_STATUS1 readback:
   - SHDN bit=1 to indicate fault shutdown event.
   - IC_OVP bit=1 when EXT1 or VIN OVP triggers IC internal OVP threshold (17V); otherwise, IC_OVP bit=0.
   - Read FLT_STATUS1 register. Either or both VIN_OV_FLT and EXT1_OV_FLT bits=1 depending on fault threshold settings and timing on OVP event.
   IC_STATUS2 readback:
   - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault.
   - CHRPUMP bit=1 for power train setup in step-down divide-by-3 charge pump mode.
   - REG_SET bit=1 to indicate new register value(s) entered.
   To re-enable EXT1 FET after SHDN fault, cycle EXTG_EN bit.

9. Set PT_EN=1 and pull PT_EN pin to logic high to enable power train. In dual IC operation, turn on the slave IC power train first before the master IC.

   a. Read IC_STATUS1 and IC_STATUS2 registers.
   IC_STATUS1 should read back 0x00 with no fault condition.
   IC_STATUS2 readback:
   - PT_EN_IND bit=1 to indicate power train is enabled.
   - EXT_EN_IND bit=1 to indicate external FET is enabled.
   - CHRPUMP bit=1 for power train setup in step-down divide-by-3 charge pump mode.
   - REG_SET bit=1 to indicate new register value(s) entered.
   - PGOOD bit=1 to indicate power train is ready and charging battery.
   Read ADC registers and STATUS registers and reset watchdog timer if enabled periodically to check IC status during charging operation. Voltage and current regulation in step-down divide-by-3 charge pump mode is controlled by the PPS adapter.

   b. Under any fault event:
   IC_STATUS1 readback:
   - SHDN bit=1 to indicate fault shutdown event.
   - Check IC_STATUS1, FLT_STATUS1 and FLT_STATUS2 register to check for which fault event(s) trigger.
   IC_STATUS2 readback:
   - PT_EN_IND bit=1 to indicate power train is set to enable but it is off due to fault(s).
   - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault(s).
   - CHRPUMP bit=1 for power train setup in step-down divide-by-3 charge pump mode.
   - REG_SET bit=1 to indicate new register value(s) entered.
   - PGOOD bit=0 to indicate power train is off.
   To re-enable power train, repeat step 8 by cycling EXTG_EN bit and then repeat step 9 by cycling PT_EN bit or PT_EN pin.

Reverse Step-Up Mode Initialization and Power Up Sequence

The initialization and power up sequence below uses EXT2 as an example. The same sequence applies to EXT1 with the only change in EXTGX bit and related EXT1 register setting.

1. Pull EN to logic high and then set IC_EN bit=1 at 100us(TBD) after EN is logic high to enable IC.
2. IC startup from POR stage, POR bit reports 1 indicating fresh IC startup. Read POR bit to confirm IC is enabled.
3. Set FREQUENCY register to desired setting. In dual IC operation, set both ICs to the same frequency setting.
4. Set VOUT_REG register to target regulation voltage at VIN.
5. Set IIN_MAX register to target current limit. VBATT_REG and IOUT_MAX registers are not used in reverse step-up mode.
6. Set FAULT and WARNING registers to desired setting. Each Fault and Warning enables at different time based on IC status and operating mode. Details listed in table 7.
7. Set WATCHDOG register to desired setting.
8. Set MODE register with the following:
    a. V_EXTG=1 for 9V gate drive (value depended on selection of external FET).
    b. EXTGX[1:0]=01 for EXT2.
    c. PT_OPER[1:0]=10 or 11 for reverse step-up mode.
    d. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - STEP_UP bit=1 for power train setup in reverse step-up mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
9. Set PT_EN=1 and pull PT_EN pin to logic high to enable power train. In dual IC operation, turn on the slave IC power train first before the master IC.
    a. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - PT_EN_IND bit=1 to indicate power train is enabled.
    - EXT_EN_IND bit=1 to indicate external FET is enabled.
    - STEP_UP bit=1 for power train setup in reverse step-up mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
    - PGOOD bit=1 to indicate power train is ready and VIN ready to load.
    Read ADC registers and STATUS registers and reset watchdog timer if enabled periodically to check IC status during reverse step-up operation.
    b. Under any fault event:
    IC_STATUS1 readback:
    - SHDN bit=1 to indicate fault shutdown event.
    - Check IC_STATUS1, FLT_STATUS1 and FLT_STATUS2 register to check for which fault event(s) trigger.
    IC_STATUS2 readback:
    - PT_EN_IND bit=1 to indicate power train is set to enable but it is off due to fault(s).
    - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault(s).
    - STEP_UP bit=1 for power train setup in reverse step-up mode.
    - REG_SET bit=1 to indicate new register value(s) entered.

- PGOOD bit=0 to indicate power train is off.
To re-enable power train, repeat step 9 by cycling EXTG_EN bit and then repeat step 10 by cycling PT_EN bit or PT_EN pin.

10. Set EXTG_EN bit=1 to enable external EXT2 FET. In dual IC operation, the external FETs are controlled by the master IC.

    a. Read IC_STATUS1 and IC_STATUS2 registers.
    IC_STATUS1 should read back 0x00 with no fault condition.
    IC_STATUS2 readback:
    - EXT_EN_IND bit=1 to indicate external FET is enabled.
    - STEP_UP bit=1 for power train setup in reverse step-up mode.
    - REG_SET bit=1 to indicate new register value(s) entered.

    b. EXT2 or VIN pins should not be detecting OVP as it is set as the output in reverse step-up mode. But if EXT2 or VIN pin detects OVP event, then IC_STATUS1 and IC_STATUS2 would report:
    IC_STATUS1 readback:
    - SHDN bit=1 to indicate fault shutdown event.
    - IC_OVP bit=1 when EXT2 or VIN OVP triggers IC internal OVP threshold (19.5V); otherwise, IC_OVP bit=0.
    - Read FLT_STATUS1 register. Either or both VIN_OV_FLT and EXT2_OV_FLT bits=1 depending on fault threshold settings and timing on OVP event.
    IC_STATUS2 readback:
    - EXT_EN_IND bit=1 to indicate external FET is set to enable but FET is off due to fault.
    - STEP_UP bit=1 for power train setup in reverse step-up mode.
    - REG_SET bit=1 to indicate new register value(s) entered.
    To re-enable EXT2 FET after SHDN fault, cycle EXTG_EN bit.

Fault and Warning Detection Condition

Below table list each fault detection status after its respected mask bit is set to 0. The same detection status applies to warning detection.

FAULT	STEP-DOWN REGULATION MODE	STEP-DOWN DIVIDE-BY-3 CHARGE PUMP MODE	REVERSE STEP-UP MODE	FAULT SHUTDOWN ACTION
TEMP_OT	Always Active	Always Active	Always Active	- Shutdown power train - Disable EXT1 and EXT2 FETs - TEMP_OT_FLT bit=1 - SHDN bit=1 - PGOOD bit=0
IIN_UC	Default: Active after PGOOD bit=1 AA bit 1: Always Active	Active after PGOOD bit=1	Ignored	- Shutdown power train - Disable EXT1 and EXT2 FETs - IIN_UC bit =1 - SHDN bit=1 - PGOOD bit=0
IIN_OC	Active after PGOOD bit=1	Active after PGOOD bit=1	Active after PGOOD bit=1	- Shutdown power train - Disable EXT1 and EXT2 FETs - IIN_OC bit =1 - SHDN bit=1 - PGOOD bit=0
IOUT_OC	Active after PGOOD bit=1	Ignored	Ignored	- Shutdown power train - Disable EXT1 and EXT2 FETs - IOUT_OC bit =1 - SHDN bit=1 - PGOOD bit=0
VIN_UV	Active after EXT_EN_IND bit=1	Active after EXT_EN_IND bit=1	Active after PGOOD bit=1	- Shutdown power train - Disable EXT1 and EXT2 FETs - VIN_UV bit =1 - SHDN bit=1 - PGOOD bit=0
VIN_OV	Active after EXT_EN_IND bit=1	Active after EXT_EN_IND bit=1	Active after EXT_EN_IND bit=1	- Shutdown power train - Disable EXT1 and EXT2 FETs - VIN_OV bit =1 - SHDN bit=1 - PGOOD bit=0

FAULT	STEP-DOWN REGULATION MODE	STEP-DOWN DIVIDE-BY-3 CHARGE PUMP MODE	REVERSE STEP-UP MODE	FAULT SHUTDOWN ACTION
EXT1_OV	Always Active	Always Active	Always Active	At or after EXTG_EN bit=1: - Disable EXT1 and EXT2 FETs - EXT1_OV_FLT bit=1 and/or EXT2_OV_FLT bit=1 - SHDN bit=1 During power train operation: - Shutdown power train - Disable EXT1 and EXT2 FETs - EXT1_OV_FLT bit=1 and/or EXT2_OV_FLT bit=1 - SHDN bit=1
EXT2_OV	Always Active	Always Active	Always Active	
VBATT_UV	Always Active	Always Active	Always Active	- Shutdown power train - Disable EXT1 and EXT2 FETs - VBATT_UV bit =1 - SHDN bit=1 - PGOOD bit=0
VBATT_OV	Always Active	Always Active	Always Active	- Shutdown power train - Disable EXT1 and EXT2 FETs - VBATT_OV bit =1 - SHDN bit=1 - PGOOD bit=0
VOUT_UV	Always Active	Always Active	Always Active	- Shutdown power train - Disable EXT1 and EXT2 FETs - VOUT_UV bit =1 - SHDN bit=1 - PGOOD bit=0
VOUT_OV	Always Active	Always Active	Always Active	- Shutdown power train - Disable EXT1 and EXT2 FETs - VOUT_OV bit =1 - SHDN bit=1 - PGOOD bit=0

Table 7. Fault and Warning detection

IC Built-In Fault Detection

Below table list each built-in fault detection. These detections are comparator based to provide a fast response and are enabled in all operating modes unless otherwise specified.

FAULT	DESCRIPTION	FAULT SHUTDOWN ACTION
IC overtemperature Protection	Fault triggers when IC junction temperature is over 160°C.	- Shutdown power train - Disable EXT1 and EXT2 FETs - IC_OTP bit=1 - SHDN bit=1 - PGOOD bit=0
IC VIN overvoltage protection	Fault triggers when VIN, EXT1 or EXT2 pin voltage is over 19.5V.	- Shutdown power train - Disable EXT1 and EXT2 FETs - IC_OVP bit =1 - SHDN bit=1 - PGOOD bit=0
IC VIN undervoltage protection	Fault triggers when VIN is 1.2V typical below VOUT.	- Shutdown power train - Disable EXT1 and EXT2 FETs - IC_UVP bit =1 - SHDN bit=1 - PGOOD bit=0
IC VOUT undervoltage protection	Fault triggers when VOUT is below 3V.	- Shutdown power train - Disable EXT1 and EXT2 FETs - I^2C communication disables
IC VDDIO undervoltage protection	Fault triggers when VDDIO is below TBDV.	- Shutdown power train - Disable EXT1 and EXT2 FETs - I^2C communication disables
IC IOUT output overcurrent	Fault triggers when output current is over 5A. This fault is only enabled in step-down regulation mode and step-down divide-by-3 charge pump mode.	- Shutdown power train - Disable EXT1 and EXT2 FETs - IC_ILM bit =1 - SHDN bit=1 - PGOOD bit=0
IC Reverse step-up softstart timeout	Fault triggers when VIN is not ready passed softstart timeout limit of 10ms. This fault is only enabled in reverse step-up mode.	- Shutdown power train - Disable EXT1 and EXT2 FETs - REVERSE_TIMEOUT bit =1 - SHDN bit=1 - PGOOD bit=0

Table 8. IC built-in fault detection

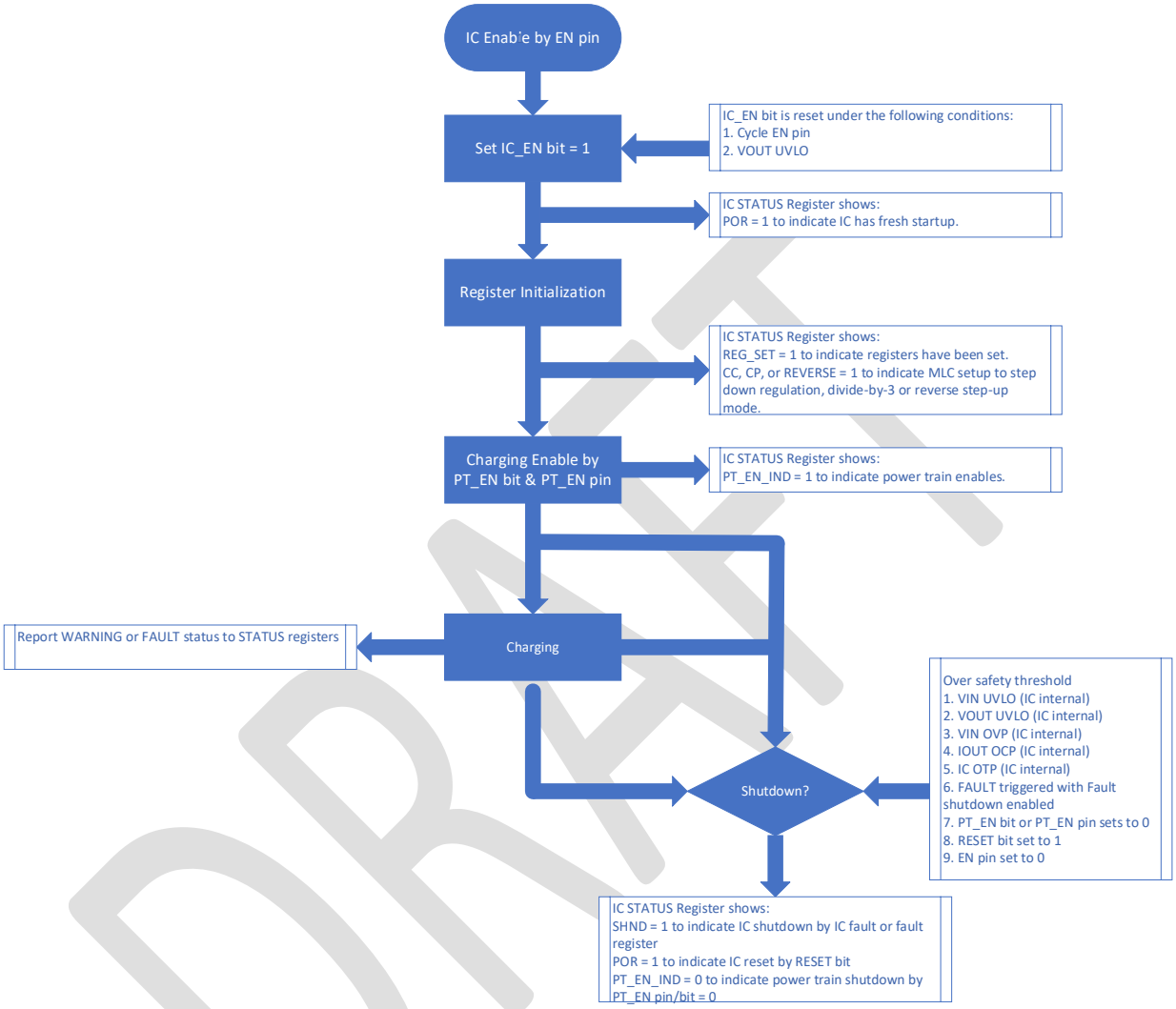


Figure 11. PE26100 Initialization and Operation Flow Chart (Need update)

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The PE26100 operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps), fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as VOUT and VDDIO voltages remain above UVLO and the EN pin remain asserted.

The data transfer protocol for standard and fast modes is the same, therefore they are referred to as F/S-mode in this document. The PE26100 supports 7-bit addressing; 10-bit addressing, and general call address are not supported. The device 7-bit address is defined as '1101XXX'.

Programming I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple PE26100 parts to be addressed on one I²C bus, the lower 3 bits of the I²C slave address are programmable by using the ADDR pin. The ADDR pin configuration to the device 7-bit address and 8-bit address with R/Wb low is shown in Table .

ADDR PIN	DEVICE 7 BIT ADDRESS	DEVICE 8 BIT ADDRESS WITH R/=0
Tied to AGND	110 1010 (0x62)	1101 0100 (0xD4)
Floating	110 1111(0x6F)	1101 1110 (0xDE)
Tied to VDDIO	110 1101 (0x65)	1101 1010 (0xDA)

Table 8. ADDR Pin Configuration

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure . All I²C-compatible devices should recognize a start condition.

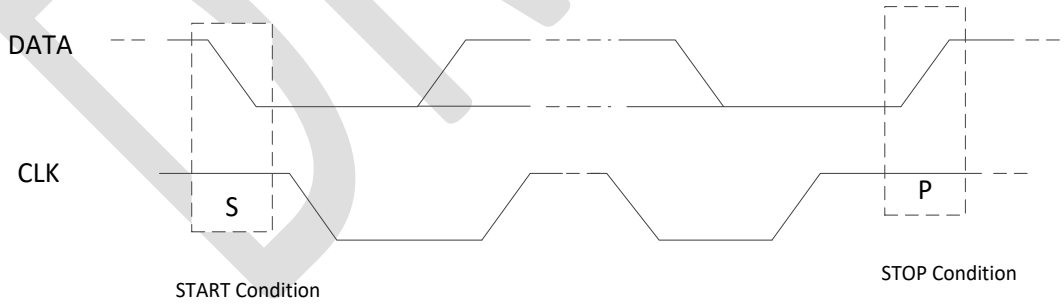


Figure 12. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/Wb on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. See Figure , Bit Transfer on the Serial Interface.

The master generates further SCL cycles to either transmit data to the slave (R/Wb bit 0) or receive data from the slave (R/Wb bit 1). In either case, the receiver needs to acknowledge the data sent by transmitter. So, an acknowledge signal can either be

generated by the master or by the slave, depending on which one is the receiver. Nine-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure . This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

PE26100 I^2C Update Sequence

The PE26100 requires a start condition, a valid I^2C address, a register address byte, and a data byte for a single update. After the receipt of each byte, PE26100 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects PE26100. The PE26100 performs an update on the falling edge of the acknowledge signal that follows the LSB.

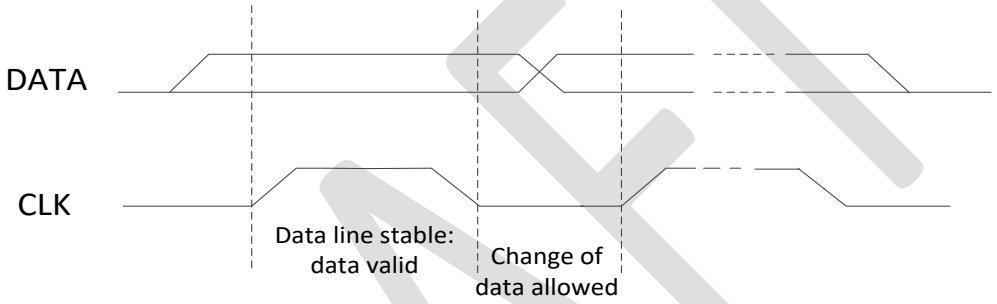


Figure 13. Bit Transfer on the Serial Interface

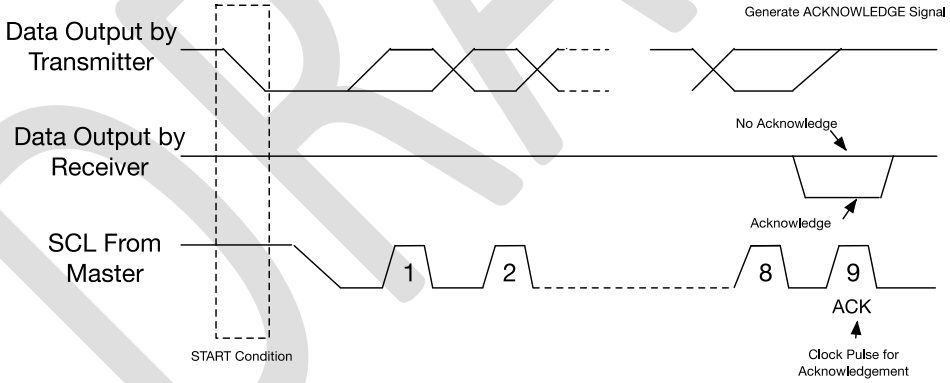


Figure 14. Acknowledge on the I^2C Bus

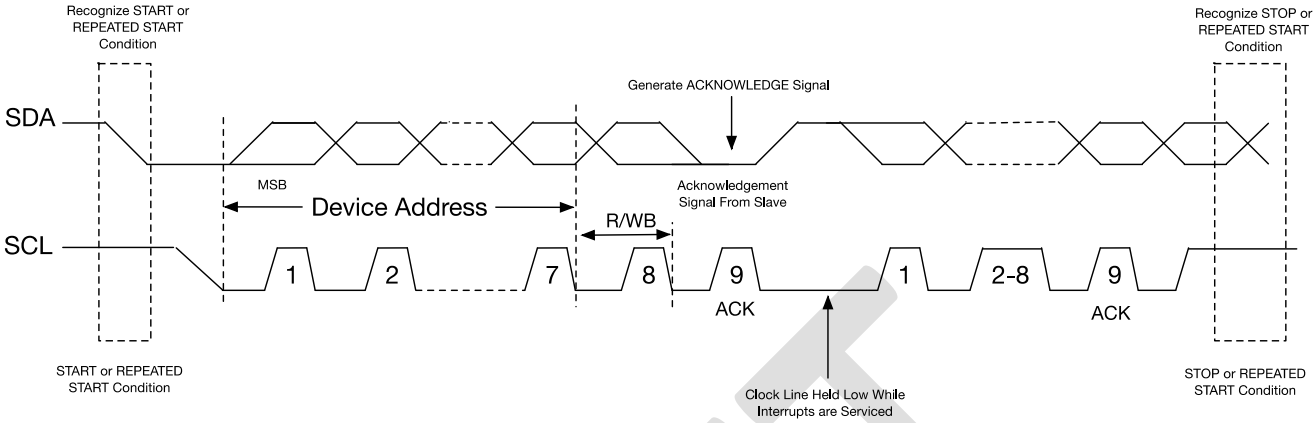


Figure 15. Bus Protocol

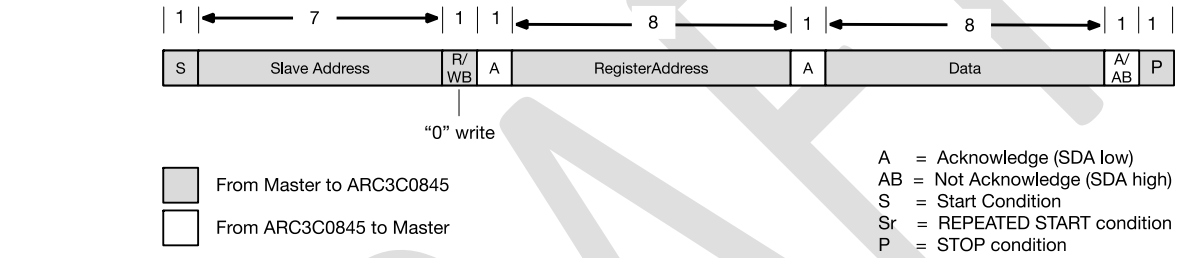


Figure 14. "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

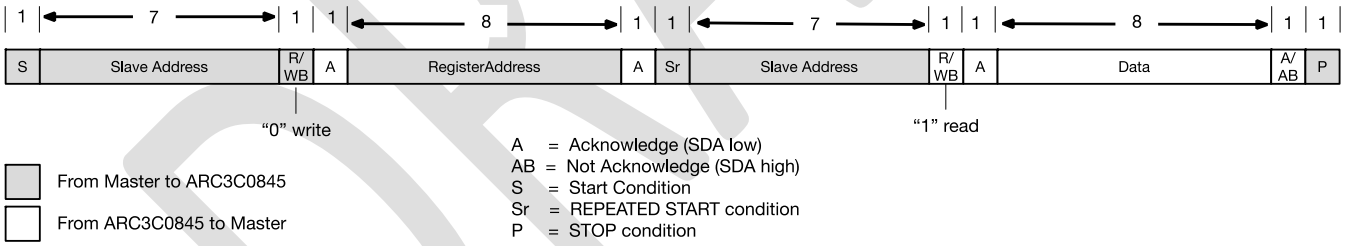


Figure 16. "Read" Data Transfer Format in Standard, Fast, Fast-Plus Modes

Register Maps (For reference only, subject to change)

7-bit I²C Slave Address: 0x6A (ADDR=0), 0x6D (ADDR=1), 0x6F (ADDR=Float)

Register Configuration Parameters

REGISTER	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL										
IC_ENABLE	0x00	R/$\overline{w}$	RESERVED							IC_EN
MODE	0x01	R/$\overline{w}$	EXTG_EN	V_EXTG	EXTGX[1:0]		VINRES	PT_OPER[1:0]		PT_EN
FREQUENCY	0X02	R/$\overline{w}$	MLC_3L/4L	RESERVED			DITHER	FSW[2:0]		
VOUT_REG	0x03	R/$\overline{w}$	VOUT_REG[7:0]							
VBATT_REG	0x04	R/$\overline{w}$	VBATT_REG[7:0]							
IOUT_MAX	0x05	R/$\overline{w}$	IOUT_MAX[7:0]							
IIN_MAX	0x06	R/$\overline{w}$	IIN_MAX[7:0]							
TELEMETRY										
TEMP_ADC	0x07	R	TEMP_ADC[7:0]							
IIN_ADC_LB	0x08	R	IIN_ADC[1:0]		RESERVED					
IIN_ADC_UB	0x09	R	IIN_ADC[9:2]							
IOUT_ADC	0x0A	R	IOUT_ADC[7:0]							
VIN_ADC_LB	0x0B	R	VIN_ADC[1:0]		RESERVED					
VIN_ADC_UB	0x0C	R	VIN_ADC[9:2]							
VBATT_ADC _LB	0x0D	R	VBATT_ADC[1:0]		RESERVED					
VBATT_ADC _UB	0x0E	R	VBATT_ADC[9:2]							
WARNING and FAULT										
TEMP_OT	0x0F	R/$\overline{w}$	TEMP_OT[7:0]							
IIN_UC	0x10	R/$\overline{w}$	IIN_UC[7:0]							
IIN_OC	0x11	R/$\overline{w}$	IIN_OC[7:0]							
IOUT_OC	0x12	R/$\overline{w}$	IOUT_OC[7:0]							
VIN_UV	0x13	R/$\overline{w}$	VIN_UV[7:0]							
VIN_OV	0x14	R/$\overline{w}$	VIN_OV[7:0]							
EXT1_OV	0x15	R/$\overline{w}$	EXT1_OV[7:0]							
EXT2_OV	0x16	R/$\overline{w}$	EXT2_OV[7:0]							
VBATT_UV	0x17	R/$\overline{w}$	VBATT_UV[7:0]							
VBATT_OV	0x18	R/$\overline{w}$	VBATT_OV[7:0]							
VOUT_UV	0x19	R/$\overline{w}$	VOUT_UV[7:0]							
VOUT_OV	0x1A	R/$\overline{w}$	VOUT_OV[7:0]							
TEMP_OT_ WARN	0x1B	R/$\overline{w}$	TEMP_OT_WARN[7:0]							
IIN_UC_ WARN	0x1C	R/$\overline{w}$	IIN_UC_WARN [7:0]							
IIN_OC_ WARN	0x1D	R/$\overline{w}$	IIN_OC_WARN [7:0]							

REGISTER	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
IOUT_OC_WARN	0x1E	R/$\overline{w}$	IOUT_OC_WARN [7:0]							
VIN_UV_WARN	0x1F	R/$\overline{w}$	VIN_UV_WARN [7:0]							
VIN_OV_WARN	0x20	R/$\overline{w}$	VIN_OV_WARN [7:0]							
EXT1_OV_WARN	0x21	R/$\overline{w}$	EXT1_OV_WARN [7:0]							
EXT2_OV_WARN	0x22	R/$\overline{w}$	EXT2_OV_WARN [7:0]							
VBATT_UV_WARN	0x23	R/$\overline{w}$	VBATT_UV_WARN [7:0]							
VBATT_OV_WARN	0x24	R/$\overline{w}$	VBATT_OV_WARN [7:0]							
VOUT_UV_WARN	0x25	R/$\overline{w}$	VOUT_UV_WARN [7:0]							
VOUT_OV_WARN	0x26	R/$\overline{w}$	VOUT_OV_WARN [7:0]							
FLT_SHDN1	0x27	R/$\overline{w}$	TEMP_OT_FLT_SHDN	IIN_UC_FLT_SHDN	IIN_OC_FLT_SHDN	IOUT_OC_FLT_SHDN	VIN_UV_FLT_SHDN	VIN_OV_FLT_SHDN	EXT1_OV_FLT_SHDN	EXT2_OV_FLT_SHDN
FLT_SHDN2	0x28	R/$\overline{w}$	RESERVED				VBATT_UV_FLT_SHDN	VBATT_OV_FLT_SHDN	VOUT_UV_FLT_SHDN	VOUT_OV_FLT_SHDN
FLT_ACTIVE	0x29	R/$\overline{w}$	RESERVED	IIN_UC_FLT_ACT	IIN_OC_FLT_ACT	IOUT_OC_FLT_ACT	VIN_UV_FLT_ACT	VIN_OV_FLT_ACT	RESERVED	RESERVED
FLT_MASK1	0x2A	R/$\overline{w}$	TEMP_OT_FLT_MASK	IIN_UC_FLT_MASK	IIN_OC_FLT_MASK	IOUT_OC_FLT_MASK	VIN_UV_FLT_MASK	VIN_OV_FLT_MASK	EXT1_OV_FLT_MASK	EXT2_OV_FLT_MASK
FLT_MASK2	0x2B	R/$\overline{w}$	RESERVED				VBATT_UV_FLT_MASK	VBATT_OV_FLT_MASK	VOUT_UV_FLT_MASK	VOUT_OV_FLT_MASK
WARN_MASK1	0x2C	R/$\overline{w}$	TEMP_OT_WARN_MASK	IIN_UC_WARN_MASK	IIN_OC_WARN_MASK	IOUT_OC_WARN_MASK	VIN_UV_WARN_MASK	VIN_OV_WARN_MASK	EXT1_OV_WARN_MASK	EXT2_OV_WARN_MASK
WARN_MASK2	0x2D	R/$\overline{w}$	RESERVED				VBATT_UV_WARN_MASK	VBATT_OV_WARN_MASK	VOUT_UV_WARN_MASK	VOUT_OV_WARN_MASK
DEGLITCH	0x2E	R/$\overline{w}$	RESERVED			DEGLITCH[4:0]				
WATCHDOG										
WATCHDOG	0x2F	R/$\overline{w}$	RESERVED			WD_RESET	WD_I2C_RESET	WD_ENABLE	WD_TIME[1:0]	
SYSTEM TEMPERATURE										
TEMP_LIM	0x30	R/$\overline{w}$	TEMP_LIM[7:0]							
TEMP_SYS	0x31	R/$\overline{w}$	TEMP_SYS[7:0]							
STATUS										
FLT_STATUS1	0x32	R	TEMP_OT_FLT	IIN_UC_FLT	IIN_OC_FLT	IOUT_OC_FLT	VIN_UV_FLT	VIN_OV_FLT	EXT1_OV_FLT	EXT2_OV_FLT
FLT_STATUS2	0x33	R	RESERVED				VBATT_UV_FLT	VBATT_OV_FLT	VOUT_UV_FLT	VOUT_OV_FLT
WARN_STATUS1	0x34	R	TEMP_OT_WARN	IIN_UC_WARN	IIN_OC_WARN	IOUT_OC_WARN	VIN_UV_WARN	VIN_OV_WARN	EXT1_OV_WARN	EXT2_OV_WARN
WARN_STATUS2	0x35	R	RESERVED				VBATT_UV_WARN	VBATT_OV_WARN	VOUT_UV_WARN	VOUT_OV_WARN
IC_STATUS1	0x36	R	IC_OTP	IC_OCP	IC_OVP	REVERSE_SSTIMOUT	WD_TIMEOUT		SYS_OTP	SHDN
IC_STATUS2	0x37	R	PGOOD	STEP_UP	CHRPUMP	STEP_DN	EXT_EN_IND	PT_EN_IND	REG_SET	POR

Detailed Register Description

Register IC_ENABLE (0x00)

The IC_ENABLE register has a single data byte associated with it. This register has a control bit to enable/disable the IC.

ADDRESS	NAME	POR VALUE
0x00	I2C	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED							IC_EN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:1]	R	0000 000	Reserved bits
IC_EN	[0]	R/$\overline{w}$	0	IC Enable bit. This bit has an 'AND' function with the EN pin. 0 = IC disables, all registers reset back to POR value. 1 = IC enables.

Register MODE (0x01)

The MODE register has a single data byte associated with it. This register is used for enabling the power train, external gates and power train operation of the part. Only set PT_EN bit after all register bits are set.

ADDRESS	NAME	POR VALUE
0x01	MODE	00h

Bit Assignment

7	6	5	4	3	2	1	0
EXTG_EN	V_EXTG	EXTGX[1:0]		VINRES	PT_OPER[1:0]		PT_EN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
EXTG_EN	[7]	R/$\overline{w}$	0	EXTGX Enable bit 0 = EXTG1 and EXTG2 disable 1 = EXTG1 and/or EXTG2 enables based on EXTGX bit
V_EXTG	[6]	R	0	Select gate driver voltage on the external B-B FET. 0 = 5V 1 = 9V
EXTGX[1:0]	[5:4]	R/$\overline{w}$	0	Select EXTG1 or EXTG2 enable when EXTG_EN bit = 1. When EXT_EN bit = 0, EXTGX bit is don't care. 00 = EXTG1 selected 01 = EXTG2 selected 10 or 11 = Both EXTG1 and EXTG2 selected
VINRES	[3]	R	0	Enable or disable internal input current sense 0 = Enable internal input current sense 1 = Disable internal input current sense (when internal input current sense is disabled, the PE26100 use external current sense resistor connect to IISP and IISN to detect input current)
PT_OPER[1:0]	[2:1]	R/$\overline{w}$	00	Power Train Operation Selection bits 00 = Step-down Regulation Mode (6A VOUT Charging) 01 = Step-down Divide-by-3 Charge Pump Mode (PPS Charging) 10 or 11 = Reverse Step-up Mode
PT_EN	[0]	R/$\overline{w}$	0	Power Train Enable bit. This bit has an 'AND' function with the PT_EN pin. 0 = Power Train disables 1 = Power Train enables

Register FREQUENCY (0x02)

The FREQUENCY register has a single data byte associated with it. This register is used for setting multilevel charge pump converter switching frequency and enabling LX dither function of the part.

ADDRESS	NAME	POR VALUE
0x02	FREQUENCY	03h

Bit Assignment

7	6	5	4	3	2	1	0
MLC_3L/4L	RESERVED			DITHER	FSW[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
MLC_3L/4L	[7]	R/$\overline{w}$	0	Select Step-down Regulation Mode in 3level or 4level mode and select Step-down Charge Pump Mode in Divide-by-2 or Divide-by-3 mode: 0 = 4level and divide-by-3 1 = 3level and divide-by-2
RESERVED	[6:4]	R	000	Reserved Bit
DITHER	[3]	R/$\overline{w}$	0	Enable LX dither function: 0 = Dither function disables 1 = Enable dither where switching frequency is dithered around switching frequency setting
FSW[2:0]	[2:0]	R/$\overline{w}$	011	Set converter switching frequency: 000 = 2MHz 001 = 1.5 MHz 010 = 1.2 MHz 011 = 1 MHz (Default) 100 = 800 kHz 101 = 750 kHz 110 = 600 kHz 111 = 500 kHz

Register VOUT_REG (0x03)

The VOUT_REG register has a single data byte associated with it. This register sets the VOUT regulation voltage in step-down regulation mode and reverse step-up voltage at VIN.

ADDRESS	NAME	POR VALUE
0x03	VOUT_REG	00h

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_ REG7	VOUT_ REG6	VOUT_ REG5	VOUT_ REG4	VOUT_ REG3	VOUT_ REG2	VOUT_ REG1	VOUT_ REG0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VOUT_REG [7:0]	[7:0]	R/$\overline{w}$	0000 0000	In Step-Down Regulation mode, which is set by PT_OPER[1:0] = 00, the VOUT_REG [7:0] bits set the step-down regulation output voltage at VOUT pin. The LSB is 10mV. The programmable range is 2.56V to 5.11V, with code 0 = 2.56V In Reverse Step-Up mode, which is set by PT_OPER[1:0] = 10 or 11, the VOUT_REG [7:0] bits set the reverse step-up regulation output voltage at VIN pin. The LSB is 80mV. The programmable range is 0V to 16V, with code 0 = 0V.

Register VBATT_REG (0x04)

The VBATT_REG register has a single data byte associated with it. This register sets the VBATT regulation voltage in step-down regulation mode at VBATTP and VBATTN remote sense pins. If VBATTP and VBATTN remote sense pins are not used, then the VBATT_REG register setting is ignored.

ADDRESS	NAME	POR VALUE
0x04	VBATT_REG	00h

Bit Assignment

7	6	5	4	3	2	1	0
VBATT_ REG7	VBATT_ REG6	VBATT_ REG5	VBATT_ REG4	VBATT_ REG3	VBATT_ REG2	VBATT_ REG1	VBATT_ REG0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_REG [7:0]	[7:0]	R/$\overline{w}$	0000 0000	Set the step-down regulation output voltage at VBATTP and VBATTN remote sense pins. The LSB is 10mV. The programmable range is 2.56V to 5.11V, with code 0 = 2.56V.

Register IOUT_MAX (0x05)

The IOUT_MAX register has a single data byte associated with it. This register sets the IOUT current limit in step-down regulation mode.

ADDRESS	NAME	POR VALUE
0x05	IOUT_MAX	00h

Bit Assignment

7	6	5	4	3	2	1	0
IOUT_MAX7	IOUT_MAX6	IOUT_MAX5	IOUT_MAX4	IOUT_MAX3	IOUT_MAX2	IOUT_MAX1	IOUT_MAX0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IOUT_MAX[7:0]	[7:0]	R/$\overline{w}$	0000 0000	The IOUT_MAX[7:0] bits set the IOUT constant current limit in step down regulation mode. The LSB is 100uV (25mA with a 4mΩ sense resistor). The programmable range is 0V to 24mV, with code 0 = 0V. The controllable range starts at 1mV. The target IOUT_MAX setting current should not exceed 5A or 20mV with a 4mΩ sense resistor.

Register IIN_MAX (0x06)

The IIN_MAX register has a single data byte associated with it. This register sets the step-down IIN current limit and reverse step-up output current limit at VIN pin. This register also sets the IIN current limit shutdown threshold in Step-down Divide-by-3 Charge Pump Mode. When IIN hits the threshold set by this register, then PE26100 enters into power train fault shutdown mode, which shutdowns the power train and disables the external back to back FETs.

ADDRESS	NAME	POR VALUE
0x06	IIN_MAX	00h

Bit Assignment

7	6	5	4	3	2	1	0
IIN_MAX7	IIN_MAX6	IIN_ MAX5	IIN_MAX4	IIN_MAX3	IIN_MAX2	IIN_MAX1	IIN_MAX0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_MAX[7:0]	[7:0]	R/$\overline{w}$	0000 0000	The IIN_MAX[7:0] bits set the VIN input current limit in step-down mode and VIN output current limit in reverse step-up mode. With internal sensing (VINRES=0), the LSB is 40mA. The ADC range is 0A to 8A, with code 0 = 0A. The controllable range starts at 400mA. With external sensing (VINRES=1), the LSB is 200uV (20mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V. The controllable range starts at 2mV.

Register TEMP_ADC (0x07)

The TEMP_ADC register has a single data byte associated with it. This register reports the IC temperature ADC reading.

ADDRESS	NAME	POR VALUE
0x07	TEMP_ADC	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_ADC7	TEMP_ADC6	TEMP_ADC5	TEMP_ADC4	TEMP_ADC3	TEMP_ADC2	TEMP_ADC1	TEMP_ADC0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_ADC[7:0]	[7:0]	R	0000 0000	TEMP_ADC[7:0] bits reports the IC temperature ADC reading in 2's complement format. The LSB is 2℃. Please see decode table below for -40℃ to 160℃ readings. 1110 1100 = -40℃ ..... 1111 0001 = -30℃ ..... 1111 0110 = -20℃ ..... 1111 1011 = -10℃ ..... 0000 0000 = 0℃ ..... 0000 0101 = 10℃ ..... 0000 1010 = 20℃ ..... 0000 1111 = 30℃ ..... 0001 0100 = 40℃ ..... 0001 1001 = 50℃ ..... 0001 1110 = 60℃ 0010 0011 = 70℃ ..... 0010 1000 = 80℃ ..... 0010 1101 = 90℃ ..... 0011 0010 = 100℃ ..... 0011 0111 = 110℃ ..... 0011 1100 = 120℃ ..... 0100 0001 = 130℃ ..... 0100 0110 = 140℃ ..... 0100 1011 = 150℃ ..... 0101 0000 = 160℃

Register IIN_ADC (0x08, 0x09)

The IIN_ADC register has two datas byte associated with it. This register reports the input current ADC reading.

ADDRESS	NAME	POR VALUE
0x08	IIN_ADC_LB	00h
0x09	IIN_ADC_UB	00h

Bit Assignment

BYTE NAME	7	6	5	4	3	2	1	0
IIN_ADC_LB	IIN_ADC1	IIN_ADC0	RESERVED					
IIN_ADC_UB	IIN_ADC9	IIN_ADC8	IIN_ADC7	IIN_ADC6	IIN_ADC5	IIN_ADC4	IIN_ADC3	IIN_ADC2

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_ADC [9:0]	IIN_ADC[9:0]	R	00 0000 0000	IIN_ADC[9:0] bits report the input current sense resistor voltage ADC reading. With internal sensing (VINRES=0), the LSB is 10mA. The ADC range is 0A to 8A, with code 0 = 0A. With external sensing (VINRES=1), the LSB is 50uV (5mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V. In reverse step-up mode, IIN_ADC reports current going out of VIN pin.

Register IOUT_ADC (0x0A)

The IOUT_ADC register has a single data byte associated with it. This register reports the battery current ADC reading.

ADDRESS	NAME	POR VALUE
0x0A	IOUT_ADC	00h

Bit Assignment

7	6	5	4	3	2	1	0
IOUT_ADC7	IOUT_ADC6	IOUT_ADC5	IOUT_ADC4	IOUT_ADC3	IOUT_ADC2	IOUT_ADC1	IOUT_ADC0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IOUT_ADC[7:0]	[7:0]	R	0000 0000	IOUT_ADC[7:0] bits report the output current sense resistor voltage ADC reading. The LSB is 100uV (25mA with a 4mΩ sense resistor). The ADC range is 0V to 24mV, with code 0 = 0V. In reverse step-up mode, IOUT_ADC reports current going into the VOUT pin.

Register VIN_ADC (0x0B, 0x0C)

The VIN_ADC register has two data bytes associated with it. This register reports the input voltage ADC reading.

ADDRESS	NAME	POR VALUE
0x0B	VIN_ADC_LB	00h
0x0C	VIN_ADC_UB	00h

Bit Assignment

BYTE NAME	7	6	5	4	3	2	1	0
VIN_ADC_LB	VIN_ADC1	VIN_ADC0	RESERVED					
VIN_ADC_UB	VIN_ADC9	VIN_ADC8	VIN_ADC7	VIN_ADC6	VIN_ADC5	VIN_ADC4	VIN_ADC3	VIN_ADC2

Bit Description

FIELD NAME	BITS	TYP	POR	DESCRIPTION
VIN_ADC[9:0]	VIN_ADC_LB [7:6] VIN_ADC_UB [7:0]	R	00 0000 0000	VIN_ADC[9:0] bits reports the input voltage ADC reading. The LSB is 20mV. The ADC range is 0V to 20V, with code 0 = 0V.

Register VBATT_ADC (0x0D, 0x0E)

The VBATT_ADC register has two data bytes associated with it. This register reports VBATT ADC reading. If VBATTP and VBATTN remote sense pins are not used, then the VBATT ADC reports back reading from VOUT pin.

ADDRESS	NAME	POR VALUE
0x0D	VBATT_ADC_LB	00h
0x0E	VBATT_ADC_UB	00h

Bit Assignment

BYTE NAME	7	6	5	4	3	2	1	0
VBATT_ADC_LB	VBATT_ADC1	VBATT_ADC0	RESERVED					
VBATT_ADC_UB	VBATT_ADC9	VBATT_ADC8	VBATT_ADC7	VBATT_ADC6	VBATT_ADC5	VBATT_ADC4	VBATT_ADC3	VBATT_ADC2

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_ ADC[9:0]	VBATT_ADC_ LB [7:5] VBATT_ADC_ UB [7:0]	R	00 0000 0000	VBATT_ADC[9:0] bits reports the input voltage ADC reading. The LSB is 5mV. The ADC range is 0V to 5V, with code 0 = 0V.

Register TEMP_OT (0x0F)

The TEMP_OT register has a single data byte associated with it. This register sets the IC over-temperature fault threshold.

ADDRESS	NAME	POR VALUE
0x0F	TEMP_OT	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT7	TEMP_OT6	TEMP_OT5	TEMP_OT4	TEMP_OT3	TEMP_OT2	TEMP_OT1	TEMP_OT0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT[7:0]	[7:0]	R/$\overline{w}$	0000 0000	TEMP_OT[7:0] bits set the IC over-temperature fault threshold in 2's complement format. The LSB is 2℃. Please see decode table below for -40℃ to 160℃ settings. 1110 1100 = -40℃ ..... 1111 0001 = -30℃ ..... 1111 0110 = -20℃ ..... 1111 1011 = -10℃ ..... 0000 0000 = 0℃ ..... 0000 0101 = 10℃ ..... 0000 1010 = 20℃ ..... 0000 1111 = 30℃ ..... 0001 0100 = 40℃ ..... 0001 1001 = 50℃ ..... 0001 1110 = 60℃ 0010 0011 = 70℃ ..... 0010 1000 = 80℃ ..... 0010 1101 = 90℃ ..... 0011 0010 = 100℃ ..... 0011 0111 = 110℃ ..... 0011 1100 = 120℃ ..... 0100 0001 = 130℃ ..... 0100 0110 = 140℃ ..... 0100 1011 = 150℃ ..... 0101 0000 = 160℃

Register IIN_UC (0x10)

The IIN_UC register has a single data byte associated with it. This register sets the input under-current fault threshold.

ADDRESS	NAME	POR VALUE
0x10	IIN_UC	00h

Bit Assignment

7	6	5	4	3	2	1	0
IIN_UC7	IIN_UC6	IIN_UC5	IIN_UC4	IIN_UC3	IIN_C2	IIN_UC1	IIN_UC0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_UC[7:0]	[7:0]	R/$\overline{w}$	0000 0000	IIN_UC[7:0] bits set the input under-current fault threshold. With internal sensing (VINRES=0), the LSB is 40mA. The ADC range is 0A to 8A, with code 0 = 0A. With external sensing (VINRES=1), the LSB is 200uV (20mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V.

Register IIN_OC (0x11)

The IIN_OC register has a single data byte associated with it. This register sets the input over-current fault threshold.

ADDRESS	NAME	POR VALUE
0x11	IIN_OC	00h

Bit Assignment

7	6	5	4	3	2	1	0
IIN_OC7	IIN_OC6	IIN_OC5	IIN_OC4	IIN_OC3	IIN_OC2	IIN_OC1	IIN_OC0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_OC[7:0]	[7:0]	R/$\overline{w}$	0000 0000	IIN_OC[7:0] bits set the input over-current fault threshold. With internal sensing (VINRES=0), the LSB is 40mA. The ADC range is 0A to 8A, with code 0 = 0A. With external sensing (VINRES=1), the LSB is 200uV (20mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V.

Register IOUT_OC (0x12)

The IOUT_OC register has a single data byte associated with it. This register sets the output over-current fault threshold.

ADDRESS	NAME	POR VALUE
0x12	IOUT_OC	00h

Bit Assignment

7	6	5	4	3	2	1	0
IOUT_OC7	IOUT_OC6	IOUT_OC5	IOUT_OC4	IOUT_OC3	IOUT_OC2	IOUT_OC1	IOUT_OC0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IOUT_OC[7:0]	[7:0]	R/$\overline{w}$	0000 0000	IOUT_OC[7:0] bits set the output over-current fault threshold on the voltage measured across the current sense resistor (25mA with a 4mΩ sense resistor) in step down regulation mode. The LSB is 100uV. The programmable range is 0V to 24mV, with code 0 = 0V.

Register VIN_UV (0x13)

The VIN_UV register has a single data byte associated with it. This register sets the input under-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x13	VIN_UV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VIN_UV7	VIN_UV6	VIN_UV5	VIN_UV4	VIN_UV3	VIN_UV2	VIN_UV1	VIN_UV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VIN_UV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VIN_UV[7:0] bits set the input under-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register VIN_OV (0x14)

The VIN_OV register has a single data byte associated with it. This register sets the input over-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x14	VIN_OV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VIN_OV7	VIN_OV6	VIN_OV5	VIN_OV4	VIN_OV3	VIN_OV2	VIN_OV1	VIN_OV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VIN_OV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VIN_OV[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register EXT1_OV (0x15)

The EXT1_OV register has a single data byte associated with it. This register sets the EXT1 pin over-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x15	EXT1_OV	00h

Bit Assignment

7	6	5	4	3	2	1	0
EXT1_OV7	EXT1_OV6	EXT1_OV5	EXT1_OV4	EXT1_OV3	EXT1_OV2	EXT1_OV1	EXT1_OV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
EXT1_OV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	EXT1_OV[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register EXT2_OV (0x16)

The EXT2_OV register has a single data byte associated with it. This register sets the EXT2 pin over-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x16	EXT2_OV	00h

Bit Assignment

7	6	5	4	3	2	1	0
EXT2_OV7	EXT2_OV6	EXT2_OV5	EXT2_OV4	EXT2_OV3	EXT2_OV2	EXT2_OV1	EXT2_OV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
EXT2_OV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	EXT2_OV[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register VBATT_UV (0x17)

The VBATT_UV register has a single data byte associated with it. This register sets the VBATT under-voltage fault threshold. If VBATTP and VBATTN remote sense pins are not used, then the VBATT_UV function is disabled. Short VBATTP pin to VBATTN pin and connect these two pins to VOUT or GND when remote sense pins are not used.

ADDRESS	NAME	POR VALUE
0x17	VBATT_UV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VBATT_UV7	VBATT_UV6	VBATT_UV5	VBATT_UV4	VBATT_UV3	VBATT_UV2	VBATT_UV1	VBATT_UV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_UV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VBATT_UV[7:0] bits set the VBATT under-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VBATT_OV (0x18)

The VBATT_OV register has a single data byte associated with it. This register sets the VBATT over-voltage fault threshold. If VBATTP and VBATTN remote sense pins are not used, then the VBATT_OV function is disabled. Short VBATTP pin to VBATTN pin and connect these two pins to VOUT or GND when remote sense pins are not used.

ADDRESS	NAME	POR VALUE
0x18	VBATT_OV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VBATT_OV7	VBATT_OV6	VBATT_OV5	VBATT_OV4	VBATT_OV3	VBATT_OV2	VBATT_OV1	VBATT_OV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_OV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VBATT_OV[7:0] bits set the VBATT over-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VOUT_UV (0x19)

The VOUT_UV register has a single data byte associated with it. This register sets the VOUT under-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x19	VOUT_UV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_UV7	VOUT_UV6	VOUT_UV5	VOUT _UV4	VOUT_UV3	VOUT_UV2	VOUT_UV1	VOUT_UV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VOUT_UV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VOUT_UV[7:0] bits set the VOUT under-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VOUT _OV (0x1A)

The VOUT_OV register has a single data byte associated with it. This register sets the VOUT over-voltage fault threshold.

ADDRESS	NAME	POR VALUE
0x1A	VOUT_OV	00h

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_OV7	VOUT_OV6	VOUT_OV5	VOUT_OV4	VOUT_OV3	VOUT_OV2	VOUT_OV1	VOUT_OV0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VOUT_OV[7:0]	[7:0]	R/$\overline{w}$	0000 0000	VOUT_OV[7:0] bits set the VOUT over-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register TEMP_OT_WARN (0x1B)

The TEMP_OT_WARN register has a single data byte associated with it. This register sets the IC over-temperature warning threshold.

ADDRESS	NAME	POR VALUE
0x1B	TEMP_OT_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT_ WARN7	TEMP_OT_ WARN6	TEMP_OT_ WARN5	TEMP_OT_ WARN4	TEMP_OT_ WARN3	TEMP_OT_ WARN2	TEMP_OT_ WARN1	TEMP_OT_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	TEMP_OT_WARN[7:0] bits set the IC over-temperature fault threshold in 2's complement format. The LSB is 2°C. Please see decode table below for -40°C to 160°C settings. 1110 1100 = -40°C ..... 1111 0001 = -30°C ..... 1111 0110 = -20°C ..... 1111 1011 = -10°C ..... 0000 0000 = 0°C ..... 0000 0101 = 10°C ..... 0000 1010 = 20°C ..... 0000 1111 = 30°C ..... 0001 0100 = 40°C ..... 0001 1001 = 50°C ..... 0001 1110 = 60°C 0010 0011 = 70°C ..... 0010 1000 = 80°C ..... 0010 1101 = 90°C ..... 0011 0010 = 100°C ..... 0011 0111 = 110°C ..... 0011 1100 = 120°C ..... 0100 0001 = 130°C ..... 0100 0110 = 140°C ..... 0100 1011 = 150°C ..... 0101 0000 = 160°C

Register IIN_UC_WARN (0x1C)

The IIN_UC_WARN register has a single data byte associated with it. This register sets the input under-current warning threshold.

ADDRESS	NAME	POR VALUE
0x1C	IIN_UC_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
IIN_UC_ WARN7	IIN_UC_ WARN6	IIN_UC_ WARN5	IIN_UC_ WARN4	IIN_UC_ WARN3	IIN_UC_ WARN2	IIN_UC_ WARN1	IIN_UC_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_UC_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	IIN_UC_WARN[7:0] bits set the input under-current fault threshold. With internal sensing (VINRES=0), the LSB is 40mA. The ADC range is 0A to 8A, with code 0 = 0A. With external sensing (VINRES=1), the LSB is 200uV (20mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V.

Register IIN_OC_WARN (0x1D)

The IIN_OC_WARN register has a single data byte associated with it. This register sets the input over-current warning threshold.

ADDRESS	NAME	POR VALUE
0x1D	IIN_OC_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
IIN_OC_ WARN7	IIN_OC_ WARN6	IIN_OC_ WARN5	IIN_OC_ WARN4	IIN_OC_ WARN3	IIN_OC_ WARN2	IIN_OC_ WARN1	IIN_OC_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IIN_OC_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	IIN_OC_WARN[7:0] bits set the input over-current fault threshold. With internal sensing (VINRES=0), the LSB is 40mA. The ADC range is 0A to 8A, with code 0 = 0A. With external sensing (VINRES=1), the LSB is 200uV (20mA with a 10mΩ sense resistor). The ADC range is 0V to 40mV, with code 0 = 0V.

Register IOUT_OC_WARN (0x1E)

The IOUT_OC_WARN register has a single data byte associated with it. This register sets the output over-current warning threshold.

ADDRESS	NAME	POR VALUE
0x1E	IOUT_OC_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
IOUT_OC_ WARN7	IOUT_OC_ WARN6	IOUT_OC_ WARN5	IOUT_OC_ WARN4	IOUT_OC_ WARN3	IOUT_OC_ WARN2	IOUT_OC_ WARN1	IOUT_OC_ WARN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IOUT_OC_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	IOUT_OC_WARN[7:0] bits set the output over-current fault threshold on the voltage measured across the current sense resistor (25mA with a 4mΩ sense resistor) in step down regulation mode. The LSB is 100uV. The programmable range is 0V to 24mV, with code 0 = 0V.

Register VIN_UV_WARN (0x1F)

The VIN_UV_WARN register has a single data byte associated with it. This register sets the input under-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x1F	VIN_UV_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VIN_UV_WARN7	VIN_UV_WARN6	VIN_UV_WARN5	VIN_UV_WARN4	VIN_UV_WARN3	VIN_UV_WARN2	VIN_UV_WARN1	VIN_UV_WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VIN_UV_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VIN_UV_WARN[7:0] bits set the input under-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register VIN_OV_WARN (0x20)

The VIN_OV_WARN register has a single data byte associated with it. This register sets the input over-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x20	VIN_OV_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VIN_OV_WARN7	VIN_OV_WARN6	VIN_OV_WARN5	VIN_OV_WARN4	VIN_OV_WARN3	VIN_OV_WARN2	VIN_OV_WARN1	VIN_OV1_WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VIN_OV_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VIN_OV_WARN[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register EXT1_OV_WARN (0x21)

The EXT1_OV_WARN register has a single data byte associated with it. This register sets the EXT1 pin over-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x21	EXT1_OV_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
EXT1_OV_ WARN7	EXT1_OV_ WARN6	EXT1_OV_ WARN5	EXT1_OV_ WARN4	EXT1_OV_ WARN3	EXT1_OV_ WARN2	EXT1_OV_ WARN1	EXT1_OV_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
EXT1_OV_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	EXT1_OV_WARN[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register EXT2_OV_WARN (0x22)

The EXT2_OV_WARN register has a single data byte associated with it. This register sets the EXT2 pin over-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x22	EXT2_OV_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
EXT2_OV_ WARN7	EXT2_OV_ WARN6	EXT2_OV_ WARN5	EXT2_OV_ WARN4	EXT2_OV_ WARN3	EXT2_OV_ WARN2	EXT2_OV_ WARN1	EXT2_OV_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
EXT2_OV_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	EXT2_OV_WARN[7:0] bits set the input over-voltage fault threshold. The LSB is 80mV. The programmable range is 0V to 20V, with code 0 = 0V.

Register VBATT_UV_WARN (0x23)

The VBATT_UV_WARN register has a single data byte associated with it. This register sets the VBATT under-voltage warning threshold. If VBATTP and VBATTN remote sense pins are not used, then the VBATT_UV_WARN function is disabled. Short VBATTP pin to VBATTN pin and connect these two pins to VOUT or GND when remote sense pins are not used.

ADDRESS	NAME	POR VALUE
0x23	VBATT_UV_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VBATT_UV_WARN7	VBATT_UV_WARN6	VBATT_UV_WARN5	VBATT_UV_WARN4	VBATT_UV_WARN3	VBATT_UV_WARN2	VBATT_UV_WARN1	VBATT_UV_WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_UV_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VBATT_UV_WARN[7:0] bits set the VBATT under-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VBATT_OV_WARN (0x24)

The VBATT_OV_WARN register has a single data byte associated with it. This register sets the VBATT over-voltage warning threshold. If VBATTP and VBATTN remote sense pins are not used, then the VBATT_OV_WARN function is disabled. Short VBATTP pin to VBATTN pin and connect these two pins to VOUT or GND when remote sense pins are not used.

ADDRESS	NAME	POR VALUE
0x24	VBATT_OV_WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VBATT_OV_WARN7	VBATT_OV_WARN6	VBATT_OV_WARN5	VBATT_OV_WARN4	VBATT_OV_WARN3	VBATT_OV_WARN2	VBATT_OV_WARN1	VBATT_OV_WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VBATT_OV_WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VBATT_OV_WARN[7:0] bits set the VBATT over-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VOUT_UV_WARN (0x25)

The VOUT_UV_WARN register has a single data byte associated with it. This register sets the VOUT under-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x25	VOUT_UV_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_UV_ WARN7	VOUT_UV_ WARN6	VOUT_UV_ WARN5	VOUT_UV_ WARN4	VOUT_UV_ WARN3	VOUT_UV_ WARN2	VOUT_UV_ WARN1	VOUT_UV_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VOUT_UV_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VOUT_UV_WARN[7:0] bits set the VOUT under-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register VOUT_OV_WARN (0x26)

The VOUT_OV_WARN register has a single data byte associated with it. This register sets the VOUT over-voltage warning threshold.

ADDRESS	NAME	POR VALUE
0x26	VOUT_OV_ WARN	00h

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_OV_ WARN7	VOUT_OV_ WARN6	VOUT_OV_ WARN5	VOUT_OV_ WARN4	VOUT_OV_ WARN3	VOUT_OV_ WARN2	VOUT_OV_ WARN1	VOUT_OV_ WARN0

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
VOUT_OV_ WARN [7:0]	[7:0]	R/$\overline{w}$	0000 0000	VOUT_OV_WARN[7:0] bits set the VOUT over-voltage fault threshold. The LSB is 20mV. The programmable range is 0V to 5V, with code 0 = 0V.

Register FLT_SHDN1 (0x27)

The FLT_SHDN1 has a single data byte associated with it. This register sets which fault shutdown power train operation and disconnect EXT_FETs.

ADDRESS	NAME	POR VALUE
0x27	FLT_SHDN1	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT_ FLT_SHDN	IIN_UC_ FLT_SHDN	IIN_OC_ FLT_SHDN	IOUT_OC_ FLT_SHDN	VIN_UV_ FLT_SHDN	VIN_OV_ FLT_SHDN	EXT1_OV_ FLT_SHDN	EXT2_OV_ FLT_SHDN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_FLT _SHDN	[7]	R/$\overline{w}$	0	IC Over Temperature fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
IIN_UC_FLT _SHDN	[6]	R/$\overline{w}$	0	IIN undercurrent fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
IIN_OC_FLT _SHDN	[5]	R/$\overline{w}$	0	IIN overcurrent fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
IOUT_OC_FLT _SHDN	[4]	R/$\overline{w}$	0	IOUT overcurrent fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
VIN_UV_FLT _SHDN	[3]	R/$\overline{w}$	0	VIN undervoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
VIN_OV_FLT _SHDN	[2]	R/$\overline{w}$	0	VIN overvoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
EXT1_OV_FLT _SHDN	[1]	R/$\overline{w}$	0	EXT1 overvoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
EXT2_OV_FLT _SHDN	[0]	R/$\overline{w}$	0	EXT2 overvoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.

Register FLT_SHDN2 (0x28)

The FLT_SHDN2 has a single data byte associated with it. This register sets which fault shutdown power train operation and disconnect EXT_FETs.

ADDRESS	NAME	POR VALUE
0x28	FLT_SHDN2	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED				VBATT_UV_ FLT_SHDN	VBATT_OV_ FLT_SHDN	VOUT_UV_ FLT_SHDN	VOUT_OV_ FLT_SHDN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:4]	R	0000	Reserved bits
VBATT_UV_FLT _SHDN	[3]	R/$\overline{w}$	0	VBATT undervoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
VBATT_OV_FLT _SHDN	[2]	R/$\overline{w}$	0	VBATT overvoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
VOUT_UV_FLT _SHDN	[1]	R/$\overline{w}$	0	VOUT undervoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.
VOUT_OV_FLT _SHDN	[0]	R/$\overline{w}$	0	VOUT overvoltage fault shutdown 0= No shutdown. 1= Shutdown power train and disconnect EXT_FETs.

Register FLT_ACTIVE (0x29)

The FLT_ACTIVE has a single data byte associated with it. This register sets when the fault detection is active for IN_UC, IIN_OC, IOUT_OC, VIN_UV and VIN_OV faults.

ADDRESS	NAME	POR VALUE
0x29	FLT_ACTIVE	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED	IIN_UC_ FLT_ACT	IIN_OC_ FLT_ACT	IOUT_OC_ FLT_ACT	VIN_UV_ FLT_ACT	VIN_OV_ FLT_ACT	RESERVED	

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7]	R/$\overline{w}$	0	Reserved bit
IIN_UC_FLT _ACT	[6]	R/$\overline{w}$	0	IIN undercurrent fault shutdown active 0= Follow Table 7 “Fault and Warning Detection” table 1= Always Active
IIN_OC_FLT _ACT	[5]	R/$\overline{w}$	0	IIN overcurrent fault shutdown active 0= Follow Table 7 “Fault and Warning Detection” table 1= Always Active
IOUT_OC_FLT _ACT	[4]	R/$\overline{w}$	0	IOUT overcurrent fault shutdown active 0= Follow Table 7 “Fault and Warning Detection” table 1= Always Active
VIN_UV_FLT _ACT	[3]	R/$\overline{w}$	0	VIN undervoltage fault shutdown active 0= Follow Table 7 “Fault and Warning Detection” table 1= Always Active
VIN_OV_FLT _ACT	[2]	R/$\overline{w}$	0	VIN overvoltage fault shutdown active 0= Follow Table 7 “Fault and Warning Detection” table 1= Always Active
RESERVED	[1:0]	R/$\overline{w}$	00	Reserved bits

Register FLT_MASK1 (0x2A)

The FLT_MASK1 has a single data byte associated with it. This register sets which fault is masked from reporting.

ADDRESS	NAME	POR VALUE
0x2A	FLT_MASK1	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT_ FLT_MASK	IIN_UC_ FLT_MASK	IIN_OC_ FLT_MASK	IOUT_OC_ FLT_MASK	VIN_UV_ FLT_MASK	VIN_OV_ FLT_MASK	EXT1_OV_ FLT_MASK	EXT2_OV_ FLT_MASK

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_FLT _MASK	[7]	R/$\overline{w}$	0	IC Over Temperature fault mask 0= No mask. 1= TEMP_OT fault masked.
IIN_UC_FLT _ MASK	[6]	R/$\overline{w}$	0	IIN undercurrent fault mask 0= No mask. 1= IIN_OC fault masked.
IIN_OC_FLT _ MASK	[5]	R/$\overline{w}$	0	IIN overcurrent fault mask 0= No mask. 1= IIN_OC fault masked.
IOUT_OC_FLT _ MASK	[4]	R/$\overline{w}$	0	IOUT overcurrent fault mask 0= No mask. 1= IOUT_OC fault masked.
VIN_UV_FLT _ MASK	[3]	R/$\overline{w}$	0	VIN undervoltage fault mask 0= No mask. 1= VIN_UV fault masked.
VIN_OV_FLT _ MASK	[2]	R/$\overline{w}$	0	VIN overvoltage fault mask 0= No mask. 1= VIN_OV fault masked.
EXT1_OV_FLT _ MASK	[1]	R/$\overline{w}$	0	EXT1 overvoltage fault mask 0= No mask. 1= EXT1_OV fault masked.
EXT2_OV_FLT _ MASK	[0]	R/$\overline{w}$	0	EXT2 overvoltage fault mask 0= No mask. 1= EXT2_OV fault masked.

Register FLT_MASK2 (0x2B)

The FLT_MASK2 has a single data byte associated with it. This register sets which fault is masked from reporting.

ADDRESS	NAME	POR VALUE
0x2B	FLT_MASK2	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED				VBATT_UV _FLT_MASK	VBATT_OV _FLT_MASK	VOUT_UV _FLT_MASK	VOUT_OV _FLT_MASK

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:4]	R	0000	Reserved bits
VBATT_UV_FLT _ MASK	[3]	R/$\overline{w}$	0	VBATT undervoltage fault mask 0= No mask. 1= VBATT_UV fault masked.
VBATT_OV_FLT _ MASK	[2]	R/$\overline{w}$	0	VBATT overvoltage fault mask 0= No mask. 1= VBATT_OV fault masked.
VOUT_UV_FLT _ MASK	[1]	R/$\overline{w}$	0	VOUT undervoltage fault mask 0= No mask. 1= VOUT_UV fault masked.
VOUT_OV_FLT _ MASK	[0]	R/$\overline{w}$	0	VOUT overvoltage fault mask 0= No mask. 1= VOUT_OV fault masked.

Register WARN_MASK1 (0x2C)

The WARN_MASK1 has a single data byte associated with it. This register sets which warning is masked from reporting.

ADDRESS	NAME	POR VALUE
0x2C	WARN _MASK1	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT_ WARN_MASK	IIN_UC_ WARN_MASK	IIN_OC_ WARN_MASK	IOUT_OC_ WARN_MASK	VIN_UV_ WARN_MASK	VIN_OV_ WARN_MASK	EXT1_OV_ WARN _MASK	EXT2_OV_ WARN _MASK

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_ WARN_MASK	[7]	R/$\overline{w}$	0	IC Over Temperature warning mask 0= No mask. 1= TEMP_OT warning masked.
IIN_UC_ WARN_MASK	[6]	R/$\overline{w}$	0	IIN undercurrent warning mask 0= No mask. 1= IIN_UC warning masked.
IIN_OC_ WARN_MASK	[5]	R/$\overline{w}$	0	IIN overcurrent warning mask 0= No mask. 1= IIN_OC warning masked.
IOUT_OC_ WARN_MASK	[4]	R/$\overline{w}$	0	IOUT overcurrent warning mask 0= No mask. 1= IOUT_OC warning masked.
VIN_UV_ WARN_MASK	[3]	R/$\overline{w}$	0	VIN undervoltage warning mask 0= No mask. 1= VIN_UV warning masked.
VIN_OV_ WARN_MASK	[2]	R/$\overline{w}$	0	VIN overvoltage warning mask 0= No mask. 1= VIN_OV warning masked.
EXT1_OV_ WARN_MASK	[1]	R/$\overline{w}$	0	EXT1 overvoltage warning mask 0= No mask. 1= EXT1_OV warning masked.
EXT2_OV_ WARN_MASK	[0]	R/$\overline{w}$	0	EXT2 overvoltage warning mask 0= No mask. 1= EXT2_OV warning masked.

Register WARN_MASK2 (0x2D)

The WARN_MASK2 has a single data byte associated with it. This register sets which warning is masked from reporting.

ADDRESS	NAME	POR VALUE
0x2D	WARN _MASK2	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED				VBATT_UV WARN_MASK	VBATT_OV WARN _MASK	VOUT_UV WARN_MASK	VOUT_OV WARN _MASK

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:4]	R	0000	Reserved bits
VBATT_UV_ WARN_MASK	[3]	R/$\overline{w}$	0	VBATT undervoltage warning mask 0= No mask. 1= VBATT_UV warning masked.
VBATT_OV_ WARN_MASK	[2]	R/$\overline{w}$	0	VBATT overvoltage warning mask 0= No mask. 1= VBATT_OV warning masked.
VOUT_UV_ WARN_MASK	[1]	R/$\overline{w}$	0	VOUT undervoltage warning mask 0= No mask. 1= VOUT_UV warning masked.
VOUT_OV_ WARN_MASK	[0]	R/$\overline{w}$	0	VOUT overvoltage warning mask 0= No mask. 1= VOUT_OV warning masked.

Register DEGLITCH (0x2E)

The DEGLITCH has a single data byte associated with it. This register sets the fault and warning deglitch filter based on the ratio ADC sample time.

ADDRESS	NAME	POR VALUE
0x2E	DEGLITCH	01h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED			DEGLITCH[4:0]				

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:5]	R	000	Reserved Bits
DEGLITCH[4:0]	[4:0]	$R/\overline{W}$	0 0001	Program the deglitch filter from 1x to 31x of ADC sample time

Register WATCHDOG (0x2F)

The WATCHDOG has a single data byte associated with it. This register sets and enables watchdog function and reset bit to reset watchdog timer.

ADDRESS	NAME	POR VALUE
0x2F	WATCHDOG	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED			WD_ RESET	WD_I2C_ RESET	WD_ENABLE	WD_TIME[1:0]	

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:5]	R	000	Reserved Bits
WD_RESET	[4]	$R/\overline{W}$	0	Watchdog Reset bit (Self Clear bit) 0= No reset. 1= Reset watchdog timer.
WD_I2C_RESET	[3]	$R/\overline{W}$	0	Enable watchdog reset by I^2C communication 0= Disable watchdog reset by I^2C communication. 1= Enable watchdog reset by I^2C communication. Watchdog timer is reset when PE26100 acknowledges to an I^2C command.
WD_I2C_RESET	[2]	$R/\overline{W}$	0	Watchdog Enable 0= Watchdog disable 1= Watchdog enable
WD_TIME[1:0]	[1:0]	$R/\overline{W}$	00	Program watchdog timer duration 00 = 80 seconds 01 = 40 seconds 10 = 20 seconds 11 = 10 seconds

Register TEMP_LIM (0x30)

The TEMP_LIM has a single data byte associated with it. This register sets the system thermal throttle limit. When TEMP_LIM ≥ TEMP_SYS register value, the PE26100 charge current in step-down regulation mode remains unchanged. When TEMP_LIM < TEMP_SYS register value, the PE26100 charge current reduces by one LSB step in IOUT_MAX[7:0] in every ADC sample cycle until TEMP_LIM ≥ TEMP_SYS register value.

ADDRESS	NAME	POR VALUE
0x30	TEMP_LIM	FFh

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_LIM[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_LIM[7:0]	[7:0]	R/$\overline{w}$	0000 0000	System temperature limit for current throttling.

Register TEMP_SYS (0x31)

The TEMP_LIM has a single data byte associated with it. This register is for system AP to report system temperature.

ADDRESS	NAME	POR VALUE
0x31	TEMP_SYS	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_SYS[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_SYS[7:0]	[7:0]	R/$\overline{w}$	0000 0000	System temperature reporting.

Register FLT_STATUS1 (0x32)

The FLT_STATUS1 has a single data byte associated with it. This register reports triggered fault(s). These bits status remains until FLT_STATUS1 register is read.

ADDRESS	NAME	POR VALUE
0x32	FLT_STATUS1	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT_ FLT	IIN_OC_ FLT	IIN_OC_ FLT	IOUT_OC_ FLT	VIN_UV_ FLT	VIN_OV_ FLT	EXT1_OV_ FLT	EXT2_OV_ FLT

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_FLT	[7]	R	0	IC Over Temperature fault status 0= No fault. 1= TEMP_OT fault triggered.
IIN_UC_FLT	[6]	R	0	IIN undercurrent fault status 0= No fault. 1= IIN_UC fault triggered.
IIN_OC_FLT	[5]	R	0	IIN overcurrent fault status 0= No fault. 1= IIN_OC fault triggered.
IOUT_OC_FLT	[4]	R	0	IOUT overcurrent fault status 0= No fault. 1= IOUT_OC fault triggered.
VIN_UV_FLT	[3]	R	0	VIN undervoltage fault status 0= No fault. 1= VIN_UV fault triggered.
VIN_OV_FLT	[2]	R	0	VIN overvoltage fault status 0= No fault. 1= VIN_OV fault triggered.
EXT1_OV_FLT	[1]	R	0	EXT1 overvoltage fault status 0= No fault. 1= EXT1_OV fault triggered.
EXT2_OV_FLT	[0]	R	0	EXT2 overvoltage fault status 0= No fault. 1= EXT2_OV fault triggered.

Register FLT_STATUS2 (0x33)

The FLT_STATUS2 has a single data byte associated with it. This register reports triggered fault(s). These bits status remains until FLT_STATUS2 register is read.

ADDRESS	NAME	POR VALUE
0x33	FLT_STATUS2	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED				VBATT_UV_FLT	VBATT_OV_FLT	VOUT_UV_FLT	VOUT_OV_FLT

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:4]	R	0000	Reserved bits
VBATT_UV_FLT	[3]	R	0	VBATT undervoltage fault status 0= No fault. 1= VBATT_UV fault triggered.
VBATT_OV_FLT	[2]	R	0	VBATT overvoltage fault status 0= No fault. 1= VBATT_OV fault triggered.
VOUT_UV_FLT	[1]	R	0	VOUT undervoltage fault status 0= No fault. 1= VOUT_UV fault triggered.
VOUT_OV_FLT	[0]	R	0	VOUT overvoltage fault status 0= No fault. 1= VOUT_OV fault triggered.

Register WARN_STATUS1 (0x34)

The WARN_STATUS1 has a single data byte associated with it. This register reports triggered warning(s). These bits status remains until WARN_STATUS1 register is read.

ADDRESS	NAME	POR VALUE
0x34	WARN_STATUS1	00h

Bit Assignment

7	6	5	4	3	2	1	0
TEMP_OT _WARN	IIN_UC _WARN	IIN_OC _WARN	IOUT_OC _WARN	VIN_UV _WARN	VIN_OV _WARN	EXT1_OV _WARN	EXT2_OV _WARN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
TEMP_OT_ WARN	[7]	R	0	IC Over Temperature warning status 0= No fault. 1= TEMP_OT_WARN warning triggered.
IIN_UC_WARN	[6]	R	0	IIN undercurrent warning status 0= No fault. 1= IIN_UC_WARN fault triggered.
IIN_OC_WARN	[5]	R	0	IIN overcurrent warning status 0= No fault. 1= IIN_OC_WARN fault triggered.
IOUT_OC_ WARN	[4]	R	0	IOUT overcurrent warning status 0= No fault. 1= IOUT_OC_WARN warning triggered.
VIN_UV_WARN	[3]	R	0	VIN undervoltage warning status 0= No fault. 1= VIN_UV_WARN warning triggered.
VIN_OV_WARN	[2]	R	0	VIN overvoltage warning status 0= No fault. 1= VIN_OV_WARN warning triggered.
EXT1_OV_ WARN	[1]	R	0	EXT1 overvoltage warning status 0= No fault. 1= EXT1_OV_WARN warning triggered.
EXT2_OV_ WARN	[0]	R	0	EXT2 overvoltage warning status 0= No fault. 1= EXT2_OV_WARN warning triggered.

Register WARN_STATUS2 (0x35)

The WARN_STATUS2 has a single data byte associated with it. This register reports triggered warning(s). These bits status remains until WARN_STATUS2 register is read.

ADDRESS	NAME	POR VALUE
0x35	WARN_STATUS2	00h

Bit Assignment

7	6	5	4	3	2	1	0
RESERVED				VBATT_UV_WARN	VBATT_OV_WARN	VOUT_UV_WARN	VOUT_OV_WARN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
RESERVED	[7:4]	R	0000	Reserved bits
VBATT_UV_WARN	[3]	R	0	VBATT undervoltage warning status 0= No fault. 1= VBATT_UV_WARN warning triggered.
VBATT_OV_WARN	[2]	R	0	VBATT overvoltage warning status 0= No fault. 1= VBATT_OV_WARN warning triggered.
VOUT_UV_WARN	[1]	R	0	VOUT undervoltage warning status 0= No fault. 1= VOUT_UV_WARN warning triggered.
VOUT_OV_WARN	[0]	R	0	VOUT overvoltage warning status 0= No fault. 1= VOUT_OV_WARN warning triggered.

Register IC_STATUS1 (0x36)

The IC_STATUS1 register has a single data byte associated with it. This register reports the IC fault status. These bits status remains until IC_STATUS1 register is read.

ADDRESS	NAME	POR VALUE
0x36	IC_STATUS1	00h

Bit Assignment

7	6	5	4	3	2	1	0
IC_OTP	IC_ILIM	IC_OVP	REVERSE_ SSTIMOUT	WD_TIMEOUT	RESERVED	SYS_OTP	SHDN

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
IC_OTP	[7]	R	0	IC overtemperature (TSD) fault indicator bit 0= No fault. 1= IC overtemperature fault triggered.
IC_OCP	[6]	R	0	IC VOUT overcurrent (OCP) fault indicator bit 0= No fault. 1= IC overtemperature fault triggered.
IC_OVP	[5]	R	0	IC VIN over-voltage protection (OVP) fault indicator bit 0= No fault. 1= IC overtemperature fault triggered.
REVERSE_ SSTIMOUT	[4]	R	0	Reverse Step-Up Softstart Timeout 0= No fault. 1= Softstart timeout triggered.
WD_TIMEOUT	[3]	R	0	Watchdog timeout fault indicator bit 0= No fault. 1= Watchdog timeout fault triggered.
IC_ERROR	[2]	R	0	IC internal startup fault indicator bit 0= No fault. 1= IC startup fault triggered. Cycle IC with EN pin to re-attempt IC startup.
SYS_OTP	[1]	R	0	System overtemperature fault indicator bit 0= No fault. 1= TEMP_SYS register value > TEMP_LIM register value
SHDN	[0]	R	0	Fault Shutdown indicator bit 0= No shutdown 1= IC shutdown by fault event(s)

Register IC_STATUS2 (0x37)

The IC_STATUS2 register has a single data byte associated with it. This register reports the status of the IC operation. These bits status remains until operation or condition changes.

ADDRESS	NAME	POR VALUE
0x37	IC_STATUS2	01h

Bit Assignment

7	6	5	4	3	2	1	0
PGOOD	STEP_UP	CHRPUMP	STEP_DN	EXT_EN_IND	PT_EN_IND	REG_SET	POR

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
PGOOD	[7]	R	0	PGOOD indicator bit 0= No reset. 1= IC power train in normal operation
STEP_UP	[5]	R	0	Reverse Step-Up mode indicator bit 0= Not in reverse step-up mode 1= In reverse step-up mode
CHRPUMP	[4]	R	0	Divide-by-3 Charge Pump mode indicator bit 0= Not in divide-by-3 charge pump mode 1= In divide-by-3 charge pump mode
STEP_DOWN	[3]	R	0	Step-Down Regulation mode indicator bit 0= Not in Step-Down Regulation mode 1= In Step-Down Regulation mode
EXT_EN_IND	[3]	R	0	External FET Enable indicator bit 0= External FET disable 1= External FET enable by EXTG_EN bit
PT_EN_IND	[2]	R	0	Power Train Enable indicator bit 0= Power Train disable 1= Power Train enable by PT_EN bit and PT_EN pin
REG_SET	[1]	R	0	Register Set indicator bit 0= No register written 1= Any register(s) written beside Register 0x00
POR	[0]	R	1	Power On Reset indicator bit 0 = Not in POR 1 = IC POR by EN pin, IC_EN bit, VOUT UVLO, or VDDIO UVLO

Application Schematic

Figure 17. Detailed Application Schematic

Application Circuit Part List for Single IC Solution

COMPONENT	QUANTITY	VALUE	PART SIZE	MANUFACTURER'S PART NUMBER
L1	1	470 nH	2.5 mm x 2.0 mm x 1.0 mm	Cyntec HTEL25201T-R47MSDR-01
L2	1	14 nH	2.5 mm x 2.0 mm x 1.0 mm	Murata
CA Fly Capacitors	1	22uF		Murata GRM219R61C226ME15
CB Fly Capacitors	2	22uF		Murata GRM219R61C226ME15
VIN Capacitors	3	10uF		Murata GRM188R61E106MA73
VOUT Capacitors	2	22uF/10V	0603	Murata GRM188R61A226M
Boot Capacitor	5		0201	Generic
COMP Capacitor	1		0201	Generic
COMP Resistor	1		0210	Generic
Output Current Sense Resistor	1			Generic
Input Disconnect FET for USB	1			SSM10N961L
Input Disconnect FET for WLC	1			SSM10N961L

Table 9. Application Circuit Part List for Single IC Solution

Application Circuit Part List for Dual IC Solution

COMPONENT	QUANTITY	VALUE	PART SIZE	MANUFACTURER'S PART NUMBER
L11, L21	2	470 nH	2.5 mm x 2.0 mm x 1.0 mm	Cyntec HTEL25201T-R47MSDR-01
L12, L22	2	14 nH	2.5 mm x 2.0 mm x 1.0 mm	Murata
CA1, CA2 Fly Capacitors	2	22uF		Murata GRM219R61C226ME15
CB1, CB2 Fly Capacitors	4	22uF		Murata GRM219R61C226ME15
VIN Capacitors	6	10uF		Murata GRM188R61E106MA73
VOUT Capacitors	4	22uF/10V	0603	Murata GRM188R61A226M
Boot Capacitors	10		0201	Generic
COMP Capacitor	1		0201	Generic
COMP Resistor	1		0210	Generic
Output Current Sense Resistor	2			Generic
Input Disconnect FET for USB	1			SSM10N961L
Input Disconnect FET for WLC	1			SSM10N961L

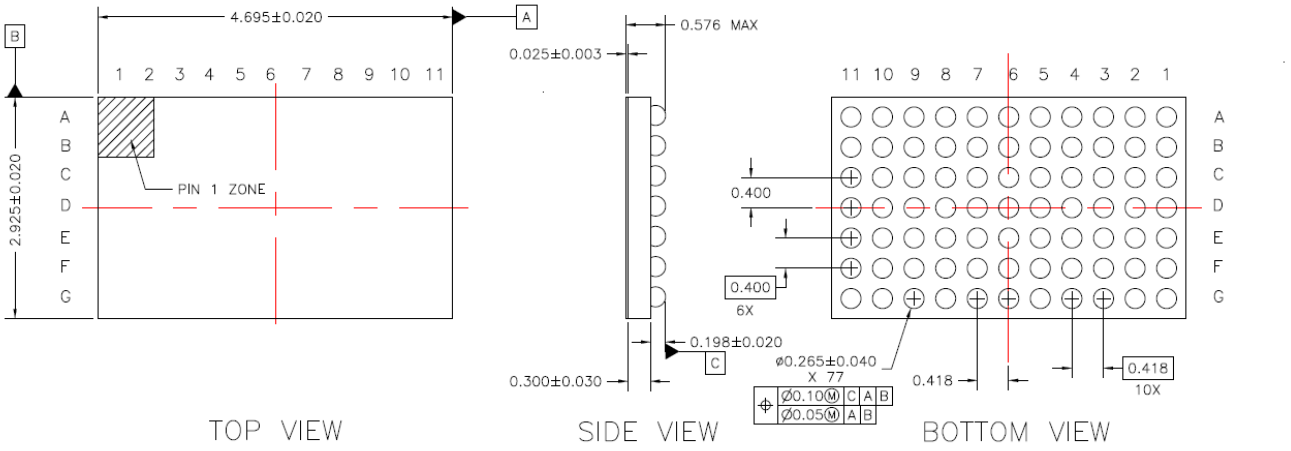
Table 9. Application Circuit Part List for Dual IC Solution

Component Selection

Users of the PE26100 should adhere closely to the parts selected for the Application Circuit Part List. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact Murata for guidance.

Layout Example

Package Mechanical Details



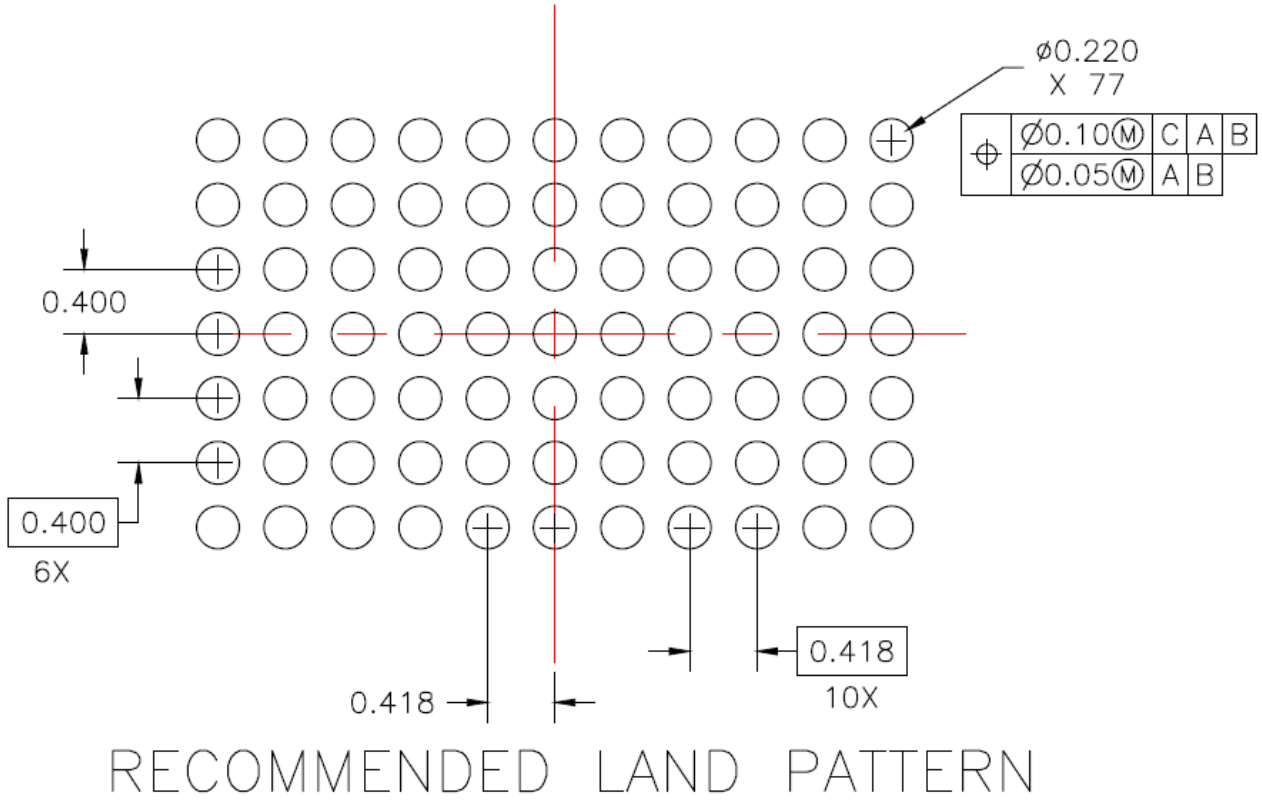
THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL	ANGULAR
X.X ±0.1	±1°
X.XX ±0.05	
X.XXX ±0.030	

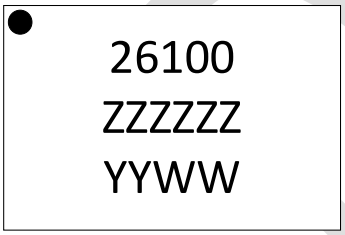
INTERPRET DIM AND TOL PER ASME Y14.5 – 1994

Guidelines for PCB Land Design



RECOMMENDED LAND PATTERN

Top Marking Information



● = Pin1 Indicator

26100 = Part Number

ZZZZZZ = Lot Number

YY = Last two digits of assembly year (2024 = 24)

WW = Assembly Work Week (01, 02, 03, …, 52)

Tape and Reel Information

Ordering Information

TA	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM ORDER QUANTITY
-40....+85°C	WLCSP	PE26100A-R	xx	Large tape-and-reel	5,000
		PE26100A-V (Not for Production Use)		Small tape-and-reel	250
		PE26100A-G (Not for Production Use)		Sample waffle tray	

Table 10: Ordering Information

Document Categories

Advance Information
The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification
The datasheet contains preliminary data. Additional data may be added at a later date. Murata reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification
The datasheet contains final data. In the event Murata decides to change the specifications, Murata will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief
The datasheet contains summary product information.

Sales Contact
For additional information, contact Sales at **https://www.murata.com/contactform.**

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Copyright and Trademark

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Refer to: https://power.murata.com/en/requirements

Edit History

Ver	Date	Edits
1.73	May 24th, 2023	1. Updated Reverse Step-up from 10V to 16V. 2. Updated EXT1/EXT2/EXTG1/EXTG2 to GND abs max to 26V from 28V. 3. Changed PGOOD pin to VDDIO pin. VDDIO pin for I2C reference. 4. Changed VIN_ADC to 20mV LSB. 5. Changed IIN_ADC to 200uV LSB (20mA with 10mOhm CSR). 6. Updated VIN_OV, VIN_UV to 80mV LSB. 7. Changed VOUT_ADC from 20mV to 7.5mV LSB. 8. Updated VOUT_OV, VOU_UV, VSET to 30mV LSB. 9. Added EXT1_OV and EXT2_UV with 80mV LSB. Add EXT1/2_OV_FLT bits. 10. Added FLT_SHDN register to trigger power train shutdown during FLT. 11. Removed WARNING registers. 12. Added V_EXTG bit to select 5V or 9V gate voltage. 13. Removed Standby current spec. 14. Changed Shutdown current spec from to 10uA typ, 30uA max. 15. Keeping EN pin as IC enable pin (or RESETb pin in Google. Changed RESET pin to PT_EN pin for hardware enable pin. 16. Added RESET bit to MODE register (Reg 0) 17. Updated VIN Regulation mode min voltage from '4.5V' to 'VOUT+0.2V'. 18. Added Fig.8 PE26100 Charging Function Diagram 19. Added Fig.9 PE26100 Initialization and Operation Flow Chart 20. Added IC_ENABLE register to enable IC and reset IC. 21. Added output current sense register on L1 for MLC regulation current sense and update IOUT setting and ADC to reflect voltage across resistor. Update pinout to add IOUT current sense resistor pins.
1.74	June 5th, 2023	22. Updated Register Map, add additional FAULT/WARNING and WATCHDOG. 23. Added other datasheet sections and detail description.
1.75	June 12th, 2023	24. Added SYNCH pin for parallel operation. 25. Updated pinout. 26. Updated VEXT_G selection to have 5V as default setting. 27. Added TEMP_LIM, TEMP_SYS register to enable charge current throttle at system over-temp. 28. Added control bits to enable both FETs.

1.8		29. Updated FREQUENCY register settings. 30. Added dual IC operation power train sequence (turn on slave IC before the master IC, master IC controls the external FETs). 31. Updated Reverse step up range from 5V to 16V to 4.8V to 16V. 32. Updated 26V abs max on EXT1, EXT2, EXTG1 and EXTG2 to 28V. 33. Updated IC OVP from 17V to 19.5V. 34. Updated VIN max from 16V to 18V. 35. Corrected IOUT ADC range and current sense resistor typos. Recommended current sense value is 4mOhm and ADC range is 0V to 24mV.
1.9	Aug 2nd, 2023	36. Updated Pinout, Pin Description Table, Typical Application Diagrams to incorporate the addition of internal input current sense resistor. 37. Swapped pin location for VDDIO, ADDR and SCL pins. 38. Added register bit VINRES to enable/disable internal input current sense to MODE register (0x01) 39. Removed CP_FSW register bits and changed ML_FSW to FSW. Moved DITHER bit to bit 3 of FREQUENCY register. 40. Removed STEP_UP/DOWN bit from VOUT_REG register. Changed VOUT_REG and VBATT_REG from 7bit to 8bit. Changed LSB from 15mV to 10mV, and updated programmable range and offset. 41. Changed VBATT_ADC from 7.5mV LSB to 5mV LSB. 42. Changed VBATT_OV, VBATT_UV, VOUT_OV, and VOUT_UV in FAULT and WARNING registers LSB from 30mV to 20mV. 43. Updated slave address settings: a. Set upper four bit of slave address to “D” or “1101”. b. Changed ADDR=floating from ‘110’ to ‘111’ 44. Changed TEMP related registers to 2’s complement format with LSB=5C and range from -160C to 160C. 45. Changed indicator bit name REVERSE to STEP_UP, CP to CHRPUMP, CC to STEP_DN. Corrected description for STEP_DN bit.
1.91	Aug 8th,2023	46. Update EC table VBATT ADC LSB size from 7.5mV to 5mV. 47. Add VINRES, IOSP and IOSN to Abs Max table. 48. Added POD and recommended land pattern.
1.92	Aug 9th, 2023	49. Change pin description for INSP and INSN input current sense pins, with input sense R, leave pins floating. 50. Figure 4 and 6 changed to float INSP and INSN pins when no external input sense R is used.
1.93		51. Fixed typos in datasheet. 52. Updated TEMP ADC, FAULT and WARNIGN to 8bit 2’s complement value.

		53. Added spec for VBATTP pin leakage current to EC table. 54. Added abs max for SYNC_SEL, SYNC, SYNCH, COMP to GND. 55. Added specs for VDDIO UVLO and supply current to EC table. 56. Added "connect to VOUT or GND when remote sense is not used" for VBATTP and VBATTN pin description and VBATT_UV, VBATT_OV, VBATT_UV_WARN and VBATT_OV_WARN register description sections. 57. Added spec for Internal IIN Current Sense Spec to EC table and update description to IIN related registers. 58. Fixed IIN and IOUT related registers that still have 7bit to 8bit resolution in register map and description. 59. Added MLC_3L/4L and CP_2x/3x for opinion to select MLC in 3L or 4L and CP in DIV2 or DIV3 operation. 60. Added IIN_ADC_LB to register 0x08 61. Added VIN OVP at 12.5V for 3L MLC operation. 62. Added VIN range spes for MLC_3L and CP_2x operations. 63. Added Top Marking Information
1.94		64. Updated Apps diagram on VINRES and IISN pins in internal and external input current sense. 65. Added Block Diagram. 66. Updated pin description on VINRES and IISN pins. 67. Added bit description for SYS_OTP fault bit. 68. Added IC_ERROR fault bit and description. 69. Updated FSW[2:0] bit settings. 70. Removed CP_2x/3x bit and combine function into MLC_3L/4L bit. 71. Added VBATTN pin leakage current to electrical specification.
1.95		72. Updated IISN connection in internal current sense configuration. Leave IISN pin floating. 73. Updated VIN undervoltage spec and fault detection. Set VIN undervoltage protection trigger when VIN < VOUT-1.2V typ. 74. Update TEMP_ADC, TEMP_OT and TEMP_OT_WARN from 5℃ LSB to 2℃ LSB. 75. Swapped PT_EN and EXTG_EN order in reverse boost mode.
1.96		76. Added in detail to specific IOUT related setting is for step down regulation mode.