PE23108

Document Category: Product Specification

High Efficiency LED Backlight Driver

Product Description

The **PE23108** is an ultra-high efficiency DC-DC converter solution with integrated programmable current sinks that drive up to eight strings of LEDs. The PE23108 integrates all MOSFETs and their control and driver circuitry. With the proprietary architecture, the PE23108 provides the highest efficiency (up to 96%) possible in a compact 3.445 mm x 2.095 mm WLCSP30 package. The unique two-stage architecture enables a small and low-profile solution size aligned to the needs of the latest mobile products.

Features

- Synchronous DC-DC converter with integrated FETs
- 2- and 3-cell Li-ion battery input voltage for LED boost: 4.5V to 15V
- 2.7V to 5.5V IC input voltage
- Proprietary architecture for ultra-high LED efficiency, up to 96%
- Integrated output disconnect switch
- Up to 42V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- Up to 12-bit dimming resolution with an additional 3-bit dithering
- Supports linear/logarithmic analog and PWM dimming for maximum flexibility and resolution
- Phase-shifted PWM dimming among active strings to minimize audible noise
- LED brightness ramp up/down control with programmable ramp rate and linear/ logarithmic ramp profiles
- 1 MHz I^2C 6.0-compatible serial interface to program the brightness
- Extensive programming capability with non-volatile memory for storing user register settings
- Eight independently enabled current sinks, up to 33 mA per current sink
- External PWM input for fine dimming resolution
- 0.5% current matching at 20 mA per current sink
- Wide range of input and output voltages with 2x charge pump ratio
- Selectable boost switching frequency from 179 kHz to 1.43 MHz
- Extensive fault protection including boost over-current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Typical Applications

Typical applications for 2- and 3-cell platforms include:

- 8”-17” FHD/UHD+ LCD backlight panels
- Ultrabooks / ultraportables / notebooks
- 2-in-1 / convertible / detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

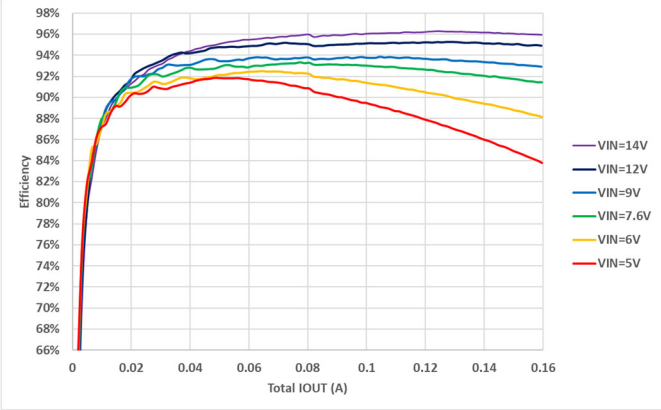


Figure 1. Typical Boost Efficiency – 8p12s, 20 mA, 715 kHz

Simplified Application

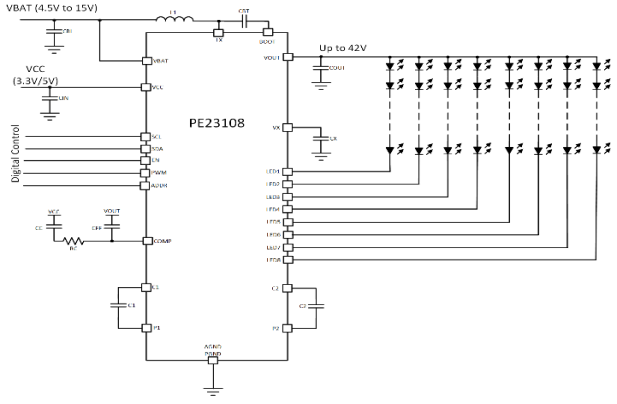


Figure 2. Typical Application Circuit

Table of Contents

Absolute Maximum Ratings[1,2]

PARAMETER	MIN	MAX	UNITS
VBAT to AGND	-0.3	18	V
VCC, PWM, COMP, EN, SCL, SDA, ADDR to AGND	-0.3	6	V
VOUT, C1, C2 to AGND	-0.3	45	V
LEDx to AGND	-0.3	40	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1, P2, to PGND	-0.3	22	V
VX to LX, P1, P2	-0.3	22	V
BOOT to VBAT	-18.3	28	V
BOOT to LX	-0.3	6	V
C1, C2 to VX	-0.3	22	V
Storage Temperature	-65	150	°C

PARAMETER	VALUE
Junction Temperature	150°C
Bump or Lead Temperature (soldering, reflow)	+260°C
ESD Tolerance, PE23108 HBM[3]	1kV
ESD Tolerance, CDM[4]	1kV

Notes:

1. *The application of any stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, and exposure at any of these ratings for extended periods may reduce the reliability of the device.*
2. *The above "Absolute Maximum Ratings" are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.*
3. *Human body model, per the JEDEC standard JS-001-2017.*
4. *Field induced charge device model, per the JEDEC standard JESD22-C101.*

Table 1. Absolute Maximum Ratings

Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS
VBAT Input Voltage Range, relative to AGND or PGND(*)	4.5	15	V
VCC Voltage Range, relative to AGND	2.7	5.5	V
VOUT Output Voltage Range, relative to AGND PGND(*)	18	42	V
VX Boost Output Voltage Range, relative to AGND or PGND	1.2*VBAT	21	V
Junction Temperature Range, T_J	-40	125	°C
*Notes *: VBAT and VOUT ranges must meet valid operating regions in continuous conduction mode (CCM): (*$VBAT \leq \frac{VOUT}{2.15}$*)*			

Table 2. Recommended Operating Conditions

Package Thermal Characteristics (1,2)

DEVICE	PARAMETER	MAX	UNITS
PE23108	Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	46	°C/W
	Junction-to-board thermal characterization (Ψ_{JB})	11	°C/W
	Junction-to-top case thermal characterization (Ψ_{JC})	8	°C/W

Notes:

1. *Package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.*
2. *Junction-to-ambient thermal resistance (ΘJA) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.*

Table 3. Package Thermal Characteristics

Electrical Characteristics[1]

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
IC Input Voltage Range	V_{VCC}		2.7		5.5	V
Input Voltage Range	V_{VBAT}		4.5		15	V
VCC Under-voltage Lockout (UVLO) Threshold High	$V_{VCC-UVLO\_H}$	VVCC rising			2.6	V
VBAT Under-voltage Lockout (UVLO) Threshold High	$V_{VBAT-UVLO\_H}$	VVBAT rising			4.4	V
Under-voltage Lockout (UVLO) Hysteresis	V_{UVLO_HYST}	VBAT		65		mV
		VCC		50		mV
VCC Shutdown Supply Current	I_{VCC_SD}	IVCC with VEN=0V			1	µA
VBAT Shutdown Supply Current	I_{VBAT_SD}	IVBAT with VEN=0V			1	
VCC Quiescent Current	I_{VCC}	EN=1.8V, ILED=100 µA, f_{SW_BOOST}=715 kHz		2		mA
Thermal Shutdown Threshold[3]	T_{TSD}			150		°C
Thermal Shutdown Hysteresis[3]	T_{TSD_HYST}			20		°C
Soft Start Time-Out Duration				10		ms
STEP-UP CONVERTER						
Output Voltage Range[4]	V_{OUT}		18		42	V
Maximum Output Power			6			Watts

Electrical Characteristics (cont.)[1]

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Switching Frequency Range	f_{SW_BOOST}	FSW_BOOST [3:0]	0100		715		kHz
			1010		286		
Boost Switching Frequency Accuracy			f_{SW_BOOST} = 715 kHz	-4		+4	%
Boost Minimum Off-Time	$T_{OFF\_BOOST\_MIN}$				170		ns
Boost Minimum On-Time	$T_{ON\_BOOST\_MIN}$				60		ns
Boost Low-Side Switch Current Limit, Cycle-by-Cycle	I_{BOOST_LIMIT}	I_{LX} rising	BOOST_ILIM [1:0]=00		2.0		A
			BOOST_ILIM [1:0]=01		1.0		
			BOOST_ILIM [1:0]=10		2.5		
			BOOST_ILIM[1:0]=11		3.0		
Output Over-Current Threshold	I_{OUT_OC}	I_{OUT} rising		250			mA
Output Over-voltage Threshold	V_{OUT_OVP}	$OV_{P\_TH[3:0]}$	0010		43.75		V
			0011		41.875		
			…				
			1111		19.375		
Output Over-voltage Hysteresis	$V_{OUT\_OVP\_HYST}$				0.35		V
Accuracy of Output Over-voltage Protection Threshold				-5		5	%

Electrical Characteristics (cont.)[1]

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LED CURRENT SINKS (LED1 to LED8)							
LED Current Full-Scale Output Range	ILED_MAX	I^2C Register Setting MAX_I[4:0]	MAX_I [4:0]=00000		2		mA
			MAX_I [4:0]=00001		3		
			…		…		
			MAX_I [4:0]=11111		33		
Minimum Sink Current LED1-8	ILEDx_MIN	IMAX programmed to 20 mA, linear mapping			4.88		µA
Leakage Current	ILED_LEAKAGE	LED1,..,8=0, VOUT = 36V				1	µA
LED Current Matching[5]	ILED_MATCHING	IMAX programmed to 20 mA ILEDX programmed to Full Scale		-1		1	%
LED Current Matching[5]	ILED_MATCHING	IMAX programmed to 20 mA ILEDX programmed to 2% Brightness Level		-2.6		2.6	%
LED Current Accuracy[6]	ILED_ACCURACY	IMAX programmed to 20 mA ILEDX programmed to Full Scale		-2		2	%
LED Regulation Voltage	VLED_REGULATION	ILEDX programmed to 20 mA			320		mV
LED Shorted String Detection Threshold		VLEDX falling	LED_SHORT_VTH[1:0]=00		4.35		V
			LED_SHORT_VTH[1:0]=01		4.85		
			LED_SHORT_VTH[1:0]=10		5.25		
			LED_SHORT_VTH[1:0]=11		5.75		
Current Ripple		ILED programmed to 20 mA DC LED current output			1		%

Electrical Characteristics (cont.)[1]

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL PWM DIMMING							
Transition Point Between Internal PWM and Analog Dimming		DIM_MODE=0			0%		
		DIM_MODE=1	PWM_IX[1:0]=00		12.5%		
			PWM_IX[1:0]=01		25% (Default)		
			PWM_IX[1:0]=10		50%		
			PWM_IX[1:0]=11		100%		
LED PWM Output Frequency	f_{LEDX}	PWM_DIM_FREQ[2:0]		2.79		22.49	kHz
LED Current Sink Minimum Output Pulse Width					350		ns
LOGIC INTERFACE							
EN Logic Input High Voltage	V_{IH_EN}			1.2			V
EN Logic Input Low Voltage	V_{IL_EN}					0.4	V
PWM Logic Input High Voltage	V_{IH_PWM}			0.9			V
PWM Logic Input Low Voltage	V_{IL_PWM}					0.5	V
Logic Input Current	$I_{PWM, IEN}$			-1.0		1.0	µA
ADDR Input Resistance	I_{ADDR_R}				100		kΩ
ADDR Input High Voltage	V_{IH_ADDR}			VCC-0.4V			V
ADDR Input Low Voltage	V_{IL_ADDR}					0.4	V
PWM Pin Input Frequency for Internal PWM mode	F_{IPWM}			0.1		40	kHz
PWM Pin Minimum Input High Pulse					350		ns
PWM Pin Minimum Input Low Pulse					350		ns
I²C SERIAL INTERFACE (SCL, SDA)							
SDA, SCL Input High Voltage	V_{IH}			1.26		3.6	V
SDA, SCL Input Low Voltage	V_{IL}					0.99	V
SDA, SCL Input Hysteresis	VHYS				0.1		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA, SCL Input Current	ISCL, ISDA				1	µA
SDA Output Low Level	VOL	I_{SDA} = 20 mA			0.4	V
I^2C Interface Initial Wait Time		Initial wait time from EN logic high to 1st I^2C command accepted	1			ms
SDA, SCL Pin Capacitance	CI/O				10	pF

Electrical Characteristics (cont.)1

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD, FAST MODE AND FAST MODE PLUS					
Serial Clock Frequency	F_{SCL}	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
Clock Low Period	t_{LOW}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Clock High Period	t_{HIGH}	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
BUS Free Time between a STOP and a START condition	t_{BUF}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Hold Time for a Repeated START condition	$t_{HD:STA}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Setup Time of STOP condition	$t_{SU:STO}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Data Setup Time	$t_{SU:DAT}$	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
Data Hold Time	t_{HD_DAT}	Standard mode	0		µs
		Fast mode	0		ns
		Fast mode plus	0		ns
Rise Time of SCL Signal	t_{RCL}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns

Electrical Characteristics (cont.)[1]

VBAT = 12V, VCC = 3.3V, VAGND = VPGND = 0V, VEN = 1.8V, TA = TJ = -40°C to +85°C, unless otherwise noted. Typical values are at TA = TJ = 25°C with 8p12s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Fall Time of SCL Signal	t_{FCL}	Standard mode		300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns
Fall Time of SDA Signal2	t_{FDA}	Standard mode		300	ns
		Fast mode	20	300	ns
		Fast mode plus	20	120	ns
Data Valid Time	t_{VD}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns
Data Valid Acknowledge Time	t_{VDA}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns
Capacitive Load for SDA and SCL	C_{BUS}	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF
MTP Non-Volatile Memory Write Cycle Time				50	ms

Notes:

1. *Min/max specifications are 100% production tested at TA=TJ=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.*
2. *Guaranteed by design.*
3. *Thermal shutdown is not production tested.*
4. *VBAT and VOUT ranges must meet valid operating regions must meet valid operating regions when in CCM operation:* $(VBAT \leq \frac{VOUT}{2.15})$
5. *The sink current matching is defined/tested as (ILED_MAX-ILED_MIN)/ILED_AVG.*
6. *The LED current accuracy is defined/tested as: 100*(ILED_AVG-ILED_Target)/ILED_AVG.*

Table 4. Electrical Characteristics

Pin Configuration

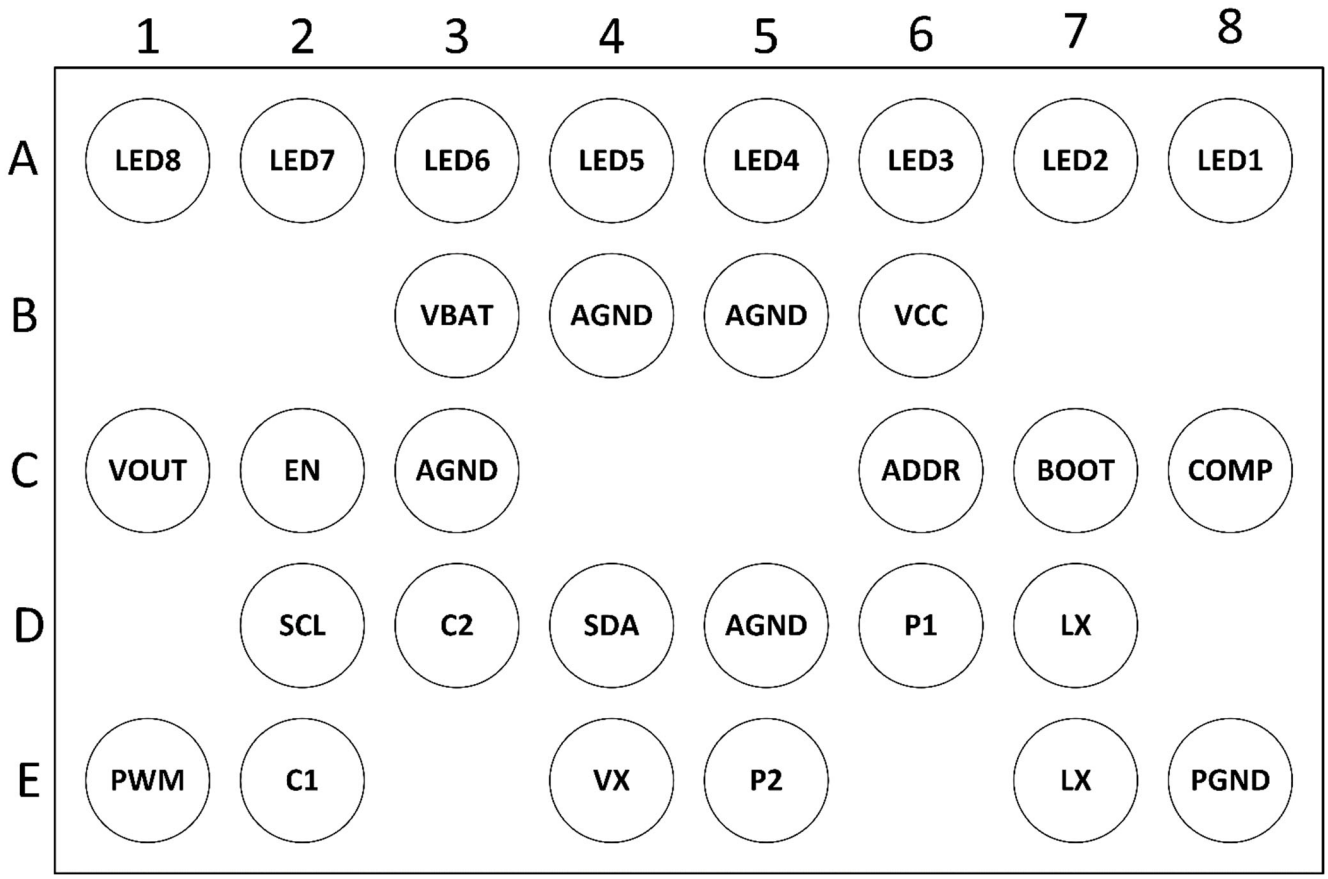


Figure 3. PE23108 30-Pin WLCSP Top View

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
A1	LED8	Individual LED current sink. Connect to the low side of individual LED strings.
A2	LED7	Individual LED current sink. Connect to the low side of individual LED strings.
A3	LED6	Individual LED current sink. Connect to the low side of individual LED strings.
A4	LED5	Individual LED current sink. Connect to the low side of individual LED strings.
A5	LED4	Individual LED current sink. Connect to the low side of individual LED strings.
A6	LED3	Individual LED current sink. Connect to the low side of individual LED strings.
A7	LED2	Individual LED current sink. Connect to the low side of individual LED strings.
A8	LED1	Individual LED current sink. Connect to the low side of individual LED strings.
B3	VBAT	LED boost input voltage, battery power supply pin.
B4, B5, C3, D5	AGND	Analog and LED current sink ground, star ground to system ground plane.
B6	VCC	IC input voltage. Connect to a 3.3V or 5V supply.
C1	VOUT	Power converter output voltage. Connect to the high side of all LED strings. Connect externally to 4x 2.2 µF 0603 capacitor. See Component Selection for capacitor selection guideline.
C2	EN	Enable input.
C6	ADDR	Sets lower three bits of the I^2C slave address. Tie to AGND pin for '000'. Leave floating for '010'. Tie to VCC pin for '101'.
C7	BOOT	Bootstrap capacitor for the boost stage high side FET. Connect a 2.2 nF, 10V or higher capacitor from BOOT to LX.
C8	COMP	External compensation pin. See Switching Converter Compensation for detail.
D2	SCL	Serial clock for I^2C bus.
D3	C2	Charge pump fly capacitor positive node. Connect 2x4.7 µF 0603 capacitor from C2 to P2.
D4	SDA	Serial data for I^2C bus.
D6	P1	Charge pump fly capacitor phase node. Connect 2x4.7 µF 0603 capacitor from P1 to C1.
D7,E7	LX	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage VBAT. See Component Selection for inductor selection guideline.
E1	PWM	PWM dimming input for brightness control. Must be connected to VCC pin if not used.
E2	C1	Charge pump fly capacitor positive node. Connect 2x4.7 µF 0603 capacitor from C1 to P1. See Component Selection for capacitor selection guideline.
E4	VX	Charge pump input node, internally driven by the output of the boost converter. Connect a 2.2 µF 0402 capacitor between this pin and PGND. See Component Selection for capacitor selection guideline.
E5	P2	Charge pump fly capacitor phase node. Connect 2x4.7 µF 0603 capacitor from P2 to C2. See Component Selection for capacitor selection guideline.
E8	PGND	Power ground must tie externally to system ground plane. High current path.

Table 5. PE23108 30-pin WLCSP Pin Descriptions

Operating Voltage Range and Charge Pump Ratio

The PE23108 uses a 2X charge-pump to improve efficiency. The charge pump architecture requires the battery input voltage to be less than the output voltage divided by 2.15x when boost DC-DC is operating in continuous conduction mode (CCM) condition:

$$VBAT \leq \frac{VOUT}{2.15}$$

Functional Block Diagram

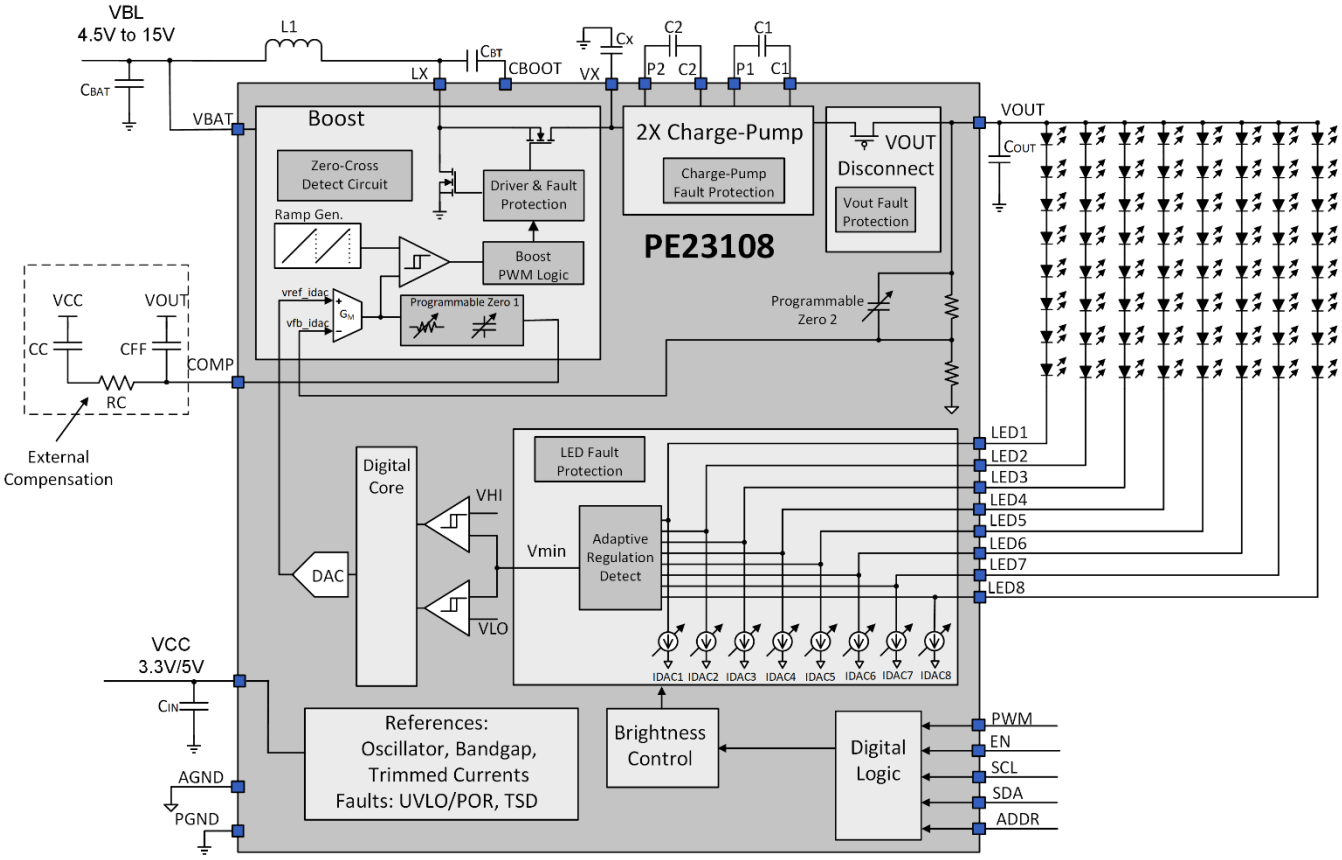


Figure 4. Block Diagram

Application Circuit

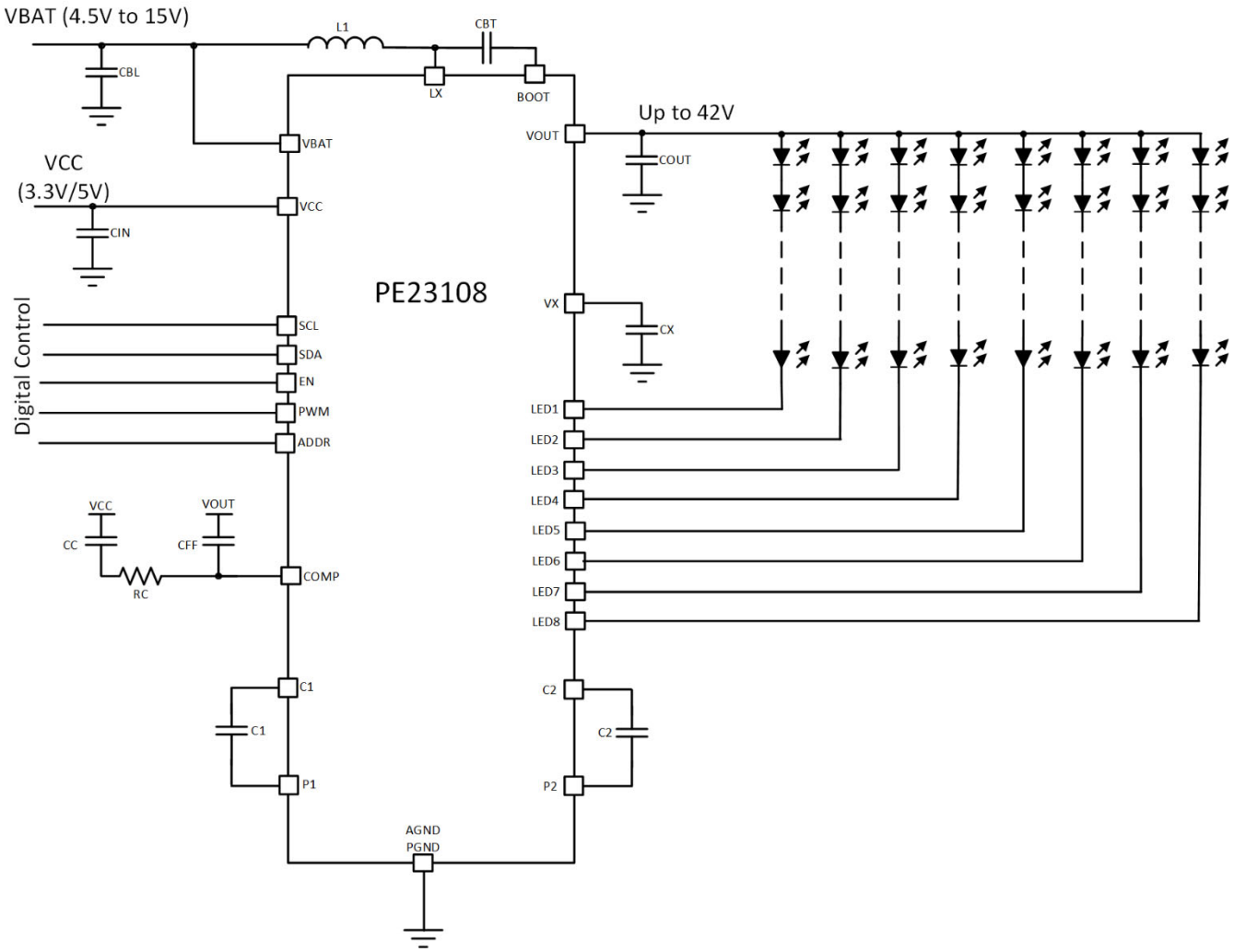


Figure 5. Application Schematic for I²C interface

Note: Star ground PGND and AGND on a system ground plane.

Typical Characteristics

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10 µH, Cout=4x2.µF, IMAX=20 mA, LED VF=2.8V at 20 mA (typ.) analog dimming.

Efficiency – 286 kHz Boost Switching Frequency

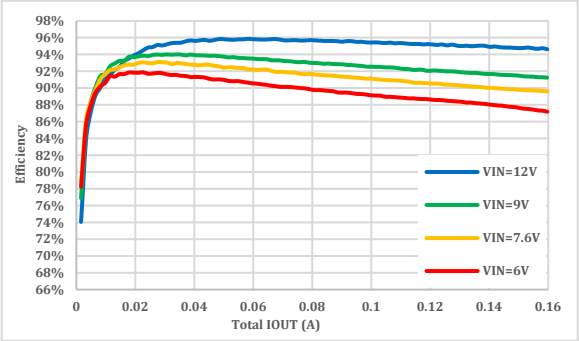


Figure 6. 8P10S Boost Efficiency[1], 10 µH Inductor

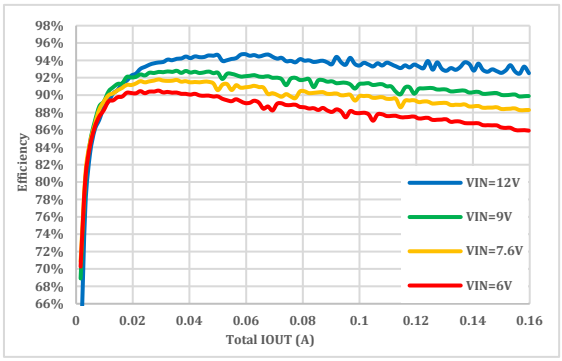


Figure 7. 8P10S System Efficiency[2], 10 µH Inductor

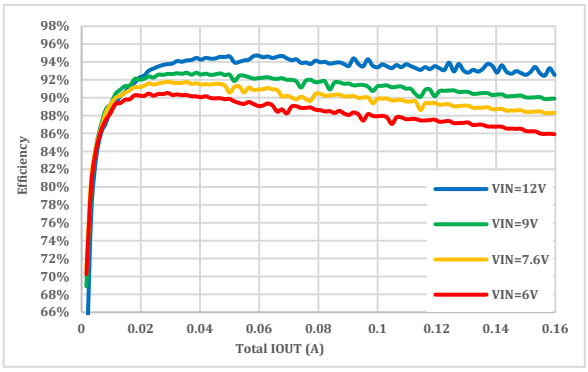


Figure 8. 8P12S Boost Efficiency[1], 10 µH Inductor

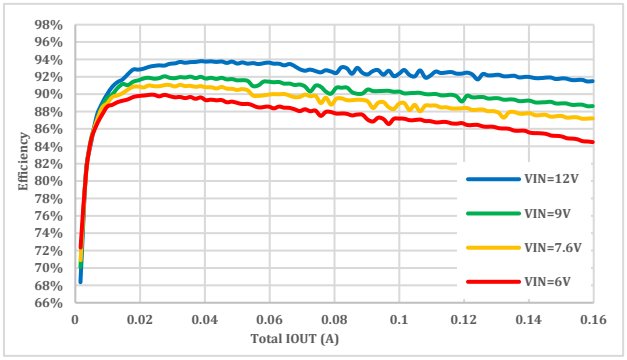


Figure 9. 8P12S System Efficiency[2], 10 µH Inductor

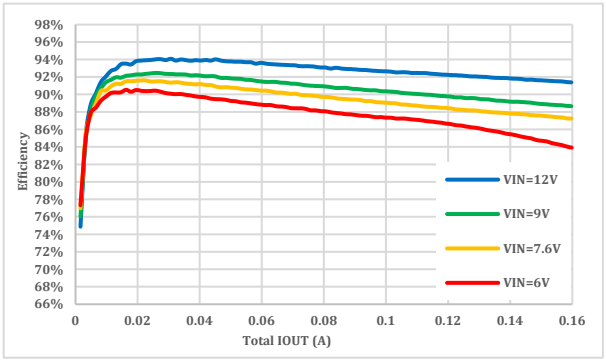


Figure 10. 8P14S Boost Efficiency[1], 10 µH Inductor

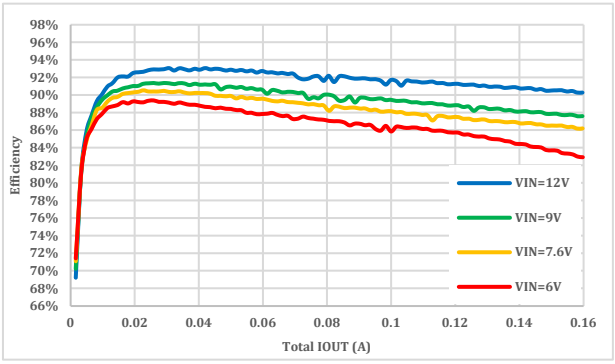


Figure 11. 8P14S System Efficiency[2], 10 µH Inductor

Notes

1. *Boost Efficiency = POUT/PVBAT*
2. *System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG=LED regulation voltage.*

Typical Characteristics (cont.)

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10 µH, Cout=4x2.2 µF, IMAX=20 mA, LED VF=2.8V at 20 mA (typ.) analog dimming.

Efficiency – 715 kHz Boost Switching Frequency

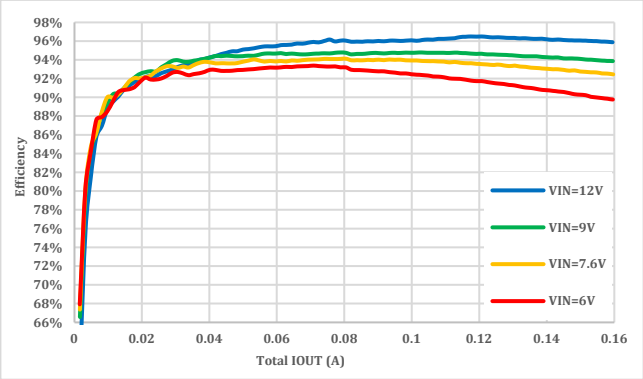


Figure 12. 8P10S Boost Efficiency[1], 10 µH Inductor

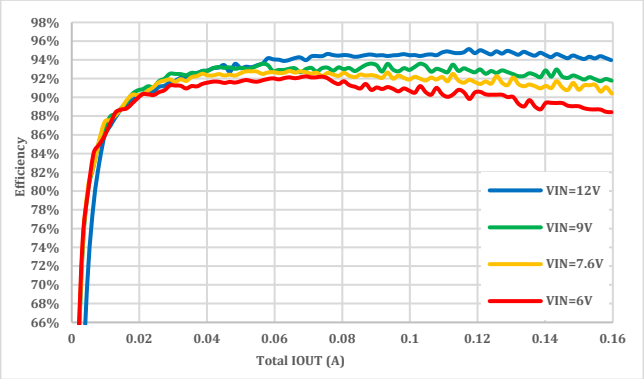


Figure 13. 8P10S System Efficiency[2], 10 µH Inductor

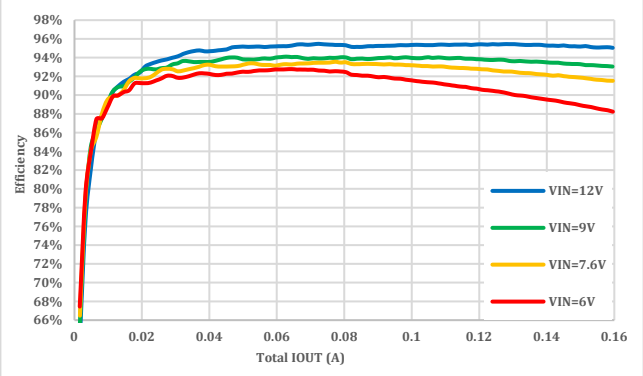


Figure 14. 8P12S Boost Efficiency[1], 10 µH Inductor

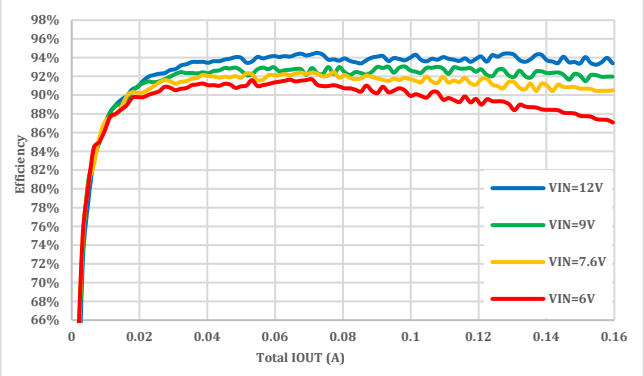


Figure 15. 8P12S System Efficiency[2], 10 µH Inductor

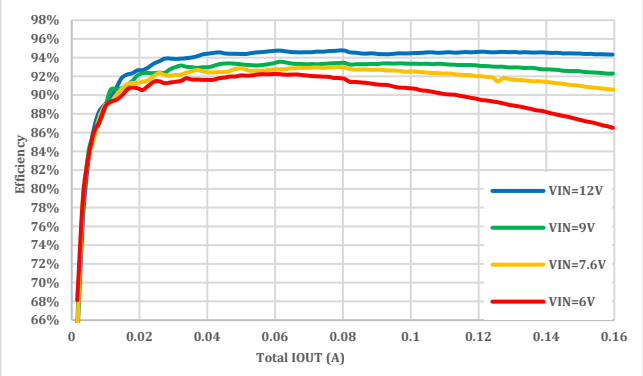


Figure 16. 8P14S Boost Efficiency[1], 10 µH Inductor

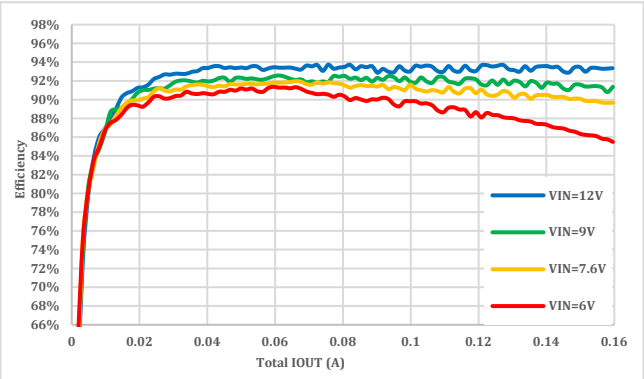


Figure 17. 8P14S System Efficiency[2], 10 µH Inductor

Notes:

1. *Boost Efficiency = POUT/PVBAT.*
2. *System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG=LED regulation voltage.*

Typical Characteristics (cont.)

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10 µH, Cout=4x2.2 µF, IMAX=20 mA, LED VF=2.8V at 20 mA (typ.) analog dimming.

Efficiency – 953 kHz Boost Switching Frequency

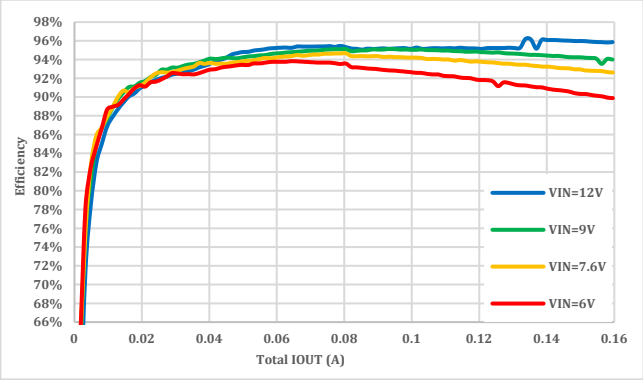


Figure 18. 8P10S Boost Efficiency[1], 10 µH Inductor

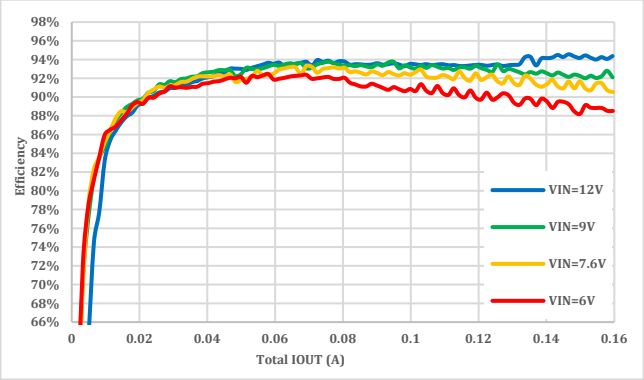


Figure 19. 8P10S System Efficiency[2], 10 µH Inductor

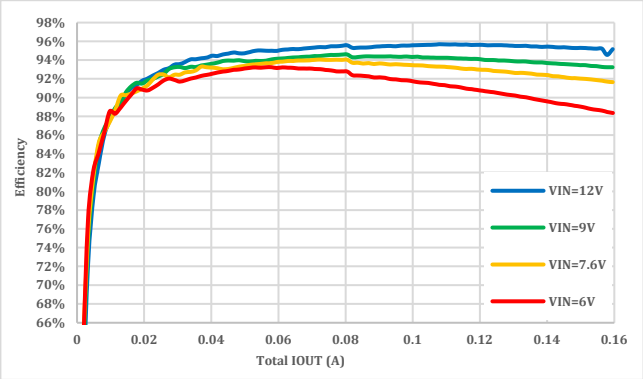


Figure 20. 8P12S Boost Efficiency[1], 10 µH Inductor

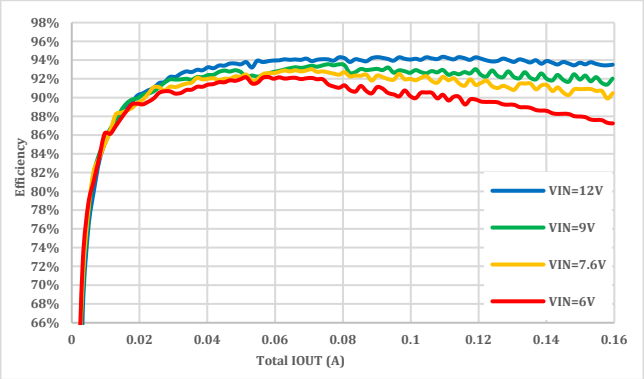


Figure 21. 8P12S System Efficiency[2], 10 µH Inductor

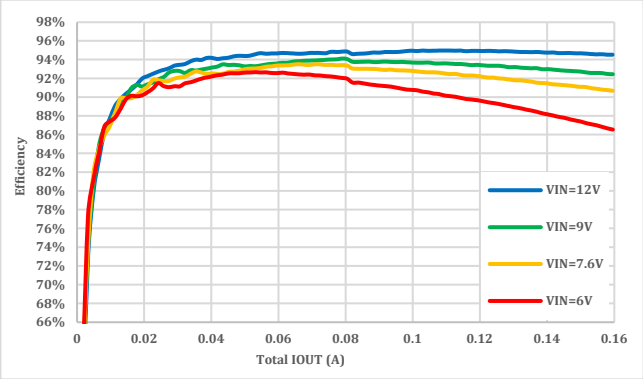


Figure 22. 8P14S Boost Efficiency[1], 10 µH Inductor

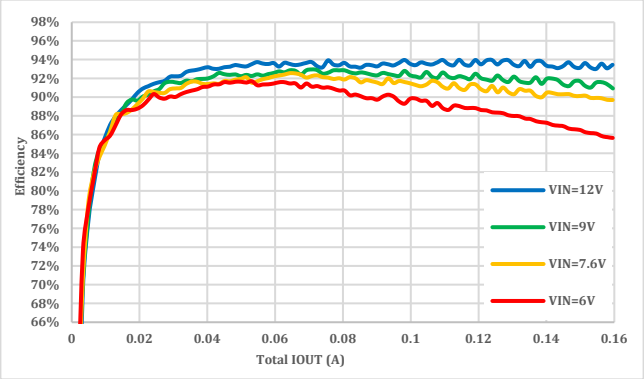


Figure 23. 8P14S System Efficiency[2], 10 µH Inductor

Notes:

1. *Boost Efficiency = POUT/PVBAT.*
2. *System Efficiency = (VOUT-VREG) * IOUT / (PVBAT+PVCC), where VREG=LED regulation voltage.*

Typical Characteristics (cont.)

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10uH, Cout=4x2.2 µF, IMAX=20mA, LED VF=2.8V at 20 mA (typ.) analog dimming.

LED Current Sinks

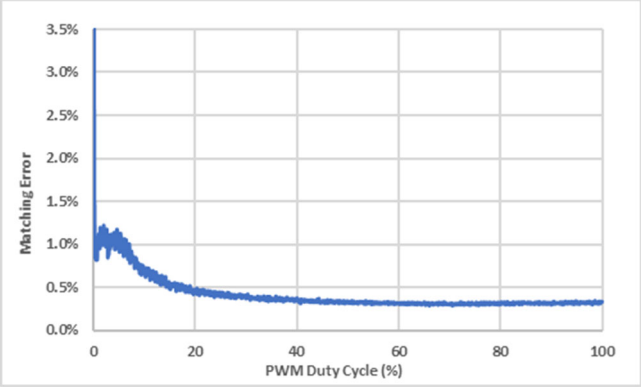


Figure 24. LED Matching – Analog (DC) Dimming Mode at 20 mA MAX_I

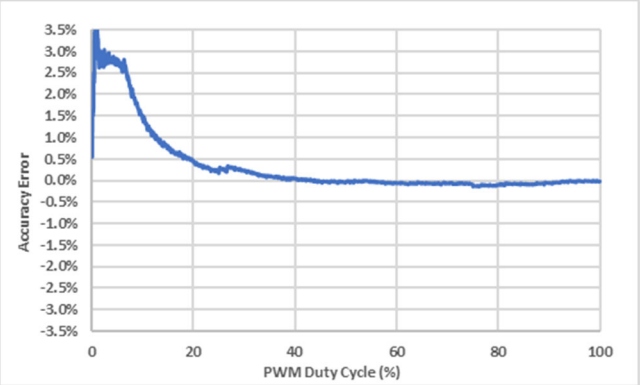


Figure 25. LED Accuracy – Analog (DC) Dimming Mode at 20 mA MAX_I

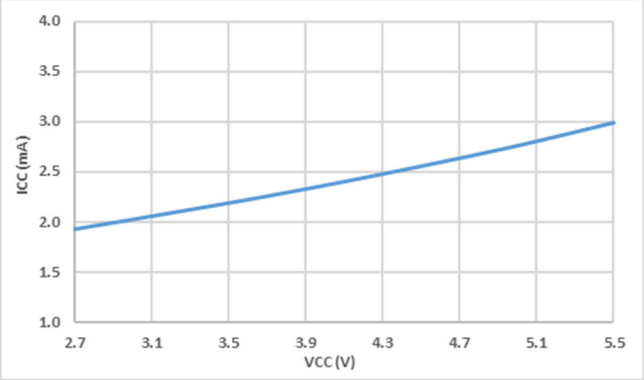


Figure 26. ICC vs. VCC at 10 mA MAX_I, Fsw=715kHz

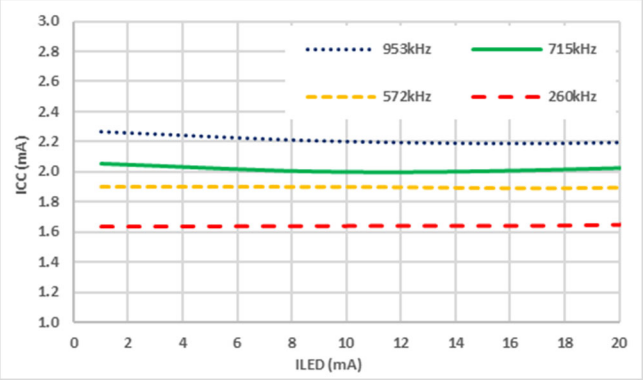


Figure 27. ICC vs. ILED at VCC=3.3V

Startup Characteristics

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10 µH, Cout=4x2.2 µF, IMAX=20 mA, LED VF=2.8V at 20 mA (typ.) analog dimming.

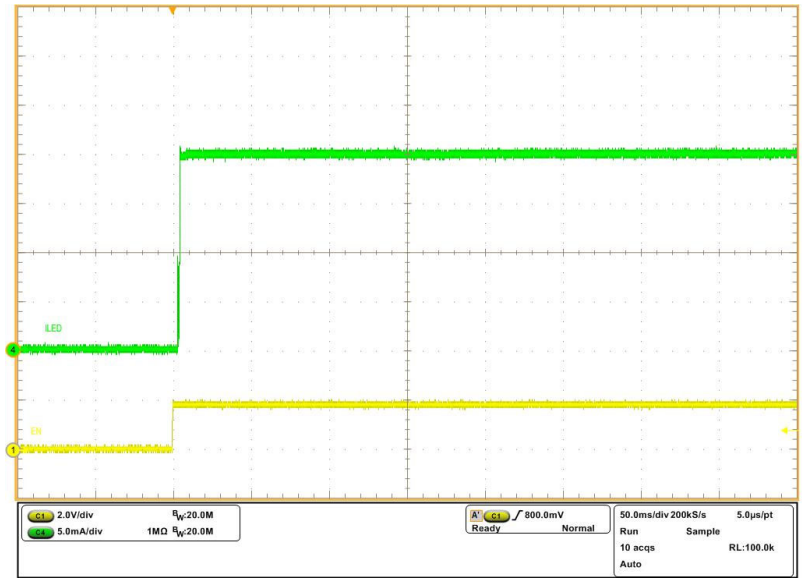


Figure 27. Startup Under 99% PWM Condition. 8P12S Configuration. Hybrid Dimming @ 25%. VBAT=12V (CH1 – EN, CH4 – ILED)

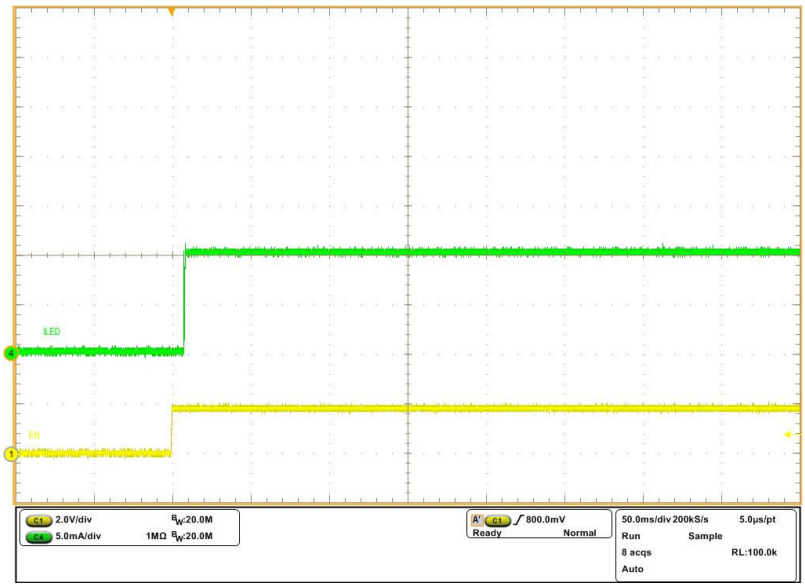


Figure 28. Startup Under 50% PWM Condition. 8P12S Configuration. Hybrid Dimming @ 25%. VBAT=12V (CH1 – EN, CH4 – ILED)

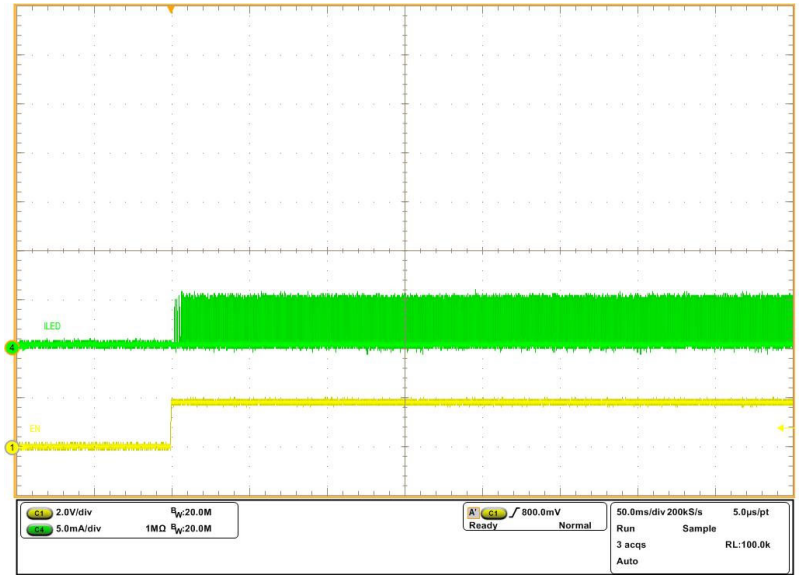


Figure 29. Startup Under 1% PWM Condition. 8P12S Configuration. Hybrid Dimming @ 25%. VBAT=12V (CH1 – EN, CH4 – ILED)

Thermal Performance

Unless otherwise specified: VCC=3.3V, VBAT=12V, L1=10 µH, Cout=4x2.2 µF, IMAX=20 mA, LED VF=2.8V at 20 mA (typ.) analog dimming

Figure 30. PE23108 Thermal Performance
8p14s configuration, 38.8V VOUT, 120 mA IOUT, 6V VBAT, 3.3V VCC 0.454W Power Dissipation,
1.0 mm 10 µH Inductor (DFE322512F-100M, Ambient Temperature is 25°C
Maximum case temperature is 42.5°C close to the LX and PGND pins of the package

Detailed Description

The PE23108 utilizes a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve very high peak efficiencies and superior efficiency over the two-cell/three-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the selection of LEDs.

The PE23108 supports 1 to 8 LED strings. Unused LEDx pins should be tied to ground. This provides maximum design flexibility for wide variety of LCD screens. Strings can be paralleled together to drive a LED string at a higher current.

The PE23108 provides a full set of protection features to guarantee robust system operation that include input voltage under-voltage lockout (UVLO), thermal shutdown (TSD), boost and charge pump over-current protection (OCP), boost and charge pump output over-voltage and under-voltage protection (OVP and UVP), and LED open and short detection.

Input Sequencing Requirements

There is no specific input sequencing requirement, but it is recommended to apply VCC, then apply VBAT and apply EN at last. The IC enables when the following conditions are met: VBAT> $V_{VBAT-UVLO\_H}$, VCC> $V_{VCC-UVLO\_H}$, and EN > V_{IH_EN}

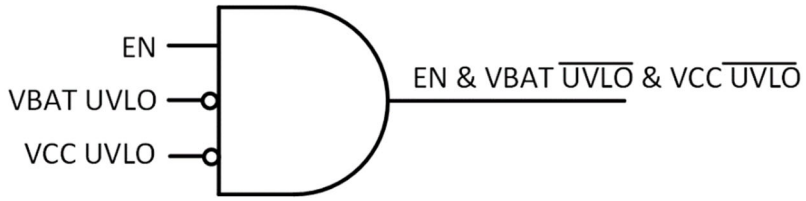


Figure 31. Input Sequencing Logic Diagram

The sequence for the PWM pin does not matter. It can be switched according to the application requirements or at 0%/100% while all other inputs are being turned on and off. See Table 6 for further clarification on various PE23108 input conditions.

VCC	VBAT	EN	DEVICE STATUS
Low	Low	Low	Non-operational
High	High	Low	Non-operational
Low	High	High	Non-operational
High	Low	High	Non-operational
High	High	High	Full IC operational

Table 6. Input Conditions

Under-voltage Lockout (UVLO)

PE23108 provides continuous monitoring of the VCC and VBAT inputs. When VCC voltage drops below approximately 2.5V and/or VBAT voltage drops below approximately 4.2V, the PE23108 will immediately shut down.

Output Over-voltage and Under-voltage Protection

The PE23108 protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is updated to 1, and the PE23108 turns off the boost converter. The boost converter automatically restarts after an OVP event when VOUT decreases below the threshold plus 0.35V typical hysteresis.

The over-voltage threshold can be configured through OVP_TH[3:0] bits in COMMAND register. The accuracy of each over-voltage threshold is +/-5%.

VOUT_OVP_SEL[3:0]	VOUT OVER-VOLTAGE THRESHOLD (V)
0000	Reserved
0001	
0010	43.75
0011	41.875
0100	40.0
0101	38.125
0110	36.25
0111	34.375
1000	32.5
1001	30.625
1010	28.75
1011	26.875
1100	25.0
1101	23.125
1110	21.25
1111	19.375

Table 7. Over-voltage Threshold

The user should select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application, in order to guarantee proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

Table 8 explains all RESET and Standby states when the part uses the I²C interface.

For all modes: UVLO high = POR IC (entire chip shut-down).

EN PIN LOGIC LEVEL	I2C_STANDBY	LEDEN[8:1]	RESET	STATUS	INTERNAL BLOCK ON	REGISTER
0	-	-	-	OFF	None	Cleared
1	0	0	0	Ready	References ON, Boost/CP off, LED drivers on standby	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	-	-	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	-	1 (self-clearing)	Reset -> Ready (self-clearing)	Ready state after self-clearing reset	Cleared
Note: "-" Denotes that level can be either high or low and does not affect operation.						

Table 8. RESET and Standby States

The STATUS1 and STATUS2 register bits are all cleared upon read, so repeated read-back of a logic-high fault bit indicates the fault event remains persistent.

Boost Output Over-voltage and Under-voltage Protection

If the boost output voltage (VX) falls below the VBAT voltage plus a VBAT-proportional offset after the LED current sinks have turned on, the PE23108 will shut down the switching converter and the LED current sinks immediately and register bit VX_UV in STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and will not start unless the part is shutdown or reset as explained in Table 8, RESET and Standby States.

The PE23108 is able to detect a missing or unconnected inductor upon startup by monitoring the boost output prior to enabling the switching converter and LED strings. When an inductor open is detected, the switching converter and LED strings remain off and both the SS_TIMEOUT and VX_UV bits in the STATUS1 register will be set and are cleared upon read.

Soft-Start Time-Out

The PE23108 implements a soft-start time out fault. If the output voltage does not rise above 2x of the battery voltage within 10ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in STATUS1 register is set to 1. This is a latched fault. The PE23108 will not start up until a reset event occurs, i.e., by toggling EN low or setting the RESET bit in the CONFIG4 register (which clears itself).

LED Short Protection

The PE23108 includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator enables when at least one LED pin is in regulation and the shorted LED fault is triggered when a LEDx voltage rises above the shorted LED voltage threshold. The shorted LED voltage threshold can be programmed to 4.35V, 4.85V, 5.25V and 5.75V by using the LED_SHORT_VTH[1:0] bits in the CONFIG3 register. This fault condition may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings. The threshold level is reference to ground.

The reduced forward voltage causes the current sink attached to that string to have a higher voltage than other current sinks, which could cause over-heating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED short fault is recorded in the STATUS1 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output will rise until it crosses the VOUT OVP threshold. Any string that is under-regulation at that moment is blocked from controlling VOUT, resulting in the output decreasing to a level needed to regulate the remaining non-open LED strings. An LED open fault is recorded in STATUS2 register.

If the open LED string is re-connected, the LED current sink will re-establish current to the level based on the output voltage, but it will not be allowed to control the VOUT voltage. All LEDs need to be turned off or the part needs to be reset in order to re-enable output control for any faulted strings.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit. It starts up initially with a de-rated over-current limit of 1.0A typically for soft-start. The cycle-by-cycle over-current limit can be programmed to 1A, 2A, 2.5A or 3A by using the BOOST_ILIM[1:0] bits in CONFIG1 register. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults where the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds the secondary current limit, which is 1-2A above the programmed BOOST_ILIM[1:0] setting, the converter and the LED current sinks are disabled immediately. The BST_ILIM_SEC bit in the STATUS1 register will be set and is cleared upon read. The switching converter and LED current sinks remain latched off and will not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented where if the output voltage drops suddenly forcing a large current out of the charge-pump, the output will be disconnected from the charge pump and the LED current sinks are temporarily disabled. The boost and charge pump remain switching, regulating at the last known voltage level. The DISC_OCP bit in the STATUS1 register will be set. The LED current sinks are enabled again when the fault at the VOUT pin is removed.

Current Setting

The maximum current of the LED outputs is set by the MAX_I[4:0] register bits in the CONFIG2 register. The default maximum current is 20 mA per LED string with 31 further settings available: 2 mA to 33 mA in 1 mA increment per step. Note that Murata trims parts for current accuracy at the default MAX_I[4:0] of 20 mA.

Fine tuning of the maximum current of the LED outputs can be set by the IMAXTUNE[3:0] register bits in the VREG_IMAXTUNE register. This allows incremental increases in the maximum output current from the MAX_I[4:0] setting mentioned above, in 4-bit resolution (16 steps) over a range from 0% to 7.66% with an average 0.51% per step. Using IMAXTUNE[3:0] to increase maximum output current from these default values will result in some loss of accuracy.

MAX_I[4:0]	FULL SCALE ILED CURRENT	MAX_I[4:0]	FULL SCALE ILED CURRENT
00000	2 mA	1 0000	18 mA
00001	3 mA	1 0001	19 mA
00010	4 mA	1 0010	20 mA
00011	5 mA	1 0011	21 mA
00100	6 mA	1 0100	22 mA
00101	7 mA	1 0101	23 mA
00110	8 mA	1 0110	24 mA
00111	9 mA	1 0111	25 mA
01000	10 mA	1 1000	26 mA
01001	11 mA	1 1001	27 mA
01010	12 mA	1 1010	28 mA
01011	13 mA	1 1011	29 mA
01100	14 mA	1 1100	30 mA
01101	15 mA	1 1101	31 mA
01110	16 mA	1 1110	32 mA
01111	17 mA	1 1111	33 mA

Table 9. Current Settings

Boost Converter Switching Frequency

The PE23108's boost converter provides wide frequency selection to meet different users' requirements. Four bits are used to set the boost switching frequency(f_{SW_BOOST}), which are the FSW_BOOST[3:0] bits in the CONFIG1 register. See Table 10.

The choice of inductor, charge pump fly capacitors and compensation components is dependent on the selected boost switching frequency for proper part operation. Contact Murata for recommended component types and values.

FREQ (KHZ)	FSW_BOOST[3:0] BINARY CODE
1430	0010
953	0011
715	0100
572	0101
477	0110
409	0111
358	1000
318	1001
286	1010
260	1011
238	1100
220	1101
204	1110
191	1111

Table 10. Boost Switching Frequency Settings

Charge Pump Switching Frequency

Table 11 lists the default relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency. The charge-pump frequency ratio and relationship to the LED brightness setting are programmable using the CP_FREQ_TRAN, SEL_CP_FREQ and CP_FREQ_DIV[1:0] bits in the CONFIG_CP register. See Table 11 for the charge pump frequency ratio setting at different CP_FREQ_TRAN, SEL_CP_FREQ and CP_FREQ_DIV[1:0] bit settings and LED brightness level. Detailed bit function is listed in the "Detailed Register Description" CONFIG_CP section.

It is recommended to select 1/8 CP frequency for IOUT≤120 mA, 1/4 CP frequency for 120 mA<IOUT≤180 mA and 1/2 CP frequency for IOUT>180 mA.

CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1]	CP_FREQ_DIV[0]	CP FREQUENCY RATIO
0	0	X	X	1/8 at <50% LED brightness 1/4 between ≥50% and <75% LED brightness 1/2 at ≥75% LED brightness
0	1	0	0	1/2 across entire LED brightness range
0	1	0	1	1/4 across entire LED brightness range
0	1	1	0	1/8 across entire LED brightness range
0	1	1	1	1/8 across entire LED brightness range
1	X	X	0	1/4 at <50% LED brightness 1/2 at ≥50% LED brightness
1	X	X	1	1/8 at <50% LED brightness 1/4 at ≥50% LED brightness

Table 11. Charge-Pump Frequency Ratio

Switching Converter Compensation

The switching converter operates in hybrid voltage-mode control and uses Type-II compensation which requires 2 external components:

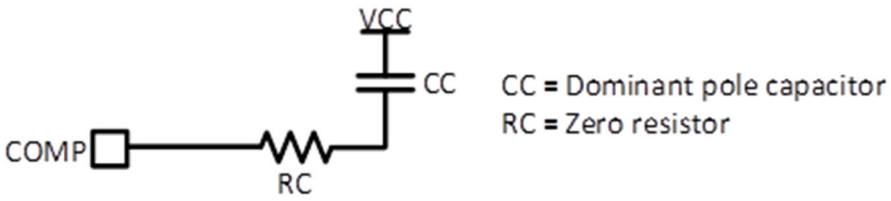


Figure 32. Compensation Components

Table 12 shows the recommended compensation component selection for different inductor values.

The SEL_VR[2:0] sets the control loop DC gain.

For a more specific set of compensation components to optimize bandwidth and phase margin for your application, please contact Murata.

INDUCTOR	RC VALUE	CC VALUE	SEL_VR[2:0]
10 µH	200 kΩ	2.2 nF	110

Table 12. Compensation Components

LED Current Output Dimming

The PE23108 supports three LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency and minimal WLED color shift at low brightness levels. These options are Analog, Phase Shift PWM, and Hybrid PWM (Mixed-Mode) dimming.

Analog Dimming (DC Modulation)

When CONFIG2 register, DIM_MODE bit is set to 0, dimming is set to Analog only. In analog dimming, the LED current sink output is always a dc current across the entire brightness range. As brightness is reduced, the LED current sink output DC level decreases which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the VOUT voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a DC current output also minimizes noise in the system.

Phase Shift PWM Dimming (PWM Modulation)

When CONFIG2 register, DIM_MODE bit is set to 1, PWM dimming is enabled. Under this mode, the mixed dimming block generates phase shifted PWM signals to dim active LED strings when the required LED current is below the threshold set by PWM_IX[1:0] register bits. The phase difference between active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of 4 frequency settings between 2.79 kHz and 22.49 kHz using the PWM_DIM_FREQ[2:0] register bits.

Hybrid PWM (Mixed-Mode) Dimming

The PE23108 allows a mixed dimming output scheme for better optical efficiency. The switch point from analog to PWM dimming is set by register bits DIM_MODE=1 and PWM_IX[1:0], and can be, 12.5%, 25%, 50% or 100% of the brightness range. 100% means PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted, and below the switch point, PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved while minimizing system noise at higher brightness levels.

PWM_IX[1:0]=11 results in a DC output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.

PWM_IX[1:0]=10 results in a DC output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.

PWM_IX[1:0]=01 results in a DC output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.

PWM_IX[1:0]=00 results in a DC output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

An example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting is shown in Figure 33.

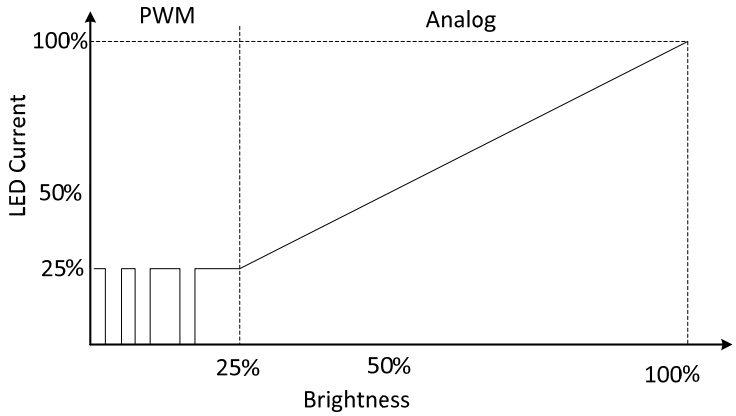


Figure 33. Mixed-Mode Dimming

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Since the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also has to scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0]=01 (25% transition point) is four times longer than at PWM_IX[1:0]=11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is 700 ns typically.

LED Brightness Control

The LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET_MSB and WLED_ISET_LSB registers written via the I²C interface, or both. The register bits DIMCODE[1:0] select 3 different brightness control options.

DIMCODE=00

When DIMCODE=00, the LED current is controlled only by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate a DC current level or phase-shifted PWM currents at the LED strings.

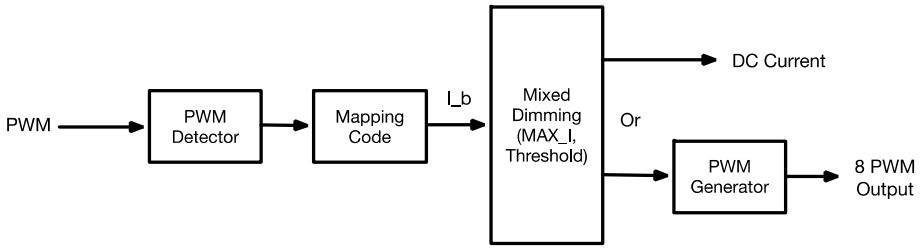


Figure 34. DIMCODE=00

DIMCODE=01

When DIMCODE=01, the LED current is controlled by the WLED_ISET_MSB and WLED_ISET_LSB registers via the I²C interface. The register codes go through a mapping first, then through the mixed dimming block to generate a DC current level or eight phase-shifted PWM currents at the LED strings. The user must first write to the WLED_ISET_LSB register and then the WLED_ISET_MSB register to update the 12-bit dimming value.

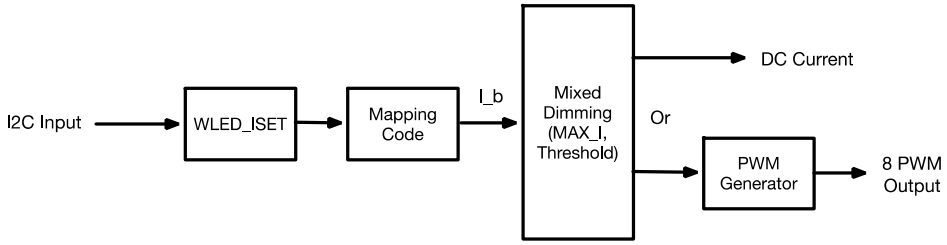


Figure 35. DIMCODE=01

DIMCODE=10

When DIMCODE=10, the LED current is controlled by both the PWM input duty cycle and the WLED_ISET_MSB and WLED_ISET_LSB register values via the I²C interface. The register codes go through a mapping first and then are multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate a DC current level or eight phase-shifted PWM currents.

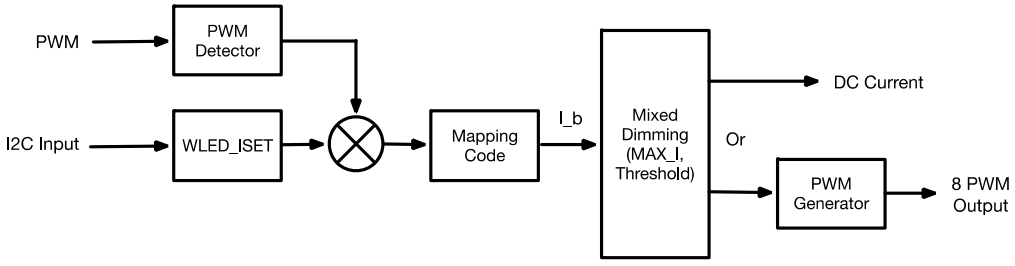


Figure 36. DIMCODE=10

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either via the PWM input or WLED_ISET_MSB and WLED_ISET_LSB registers are translated linearly into the LED current. This is the factory default setting. There are 4095 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit=0), and 32767 possible brightness states with the dither function enabled (DITHER_ENABLE bit=1).

For a better visual experience, PE23108 can also translate the dimming settings via a logarithmic mapping to produce the LED current. The user can set the LOG_MODE bit to 1 in the CONFIG2 register to enable this feature. There are 1023 possible brightness states in this mode with the dither function disabled (DITHER_ENABLE bit=0), and 8191 possible brightness states with the dither function enabled (DITHER_ENABLE bit=1).

With the dither function enabled, the PE23108 utilizes the DITHER_LSB[2:0] bits combined with WLED_ISET_MSB[11:4] and WLED_ISET_LSB[3:0] to form a 15-bit LED output current setting, where the DITHER_LSB[2:0] bits become the lower LSBs. The user can then write to the 8 MSBs in register 0x06 first then the 7 LSBs in register 0x05 for a 15-bit resolution LED dimming adjustment.

PWM Input and Output Resolution

With DIMCODE=00, the brightness is controlled by input PWM signal. The PE23108's PWM input frequency range is from 100 Hz to 40 KHz. The input frequency is independent of the PWM output frequency. The PWM output frequency is set by the PWM_DIM_FREQ[2:0] register bits.

Note that since the on-chip clock is 2.857 MHz, a 12-bit PWM input resolution can be obtained with at 697 Hz PWM input signal (2.857 MHz/2^12 = 697 Hz). Lower PWM input frequencies will increase PWM input resolution, and higher PWM input frequencies will reduce PWM input resolution. See Table 13 for input resolution at different PWM input frequencies.

PWM INPUT FREQUENCY	INPUT RESOLUTION
fPWM ≤ 174 Hz	14 bits
174 Hz < fPWM ≤ 349 Hz	13 bits
349 Hz < fPWM ≤ 697 Hz	12 bits
697 Hz < fPWM ≤ 1.395 kHz	11 bits
1.395 kHz < fPWM ≤ 2.79 kHz	10 bits
2.79 kHz < fPWM ≤ 5.58 kHz	9 bits
5.58 kHz < fPWM ≤ 11.16 kHz	8 bits
11.16 kHz < fPWM ≤ 22.32 kHz	7 bits

Table 13. Input Resolution at Different PWM Input Frequencies

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0]=11). A 2.79 kHz PWM output frequency setting (PWM_DIM_FREQ[2:0]=001) provides 10 bits of dimming resolution relative to the full-scale LED output current, so each 25% segment has 8 bits of dimming resolution. In hybrid dimming, depending on the hybrid transition point, a higher resolution can be achieved by selecting a lower transition point. For example, with a 25% transition point, the same 2.79 kHz PWM output frequency setting would provide a 10 bits resolution from 0% to 25% dimming range vs 8 bits in 100% PWM dimming. The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

The PE23108 provides a dithering function by increasing the dimming resolution. With the DITHER_ENABLE bit set to 1, the dimming resolution increases by 3 bits by utilizing the DITHER_LSB[2:0] bits as the lower 3 LSB. These three LSB bits combine with the WLED_ISET[11:0] to provide 15-bit of dimming resolution. See Table 14 for PWM output resolution at different PWM output frequency settings.

PWM OUTPUT FREQUENCY SETTING	OUTPUT RESOLUTION	OUTPUT RESOLUTION WITH DITHER ON
2.79 kHz	10 bits	13 bits
5.59 kHz	9 bits	12 bits
11.2 kHz	8 bits	11 bits
22.49 kHz	7 bits	10 bits

Table 14. Output Resolution at Different PWM Output Frequency Settings

Fade In/Out Control

The Fade In/Out control makes a smooth transition from one brightness value to another for a better human eye experience. PE23108 provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED[7:0] bits in the FADING_SPEED register. See the register FADING_SPEED section for detailed description.

Digital R-C Filter Mode Brightness Change

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to pick a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC-filter is used to filter the output brightness change response to each input brightness change.

Two bits RCFILTER[1:0], control the coefficient of this RC time constant as shown in Table 15 for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings. The RCFILTER[1:0] bits are available through the FILTER_SETTINGS register.

RCFILTER[1:0]	RC TIME CONSTANT (T)
00	Disabled
01	417 ms
10	207 ms
11	103 ms

Table 15. RC Filter Settings

Input PWM Filter

When a duty cycle is applied at the PWM pin to control brightness, the on-time and period are sampled by the internal 2.857 MHz master clock to translate time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by +/-1 LSB at steady-state, which translates into jitter on the final brightness result, and this can be visible as flicker. Adding some basic filtering to this sampled system can help eliminate this flicker at steady-state.

PWMFILTER[2:0] register bits in FILTER_SETTING register enable/disable this filter as well as control the amount of filtering. Furthermore, the filtering is dependent on the direction of the sampled PWM time-step as follows: if the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold. Conversely, if the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold. The time-step size is 700 ns.

PWMFILTER[2:0]	MINIMUM PWM TIME-STEP SIZE
000	OFF
001	2 steps
010	4 steps
011	6 steps
100	8 steps
101	10 steps
110	12 steps
111	14 steps

Table 16. PWM Filter Settings

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The PE23108 operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps), fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as VCC and VBAT voltages remain above UVLO and the EN pin remain asserted.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The PE23108 supports 7-bit addressing; 10-bit addressing, and general call address are not supported. The device 7-bit address is defined as ‘1001XXX‘.

Programming I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple PE23108 parts to be addressed on one I²C bus, the lower 3 bits of the I²C slave address are programmable by using the ADDR pin. The ADDR pin configuration to the device 7-bit address and 8-bit address with R/Wb low is shown in Table 17.

ADDR PIN	DEVICE 7 BIT ADDRESS	DEVICE 8 BIT ADDRESS WITH R/=0
Tied to AGND	1001000 (0x48)	10010000 (0x90)
Floating	1001010 (0x4A)	10010100 (0x94)
Tied to VCC	1001101 (0x4D)	10011010 (0x9A)

Table 17. ADDR Pin Configuration

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 37. All I²C-compatible devices should recognize a start condition.

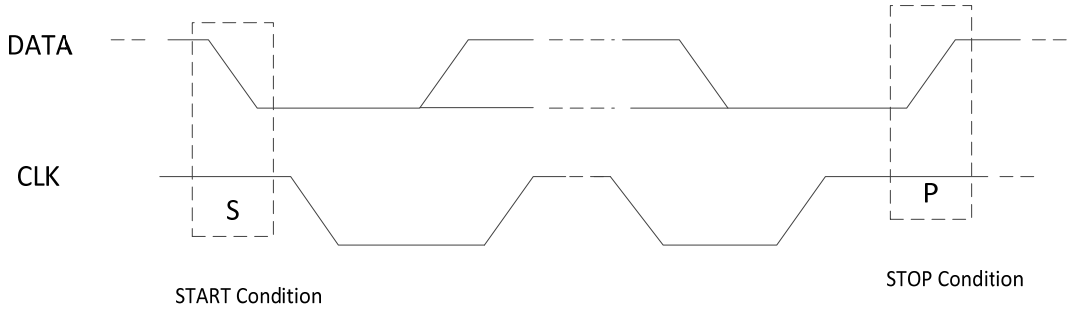


Figure 37. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/Wb on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. See Figure 38, Bit Transfer on the Serial Interface.

The master generates further SCL cycles to either transmit data to the slave (R/"W" bit 0) or receive data from the slave (R/"W" bit 1). In either case, the receiver needs to acknowledge the data sent by transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. Nine-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 37. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

PE23108 I²C Update Sequence

The PE23108 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, PE23108 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the PE23108. The PE23108 performs an update on the falling edge of the acknowledge signal that follows the LSB.

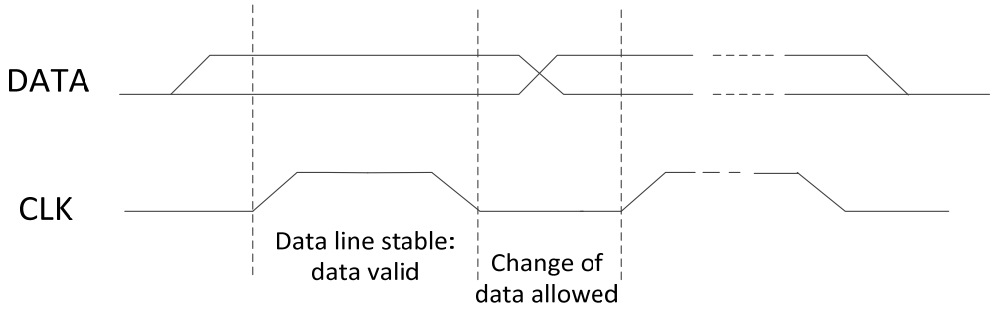


Figure 38. Bit Transfer on the Serial Interface

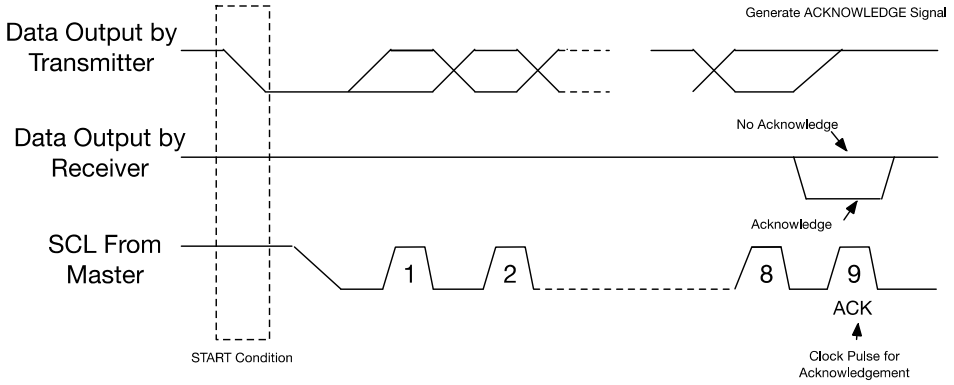


Figure 39. Acknowledge on the I²C Bus

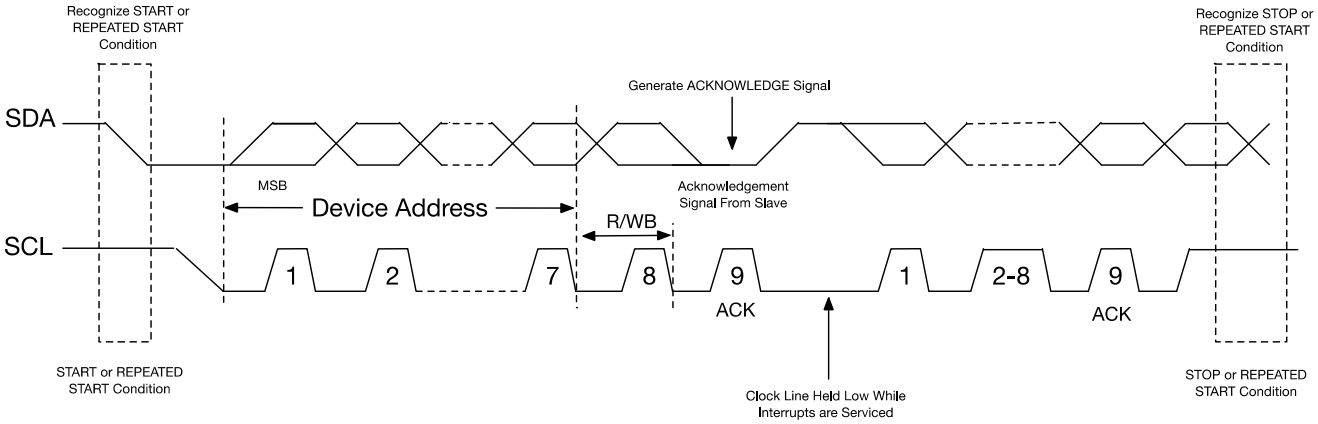


Figure 40. Bus Protocol

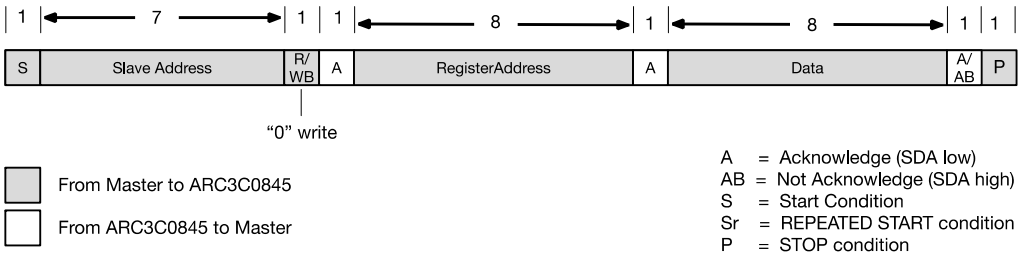


Figure 41. "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

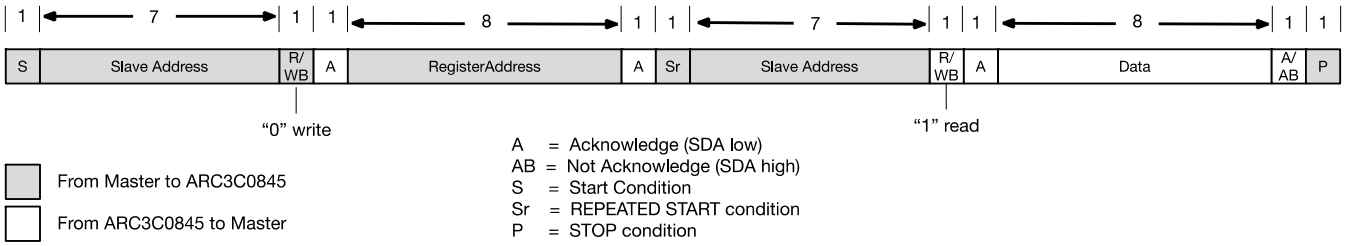


Figure 42. "Read" Data Transfer Format in Standard, Fast, Fast-Plus Modes

PE23108 MTP Non-volatile Memory Description

The PE23108 contains non-volatile memory (NVM) to store the default values for registers 0x00 to 0x0B. The data in the NVM is recalled to the registers at the device POR event. This function saves system initialization time by allowing user to program the device default setting in the production line instead of programming these settings every time after POR event. To perform the MTP programming cycle, first write the desired values for registers 0x00 to 0x0B. Then set the MTP_WRITE_CMD[4:0] bits to 10010 to initialize the MTP programming. During the MTP programming cycle, the MTP_WRITE_CMD[4:0] bits remain at 10010 and MTP_WRITE_DNE bit is at 0. When the MTP programming cycle completes, the MTP_WRITE_CMD[4:0] bits automatically reset back to 00000 and MTP_WRITE_DNE bit is set to 1. The MTP programming cycle takes 50 ms maximum to complete. During the MTP programming cycle, do not write to registers 0x00 to 0x0B to avoid data corruption.

Register Maps

Slave Address: 1001000 (0x48)[1]

Register Configuration Parameters

REGISTER	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	SEL_VR [2:0]			BOOST_MODE	OVP_TH [3:0]			
CONFIG1	0x01	(Reserved)	BOOST_ILIM [1:0]			FSW_BOOST [3:0]			
FADING_SPEED	0x02	FADING_SPEED [3:0]				(Reserved)			
CONFIG2	0x03	(Reserved)	LOG_ MODE	DIM_MODE	MAX_I [4:0]				
LEDEN	0x04	LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1
WLED_ISET_LSB	0x05	WLED_ISET_LSB [3:0]				DITHER_LSB[2:0]			(Reserved)
WLED_ISET_MSB	0x06	WLED_ISET_MSB [11:4]							
CONFIG3	0x07	(Reserved)	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ [2:0]		
CONFIG4	0x08	I2C_ STANDBY	RESET	(Reserved)					
FILTER_SETTINGS	0x09	DIMCODE [1:0]		DITHER_ ENABLE	RCFILTER [1:0]		PWMFILTER [2:0]		
VREG_IMAXTUNE	0x0A	LED_VREG_CNT_INIT [3:0]				IMAXTUNE [3:0]			
CONFIG_CP	0x0B	(Reserved)				CP_FREQ_ TRAN	SEL_CP_ FREQ	CP_FREQ_DIV [1:0]	
CHKSUM0	0x0C	CHKSUM0 [7:0]							
CHKSUM1	0x0D	CHKSUM1[7:0]							
STATUS1	0x0E	BST_ILIM_SEC	VOUT_ OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_ TIMEOUT	LED_SHORT
STATUS2	0x0F	MTP_WRITE_CMD [4:0]					MTP_WRITE_DNE	CRC_OK	LED_OPEN

Notes:
1. *ADDR pin tied to GND. Excluding read/write bit. 10010000 (0x90) if including R/Wb bit=0.)*

Detailed Register Description

Register COMMAND

ADDRESS	NAME	POR VALUE(1)
0x00	COMMAND	0xC2

Bit Assignment

7	6	5	4	3	2	1	0
SEL_VR [2:0]			BOOST_MODE	OVP_TH [3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
SEL_VR [2:0]	[7:5]	R/$\overline{w}$	110	3-bit selection of control loop DC GAIN: From highest (000) to lowest (111) in 2 dB increment. See Switching Converter Compensation for recommended setting.
BOOST_MODE	[4]	R/$\overline{w}$	0	0 = DCM fixed-frequency boost switching (no negative inductor current) 1 = Forced CCM fixed-frequency boost switching (negative inductor current allowed)
OVP_TH [3:0]	[3:0]	R/$\overline{w}$	0010	4-bit selection of VOUT OVP thresholds: 0010 – 43.75V (default) 0011 – 41.875V 0100 – 40V 0101 – 38.125V 0110 – 36.25V 0111 – 34.375V 1000 – 32.5V 1001 – 30.625V 1010 – 28.75V 1011 – 26.875V 1100 – 25V 1101 – 23.125V 1110 – 21.25V 1111 – 19.375V

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register CONFIG1

ADDRESS	NAME	POR VALUE(1)
0x01	CONFIG1	0x4B

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	BOOST_ILIM [1:0]		Reserved	FSW_BOOST[3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
Reserved	[7], [4]	R/$\overline{w}$	0	
BOOST_ILIM [1:0]	[6:5]	R/$\overline{w}$	10	Boost cycle-by-cycle ILIM threshold 00 = 2.0A 01 = 1.0A 10 = 2.5A (default) 11 = 3.0A
FSW_BOOST[3:0]	[3:0]	R/$\overline{w}$	1011	Boost switching frequency. See Boost Converter Switching Frequency section for full frequency chart. 0000-0010 = 1.43 MHz 0011 = 953 kHz 0100 = 715 kHz 0101 = 572 kHz 0110 = 477 kHz 0111 = 409 kHz 1000 = 358 kHz 1001 = 318 kHz 1010 = 286 kHz 1011 = 260 kHz (default) 1100 = 238 kHz 1101 = 220 kHz 1110 = 204 kHz 1111 = 191 kHz

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register FADING_SPEED

ADDRESS	NAME	POR VALUE(1)
0x02	FADING_SPEED	0x02

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED [3:0]				Reserved			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
FADING_ SPEED	[7:4]	R/$\overline{w}$	0000	Sets the fading counter value. This is the period between each intensity step. 0000 = No fading (default) 0001 = 44.70 µs per step 0010 = 1.432 ms per step 0011 = 2.148 ms per step 0100 = 2.860 ms per step 0101 = 3.548 ms per step 0110 = 4.290 ms per step 0111 = 5.012 ms per step 1000 = 5.700 ms per step 1001 = 6.440 ms per step 1010 = 7.160 ms per step 1011 = 7.800 ms per step 1100 = 8.590 ms per step 1101 = 9.300 ms per step 1110 = 10.024 ms per step 1111 = 10.700 ms per step
Reserved	[3:0]	R/$\overline{w}$	0010	

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register CONFIG2

ADDRESS	NAME	POR VALUE(1)
0x03	CONFIG2	0x12

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LOG_MODE	DIM_MODE	MAX_I [4:0]				

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
Reserved	[7]	R/$\overline{w}$	0	
LOG_MODE	[6]	R/$\overline{w}$	0	Dimming mode selector 0 = Linear mode (default) 1 = Logarithmic mode. The log table uses 1023 codes with the dither function disabled and up to 8191 codes with the dither function enabled.
DIM_MODE	[5]	R/$\overline{w}$	0	Dimming mode selector 0 = Analog dimming only (default) 1 = Mixed-mode dimming
MAX_I [4:0]	[4:0]	R/$\overline{w}$	10010	Program maximum current per string in 1 mA steps: 00000 = 2 mA 10000=18 mA 00001 = 3 mA 10001=19 mA 00010 = 4 mA 10010 = 20 mA (default) 00011 = 5 mA 10011 = 21 mA 00100 = 6 mA 10100 = 22 mA 00101 = 7 mA 10101 = 23 mA 00110 = 8 mA 10110 = 24 mA 00111 = 9 mA 10111 = 25 mA 01000 = 10 mA 11000 = 26 mA 01001 = 11 mA 11001 = 27 mA 01010 = 12 mA 11010 = 28 mA 01011 = 13 mA 11011 = 29 mA 01100 = 14 mA 11100 = 20 mA 01101 = 15 mA 11101 = 31 mA 01110 = 16 mA 11110 = 32 mA 01111 = 17 mA 11111 = 33 mA

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register LEDEN

ADDRESS	NAME	POR VALUE(1)
0x04	LEDEN	0xFF

Bit Assignment

7	6	5	4	3	2	1	0
LEDEN_8	LEDEN_7	LEDEN_6	LEDEN_5	LEDEN_4	LEDEN_3	LEDEN_2	LEDEN_1

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
LEDEN_8,.., LEDEN_1	[7:0]	R/$\overline{W}$	0	LED string enabled 0 = string is disabled 1 = string is enabled (default)

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register WLED_ISET_LSB

ADDRESS	NAME	POR VALUE(1)
0x05	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				DITHER_LSB[2:0]			Reserved

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
WLED_ISET[3:0]	[7:4]	R/$\overline{w}$	0000	LED output current setting bits 1-0. For details, please refer to the WLED section. If changing the LSB bits, these must be written before the MSB bits. Changes to these bits are only implemented when the next register is written, which is typically the MSBs but could be any register.
DITHER_LSB[2.0]	[3:1]	R/$\overline{w}$	000	With DITHER_ENABLE=1, these three bits combine with WLED_ISET[11:0] as the lower LSBs to form a 15-bit ILED dimming control. Write to these bits along with WLED_ISET[11:0] for 15-bit dimming adjustment.
Reserved	[0]	R/$\overline{w}$	0	

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register WLED_ISET_MSB

ADDRESS	NAME	POR VALUE(1)
0x06	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[9:4]							

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
WLED_ISET[11:4]	[7:0]	R/$\overline{W}$	00000000	The MSB bits of the WLED_ISET[9:0] brightness code. For details see the WLED section.

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register CONFIG3

ADDRESS	NAME	POR VALUE(1)
0x07	CONFIG3	0x0B

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	LED_SHORT_VTH [1:0]		PWM_IX [1:0]		PWM_DIM_FREQ[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
Reserved	[7]	R/$\overline{w}$	0	
LED_SHORT_VTH [1:0]	[6:5]	R/$\overline{w}$	00	LED short detect threshold: 00 = 4.35V (default) 01 = 4.85V 10 = 5.25V 11 = 5.75V
PWM_IX [1:0]	[4:3]	R/$\overline{w}$	01	PWM_IX[1:0] transition point between analog dimming and PWM dimming during mode change: 00 = 12.5% 01 = 25% (default) 10 = 50% 11 = 100% (also 100% PWM dimming)
PWM_DIM_FREQ	[2:0]	R/$\overline{w}$	011	PWM_DIM_FREQ (kHz) 000 = 2.79 kHz 001 = 5.59 kHz 010 = 11.2 kHz 011 = 22.49 kHz (default) 100, …, 111= reserved

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register CONFIG4

ADDRESS	NAME	POR VALUE(1)
0x08	CONFIG4	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C_STANDBY	RESET	Reserved					

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
I2C_STANDBY	[7]	R/$\overline{W}$	0	Quasi-low current mode with references and digital blocks disabled, but register contents retained (MTP not re-loaded) 0 = Not in standby 1 = Standby mode
RESET	[6]	R/$\overline{W}$	0	Power on reset bit – clears all register contents and MTP will be re-loaded
Reserved	[5:0]	R/$\overline{W}$	000000	

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register FILTER_SETTINGS

ADDRESS	NAME	POR VALUE(1)
0x09	FILTER_SETTINGS	0x24

Bit Assignment

7	6	5	4	3	2	1	0
DIMCODE[1:0]		DITHER_ENABLE	RCFILTER[1:0]		PWMFILTER[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
DIMCODE[1:0]	[7:6]	R/W	00	Brightness control method: 00 = PWM control only (default) 01 = I2C control only 10 = Input PWM x I2C control 11 = Reserved
DITHER_ENABLE	[5]	R/W	1	0 = Dithering disabled 1 = Enable dithering for up to 15-bit effective resolution for linear dimming mode, up to 13-bit effective resolution for logarithmic dimming mode (default).
RCFILTER[1:0]	[4:3]	R/W	00	RC Filter Time Constant (LI) 00 = RC filter OFF (default) 01 = 373.3 ms 10 = 185.2 ms 11 = 92.2 ms
PWMFILTER[2:0]	[2:0]	R/W	100	Enables/disables the PWM filter and sets step size: 000 = Off 001 = 2 steps 010 = 4 steps 011 = 6 steps 100 = 8 steps (default) 101 = 10 steps 110 = 12 steps 111 = 14 steps

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register VREG_IMAXTUNE

ADDRESS	NAME	POR VALUE(1)
0x0A	VREG_IMAXTUNE	0x00

Bit Assignment

7	6	5	4	3	2	1	0
LED_VREG_CNT_INIT[3:0]				IMAXTUNE[3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR (1)	DESCRIPTION
LED_VREG_CNT_INIT[3:0]	[7:4]	R/$\overline{W}$	0000	Initial VOUT starting target voltage: 0000 = 13.75V (default) 0001 = 16.02V 0010 = 18.29V 0011 = 20.56V 0100 = 22.83V 0101 = 25.1V 0110 = 27.37V 0111 = 29.64V 1000 = 31.91V 1001 = 34.18V 1010 = 36.45V 1011 = 38.72V 1100-1111 = Reserved
IMAXTUNE[3:0]	[3:0]	R/$\overline{W}$	0000	Sets percentage increase of LED full-scale current set by MAX_I[4:0] 0000 = 0.00% increase 0001 = 0.52% increase 0010 = 0.93% increase 0011 = 1.45% increase 0100 = 1.86% increase 0101 = 2.38% increase 0110 = 2.79% increase 0111 = 3.31% increase 1000 = 3.84% increase 1001 = 4.37% increase 1010 = 4.77% increase 1011 = 5.30% increase 1100 = 5.70% increase 1101 = 6.23% increase 1110 = 6.63% increase 1111 = 7.60% increase

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*

Register CONFIG_CP[2]

ADDRESS	NAME	POR VALUE[1]
0x0B	CONFIG_CP	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved				CP_FREQ_TRAN	SEL_CP_FREQ	CP_FREQ_DIV[1:0]	

Bit Description

FIELD NAME	BITS	TYPE	POR [1]	DESCRIPTION
Reserved	[7:4]	R/w	0000	
CP_FREQ_TRAN	[3]	R/w	0	0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump frequency changes at 50% LED brightness only, and as a function of CP_FREQ_DIV[0]
SEL_CP_FREQ	[2]	R/w	0	When CP_FREQ_TRAN=0: 0 = Charge pump frequency changes at 75% and 50% LED brightness automatically 1 = Charge pump is independent of LED brightness and selected by CP_FREQ_DIV[0] When CP_FREQ_TRAN=1: SEL_CP_FREQ bit is don't care
CP_FREQ_DIV[1:0]	[1:0]	R/w	00	When CP_FREQ_TRAN=0, SEL_CP_FREQ=1: 00 = 1/2 01 = 1/4 10 = 1/8 11 = 1/8 When CP_FREQ_TRAN=1: CP_FREQ_DIV[0] = 0 then charge pump frequency changes between 1/2 (≥50% LED brightness) and 1/4 (<50% LED brightness) CP_FREQ_DIV[0] = 1 then charge pump frequency changes between 1/4 (≥50% LED brightness) and 1/8 (<50% LED brightness)

Notes

1. *The POR value listed for each register is the factory programmed default value. These POR values may be no longer valid after performing MTP programming.*
2. *See the Charge Pump Switching Frequency Section for detailed operation description.*

Register CHKSUM0

ADDRESS	NAME
0X0C	CHKSUM0

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM0[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	DESCRIPTION
CHKSUM0[7:0]	[7:0]	R	Lower 8-bit of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded as long as the internal factory checksum is correct. After each MTP write, the CHKSUM0 register value is updated after toggling EN pin or cycling VCC.

Register CHKSUM1

ADDRESS	NAME
0x0D	CHKSUM1

Bit Assignment

7	6	5	4	3	2	1	0
CHKSUM1[7:0]							

Bit Description

FIELD NAME	BITS	TYPE	DESCRIPTION
CHKSUM1[7:0]	[7:0]	R	Upper 8-bit of the 16-bit register checksum for registers 0x00 to 0x0B. If incorrect, the MTP values are still loaded as long as the internal factory checksum is correct. After each MTP write, the CHKSUM1 register value is updated after toggling EN pin or cycling VCC.

Register STATUS1

ADDRESS	NAME	POR VALUE(1)
0x0E	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	DISC_OCP	TSD	SS_TIMEOUT	LED_SHORT

Bit Description

FIELD NAME	BITS	TYPE	POR(1)	DESCRIPTION
BST_ILIM_SEC	[7]	R	0	Status bit to flag a secondary current limit: 0 = No error 1 = Boost current exceeded secondary current limit
VOUT_OVP	[6]	R	0	Status bit to flag an output over-voltage condition: 0 = No error 1 = Output over-voltage
VX_OV	[5]	R	0	Status bit to flag a VX over-voltage condition: 0 = No error 1 = VX voltage is above over-voltage threshold
VX_UV	[4]	R	0	Status bit to flag a VX under-voltage condition: 0 = No error 1 = VX voltage is below under-voltage threshold
DISC_OCP	[3]	R	0	Status bit to flag a disconnect switch over-current event: 0 = No error 1 = Disconnect switch exceeded over-current threshold, or VOUT is shorted to ground
TSD	[2]	R	0	Status bit to flag a thermal shutdown condition: 0 = No error 1 = Part has exceeded thermal shutdown threshold
SS_TIMEOUT	[1]	R	0	Status bit to flag a soft start timeout condition: 0 = No error 1 = Soft start has not completed before the timeout event
LED_SHORT	[0]	R	0	Status bit to flag an LED shorted-string fault: 0 = No error 1 = An LED shorted-string event occurred on one or more enabled strings

Register STATUS2

ADDRESS	NAME	POR VALUE(1)
0x0F	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
MTP_WRITE_CMD[4:0]					MTP_WRITE_DNE	CRCOK	LED_OPEN

Bit Description

FIELD NAME	BITS	TYPE	POR(1)	DESCRIPTION
MTP_WRITE_CMD[4:0]	[7:3]	R/W̄	00000	Writing 10010 to this register bits automatically initiates an MTP programming cycle to register 0x00 to 0x0B. At the end of programming, this register is automatically cleared, and the MTP_WRITE_DNE read-only status bit will show '1'.
MTP_WRITE_DNE	[2]	R	0	Status bit indicating the completion of MTP programming for registers 0x00 to 0x0B. Clears upon read.
CRCOK	[1]	R	0	Status bit indicating the CHECKSUM for registers 0x00 to 0x0B is good.
LED_OPEN	[0]	R	0	Status bit to flag an open or grounded condition on any LED pin. 0 = No error 1 = One or more LED strings is grounded open

Application Schematic

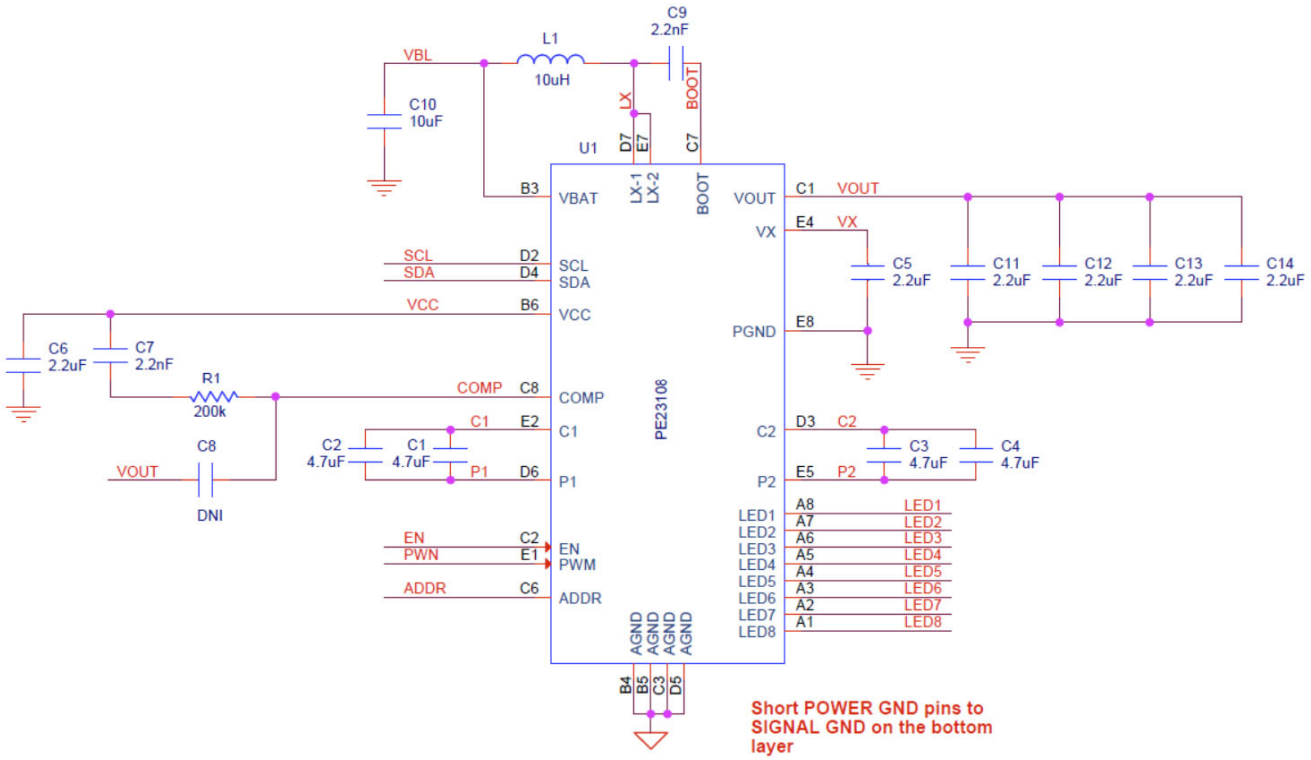


Figure 43. Detailed Application Schematic

Note: Contact factory for details of the compensation components on the COMP pin.

Application Circuit Part List[1]

COMPONENT	VALUE	PART SIZE	MANUFACTURER'S PART NUMBER
C1, C2, C3, C4 (2)	4.7 µF 35V X5R or better	0603	GRM188R6YA475KE15D
C5, C6	2.2 µF 25V X5R or better	0402	GRM155C81E225KE11D
C7 (4), C9	2.2 nF 50V X5R or better	0402	GRM155R71H222KA01D
C8 (4)	DNI	0402	
C10 (3)	10 µF 25V X5R or better	0603	GRM188R61E106MA73J
C11, C12, C13, C14 (6)	2.2 µF 50V X5R or better	0603	GRM188R61H225ME11D
L1 (5)	10 µH	3.2 mm x 2.5 mm x 1.2 mm	DFE322512F-100M
R1 (4)	200 kΩ	0201	

Notes:

1. *Components in this part list are optimized for 8P12S or higher applications. Contact Murata for optimized selection based on your application.*
2. *Quantity and value based on effective capacitance per applications. It is recommended to have a total of >0.7uF efficiency capacitance on C1/C2 pins at bias voltage.*
3. *Value may need to be adjusted based on proximity of the input source to eliminate input voltage ringing.*
4. *Please see Switching Converter Compensation section for general selection. Contact Murata for optimized selection based on your application.*
5. *See also recommended inductor values below for varying operating conditions.*
6. *Value may need to be adjusted based on loading, boost switching frequency and inductor selection to reduce output voltage ripple.*

Table 18. Application Circuit Part List

Component Selection

Users of the PE23108 should adhere closely to the parts selected for the Application Circuit Part List. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact Murata for guidance.

Efficiency Optimization

The PE23108 is designed specifically to address 2-cell and 3-cell narrow voltage DC (NVDC) platforms, and for a wide range of LED configurations. The two-stage architecture relies less on the inductor for power and voltage conversion; therefore, reduction in the physical size of the inductor has less impact on the overall conversion efficiency compared with traditional single stage architectures. This enables the use of low profile, small footprint and low-cost chip inductors versus wire-wound inductors used by traditional LED boost drivers.

Capacitors Selection

Due to component availability, size, second source requirement or other reasons causing the Application Circuit Part List cannot be followed, then use the following guideline to select appropriate capacitors for PE23108.

Charge Pump Capacitors (C1 and C2)

The effective capacitance of the capacitors used for C1 and C2 should have a minimum value of 0.7 µF and the ideal value is 1 µF. The effective capacitance should match closely between charge pump capacitors; therefore, the same capacitor cannot be used for both the first and second charge pump stages. For example, with VOUT at 40V, 20V is applied across the charge pump capacitors C1 and C2. This wide capacitance difference between C1 and C2 or lower capacitance value can lower efficiency.

If a single capacitor cannot meet the effective capacitor requirement, then two or more capacitors could parallel together to meet the effective capacitor requirement.

VX Capacitor

The VX boost convertor output capacitor should have an effective capacitance between 0.1 µF and 0.3 µF. VX voltage is approximately VOUT/2.

VCC Capacitor

The VCC should have a minimum effective capacitance of 0.5 µF. Typical VCC input voltage is 3.3V with maximum input voltage at 5.5V.

VOUT Capacitor

The VOUT LED output voltage capacitor should have a typical effective capacitance of 1 µF or higher.

Layout Example

The figures that follow show a Type-III PCB layout example using a six-layer board. Trace width and spacing is 0.1 mm/0.1 mm. Vias size is 0.2 mm hole and 0.5 mm pad.

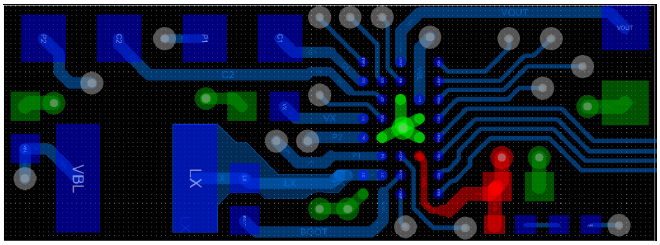


Figure 44. Top Layer

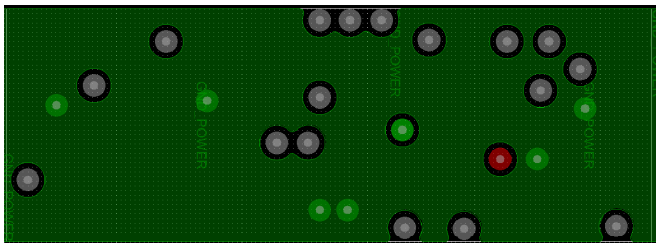


Figure 45. Layer 2

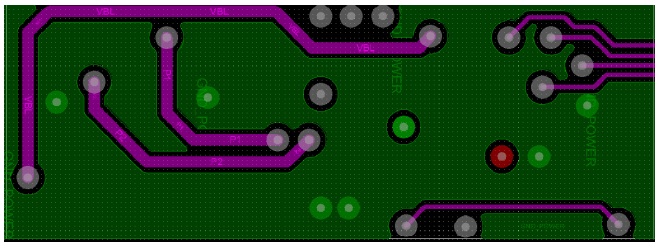


Figure 46. Layer 3

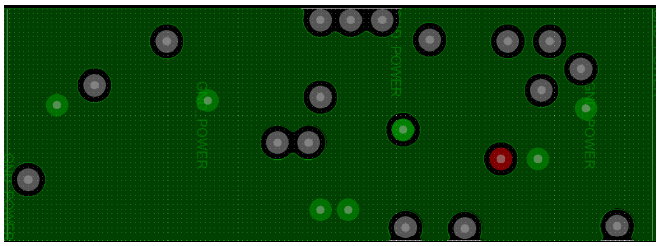


Figure 47. Bottom Layer

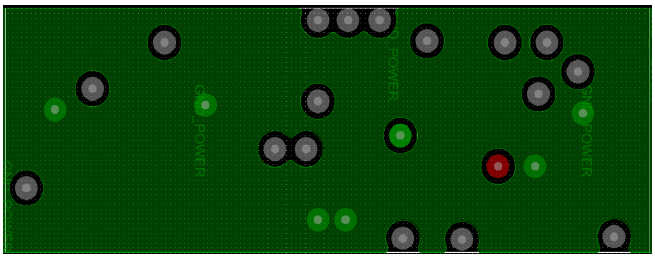


Figure 48. Layer 3

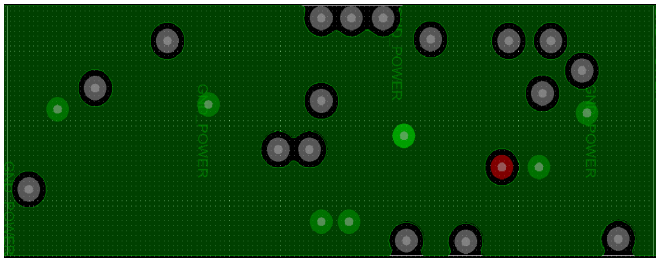


Figure 49. Bottom Layer

Package Mechanical Details

PE23108

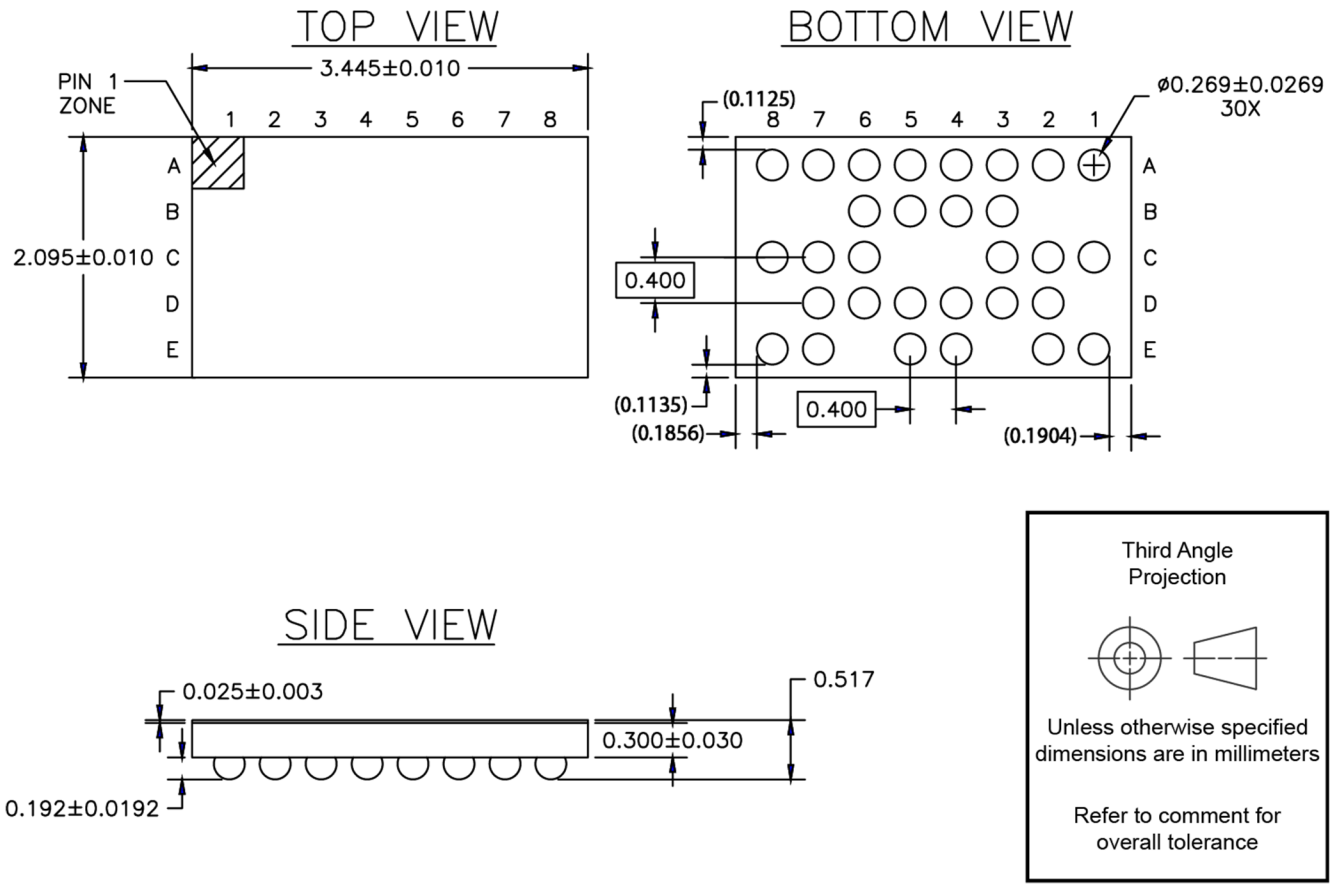


Figure 50. Package Mechanical Details for PE23108

Guidelines for PCB Land Design

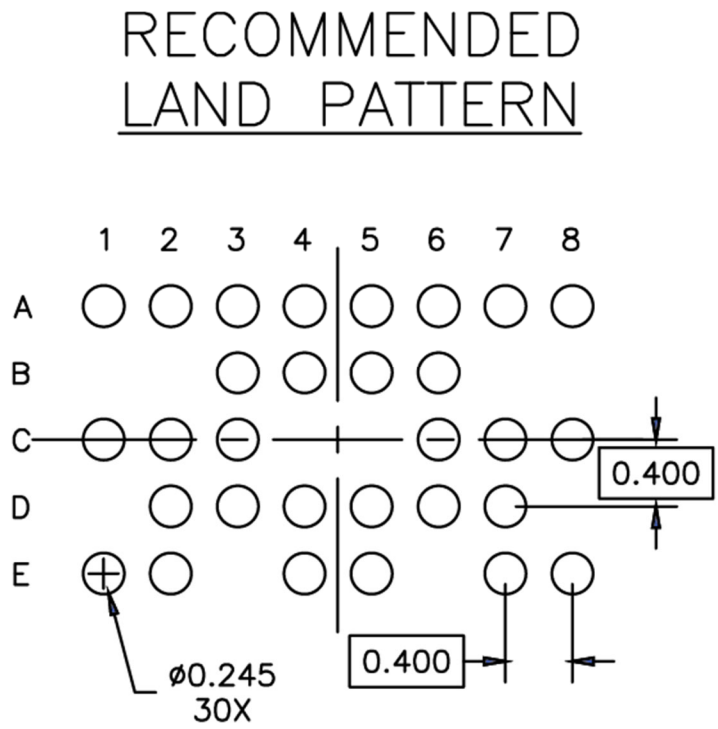
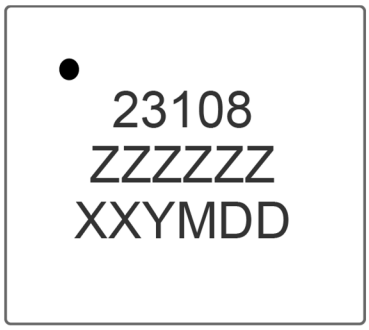


Figure 51. Recommended PCB Footprint for PE23108

The solder mask openings should be larger with a typical 0.05 mm ring all around each of the perimeter pads. The center pad is solder mask defined, with the dimensions as given above. The copper for the center pad can be extended beyond the solder mask defined pad as needed to optimize the thermal performance. Put as many thermal vias as possible in this copper. There should be no PCB Layer 1 copper under any package exposed metal, except for the center pad. All the exposed metal is dimensioned in the package mechanical details.

Top Marking Information



● = Pin 1 indicator
23108 = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
XX = Supplier code (maximum two characters)
Y = Last digit of assembly year (2022 = 2)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

Figure 52. Packaging Marking Information for PE23108

Tape and Reel Information

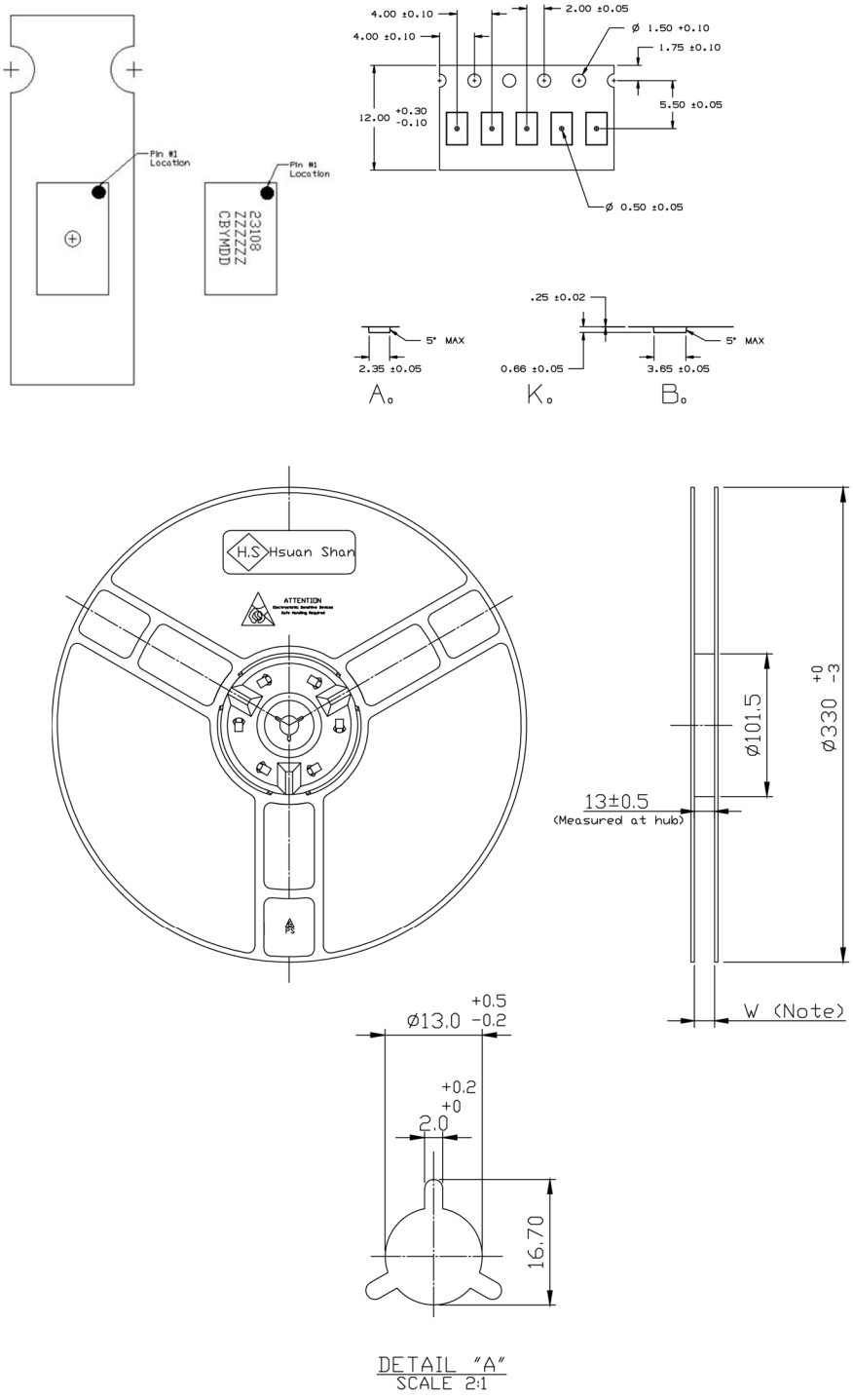


Figure 53. Tape and Reel Information for PE23108

Ordering Information

TA	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM ORDER QUANTITY
-40....+85°C	WLCSP30	PE23108A-R	30	Large tape-and-reel	5000
		PE23108A-V		Small tape-and-reel	250
		PE23108A-G		Sample waffle tray	10

Table 19: Ordering Information

Notices

⚠ CAUTION

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might lead to damage to life, body or property.

- Aircraft equipment
- Aerospace equipment
- Undersea equipment
- Power plant control equipment
- Surgical implants
- Transportation equipment (vehicles, trains, ships, etc.)
- Traffic signal equipment
- Disaster prevention / crime prevention equipment
- Application of similar complexity and/or reliability requirements to the applications listed in the above

⚠ Note

1. Please make sure that your product has been evaluated and confirmed to your specifications when our product is used in your product.
2. All the items and parameters in this approval sheet for product specification are based on the premise that our product is used for the purpose, under the condition and in the environment agreed upon between you and us. You are requested not to use our product in a manner deviating from such agreement.
3. If you have any concerns about materials other than those listed in the RoHS directive, please contact us.
4. Be sure to provide an appropriate fail-safe functionality in your product to prevent secondary damage that could be caused by the abnormal function or failure of our product.
5. Do not allow our product to be exposed to excess moisture under any circumstances.

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Murata reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Murata decides to change the specifications, Murata will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

The datasheet contains summary product information.

Sales Contact

For additional information, contact Sales at **https://www.murata.com/contactform.**

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