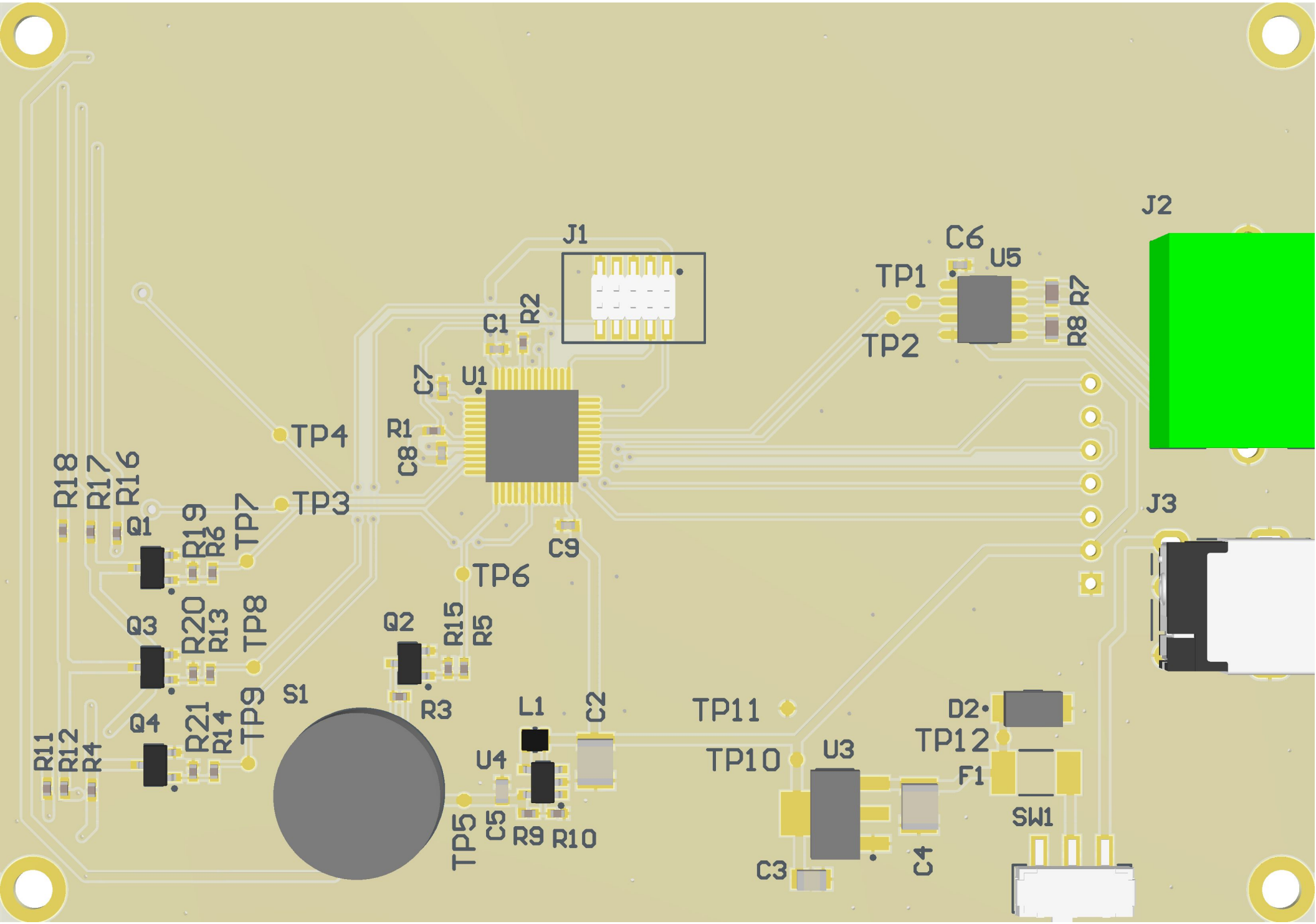
J1
J2
J3
C6
U5
TP1
TP2
R7
R8
C1
R2
C7
U1
R1
C8
TP4
TP3
R18
R17
R16
Q1
R19
R6
TP7
C9
TP6
Q3
R20
R13
TP8
Q2
R15
R5
R3
S1
TP9
Q4
R21
R14
R11
R12
R4
L1
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TP5
C5
R9
R10
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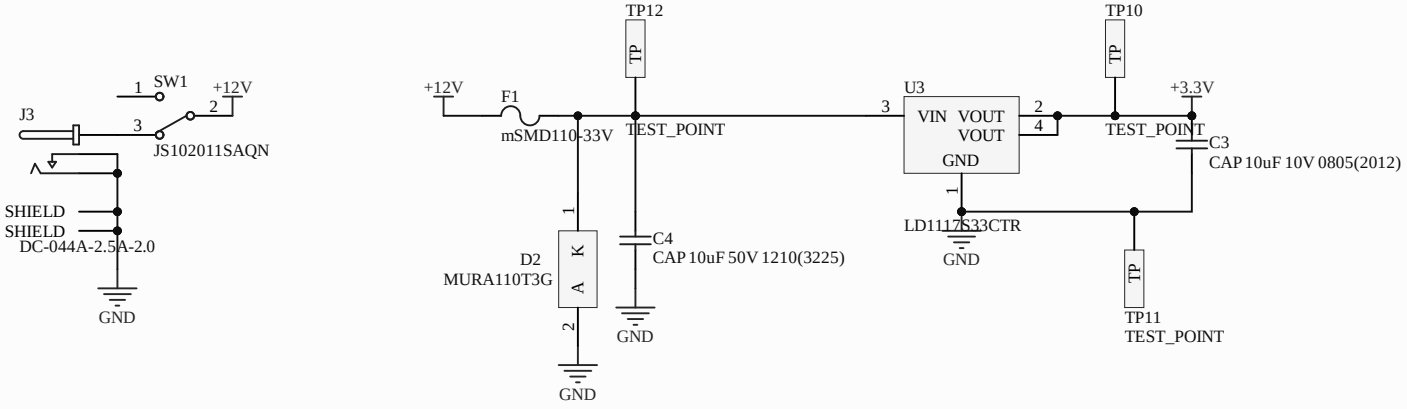
TP10
U3
D2
TP12
F1
SW1
C3
C4



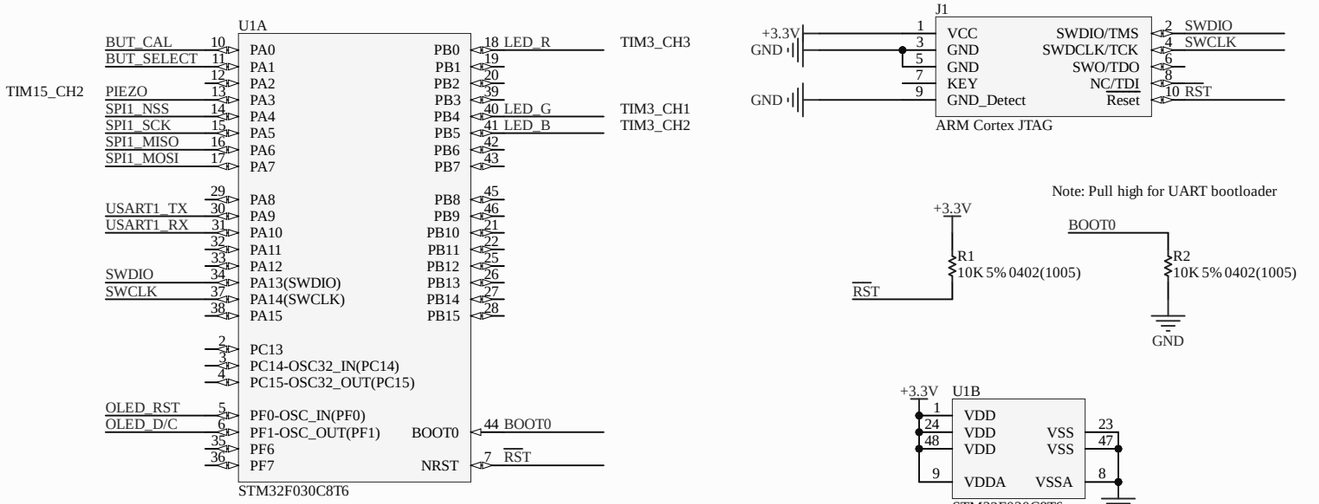
Power backup

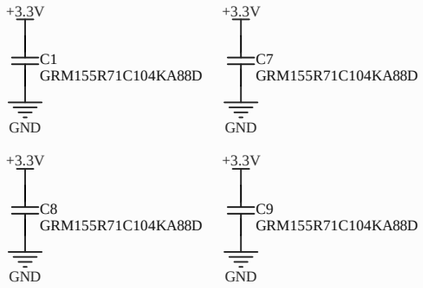
VBAT

GND

Notes:
-Device should be capable of flashing alarm for TBD seconds after power is depleted.
-Cap must stay above microcontroller brownout voltage TBD while drawing TBD current.
-Need to switch to 2xAA or similar

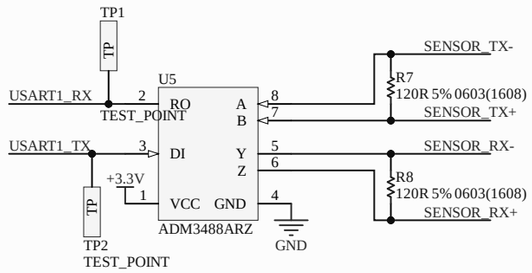
Microcontroller

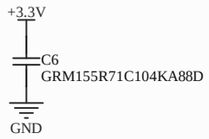


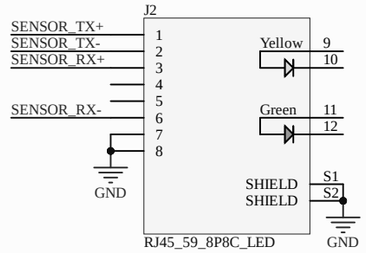


Notes:
-The specific STM32 part is generic, and could be replaced with a similar part from the F0 or F1 family.
-The microcontroller needs to sample an analog value at 200Hz, process it, and then show the results on a monochrome graphical display.
-In particular, it could be advantageous to switch to a part with a USB bootloader for easier field upgrades.

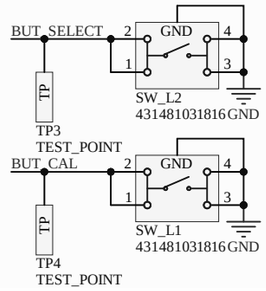
Sensor board connector







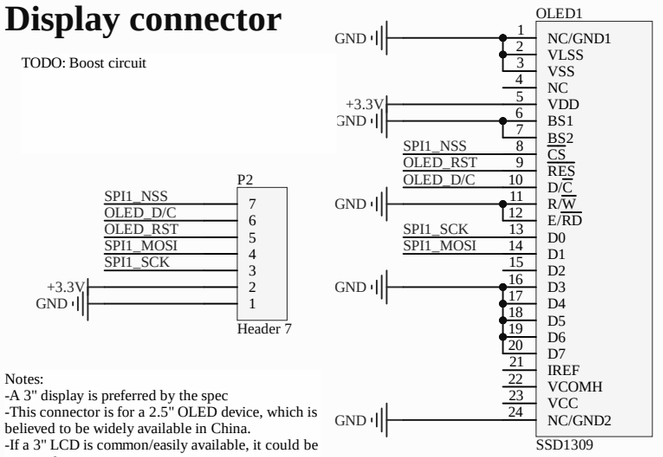
Buttons



Notes:
-This is a generic footprint, need to confirm that they integrate correctly with the mechanical design
-It would be desireable to use a sealed version if available

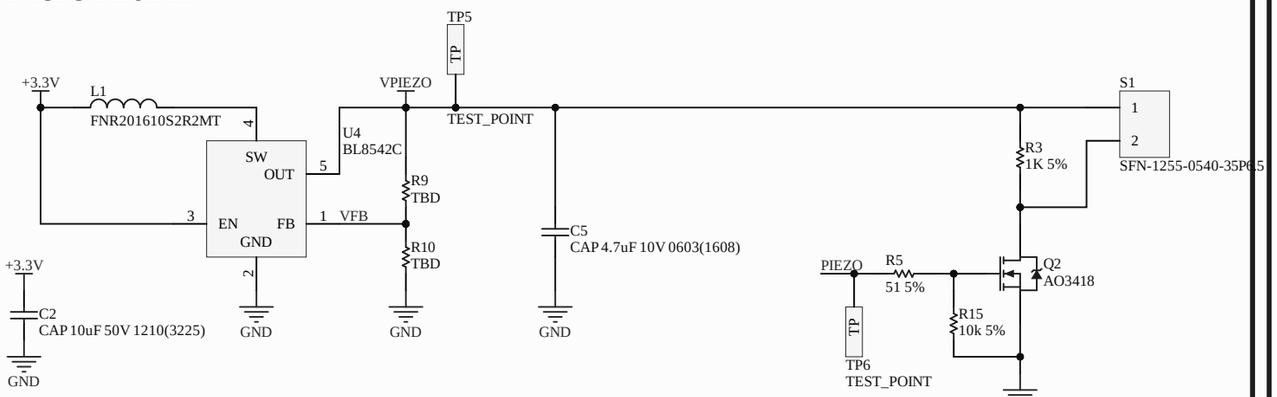
Display connector

TODO: Boost circuit



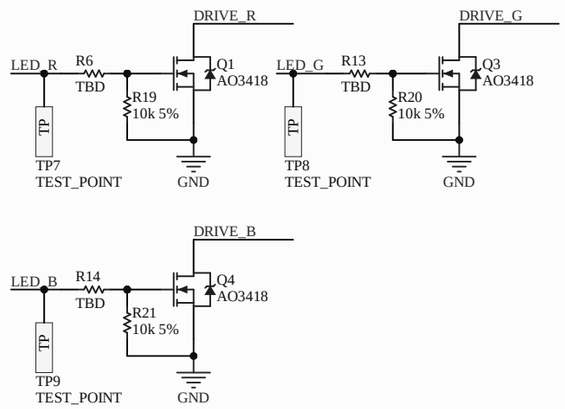
Notes:
-A 3" display is preferred by the spec
-This connector is for a 2.5" OLED device, which is believed to be widely available in China.
-If a 3" LCD is common/easily available, it could be swapped in.

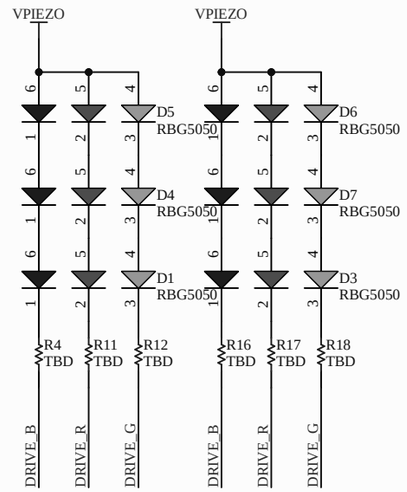
Piezo Alarm



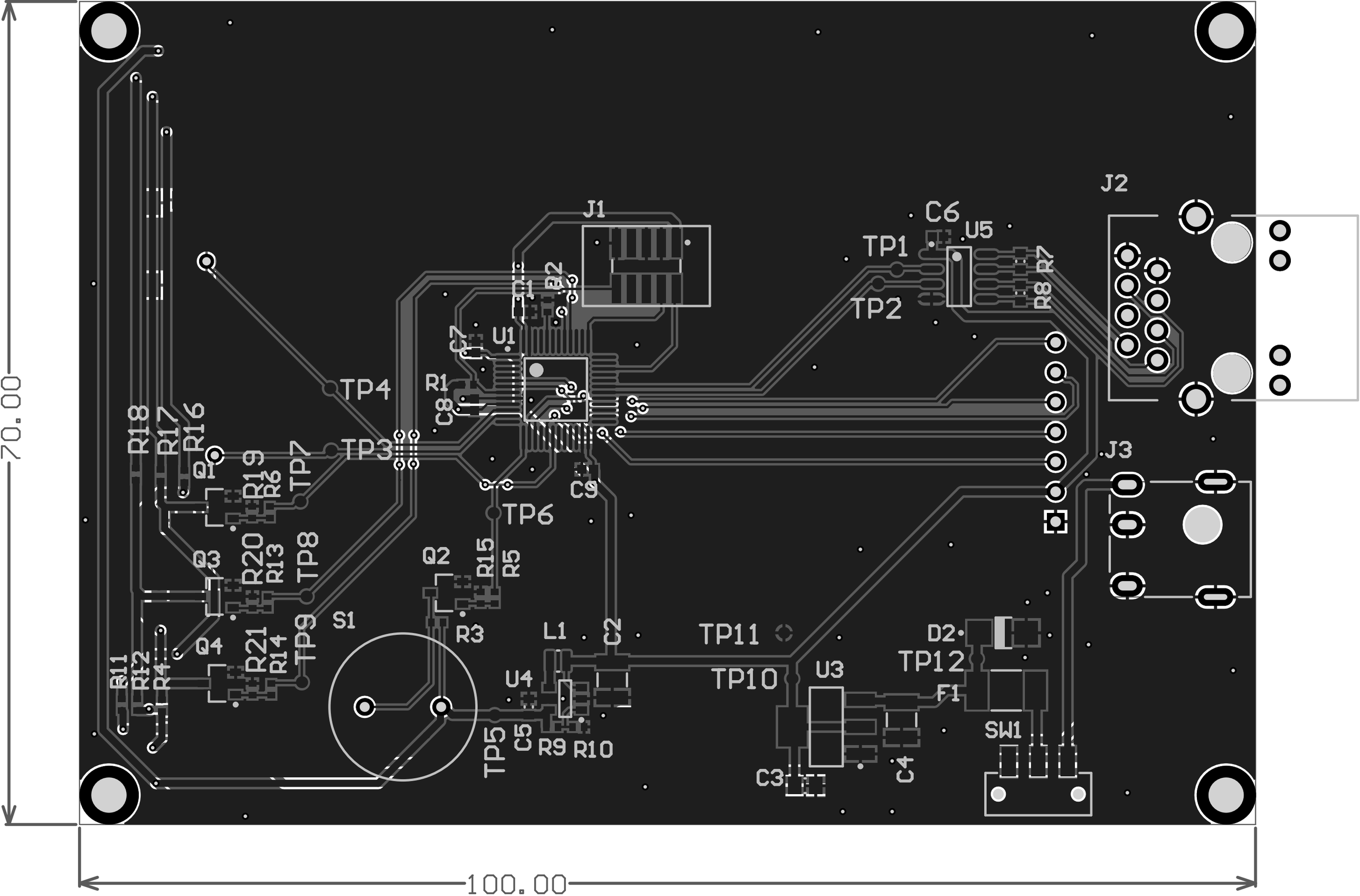
Notes:
-Need to produce drive voltage from +3.3V rail, to allow the alarm to work during a loss-of-power event.
-Peak voltage and current requirements should be adjusted based on chosen Piezo element
-Parallel resistive element R3 allows for a discharge cycle
-Drive transistor Q1 is generic

LED Alarm





Notes:
-Needs to work during a loss-of-power event


70.00
100.00
J1
J2
J3
C6
U5
TP1
TP2
R7
R8
C1
R2
C7
U1
TP4
R1
C8
R18
R17
R16
Q1
R19
R6
TP7
TP3
TP6
C9
Q3
R20
R13
TP8
Q2
R15
R5
R3
TP9
S1
Q4
R21
R14
R11
R12
R4
L1
C2
U4
TP5
C5
R9
R10
TP11
TP10
U3
D2
TP12
F1
SW1
C3
C4

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\alarm_module\pcb\PCB2.PcbDoc

Warnings 0
Rule Violations 117

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.6mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	30
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	77
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet2 (Bounding Region = (90mm, 65mm, 197mm, 135mm)	1
Room power (Bounding Region = (147mm, 61mm, 190mm, 97mm) (InComponentClass('power'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	117

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP1(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP2(2.5mm,67.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP3(97.5mm,67.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP4(97.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS1(98mm,38.37mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS2(98mm,49.5mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3mm > 2.54mm) Pad J3-MNT(95.5mm,25.5mm) on Multi-Layer Actual Hole Size = 3mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(38.29mm,43.6mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C6-1(73.49mm,50mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C7-1(33.7mm,41.09mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C8-1(33.6mm,36.19mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C9-1(42.71mm,30.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(42.9mm,8.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(32.5mm,37.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R11-1(3.6mm,10.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R12-1(4.9mm,10.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R13-1(16mm,19.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R14-1(16.3mm,12mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R15-1(34.1mm,19.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R16-1(8.9mm,29.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R17-1(6.9mm,29.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R18-1(4.8mm,29.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R19-1(14.675mm,27.075mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R20-1(14.7mm,19.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(39.8mm,43.6mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R21-1(14.7mm,12mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(29.9mm,17.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R4-1(7mm,10.6mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R5-1(35.3mm,19.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R6-1(16.175mm,27.075mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R9-1(40.7mm,8.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.133mm < 0.254mm) Between Pad U1-1(36.4mm,39.75mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.133mm < 0.254mm) Between Pad U1-12(36.4mm,34.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.133mm < 0.254mm) Between Pad U1-24(43.25mm,32.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.133mm < 0.254mm) Between Pad U1-36(44.6mm,39.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(42.675mm,9.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(42.675mm,10.7mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Arc (42.675mm,8.9mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.035mm < 0.254mm) Between Arc (72.45mm,49.355mm) on Top Overlay An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(62.6mm,3.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C3-1(62.6mm,3.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(60.8mm,3.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(60.8mm,3.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-1(38.2mm,10.7mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad C5-1(38.2mm,10.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(38.2mm,9.3mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(38.2mm,9.3mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-1(7.683mm,6.517mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-3(7.683mm,9.717mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D1-4(12.083mm,9.717mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D1-6(12.083mm,6.517mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D3-1(7.8mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D3-3(7.8mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D3-4(12.2mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D3-6(12.2mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D4-1(47.8mm,6.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D4-3(47.8mm,9.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D4-4(52.2mm,9.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D4-6(52.2mm,6.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D5-1(87.8mm,6.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D5-3(87.8mm,9.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D5-4(92.2mm,9.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D5-6(92.2mm,6.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D6-1(87.8mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D6-3(87.8mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D6-4(92.2mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D6-6(92.2mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D7-1(47.8mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D7-3(47.8mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D7-4(52.2mm,63.6mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad D7-6(52.2mm,60.4mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad F1-2(76.31mm,11.4mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(50.74mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-1(50.74mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(45.66mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(45.66mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(50.74mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(50.74mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(49.47mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(49.47mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(48.2mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(48.2mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(46.93mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(46.93mm,45.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(45.66mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(45.66mm,49.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(41.4mm,13.9mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(41.4mm,13.9mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad L1-2(40mm,13.9mm) on Top Layer And Trac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad L1-2(40mm,13.9mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-1(80mm,47.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-1(80mm,47.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-2(80mm,48.6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R7-2(80mm,48.6mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-1(80mm,45.9mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R8-1(80mm,45.9mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-2(80mm,44.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-2(80mm,44.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L1-1(10.75mm,45.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L1-2(10.75mm,52.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L1-3(6.25mm,45.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-4(6.25mm,52.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(8.5mm,53.125mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(8.5mm,53.125mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L2-1(11.25mm,18.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L2-2(11.25mm,25.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L2-3(6.75mm,18.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-4(6.75mm,25.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(9mm,26.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(9mm,26.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-1(66.4mm,6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-2(66.4mm,8.3mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-3(66.4mm,10.6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-4(60.6mm,8.3mm) on Top Layer And Trac

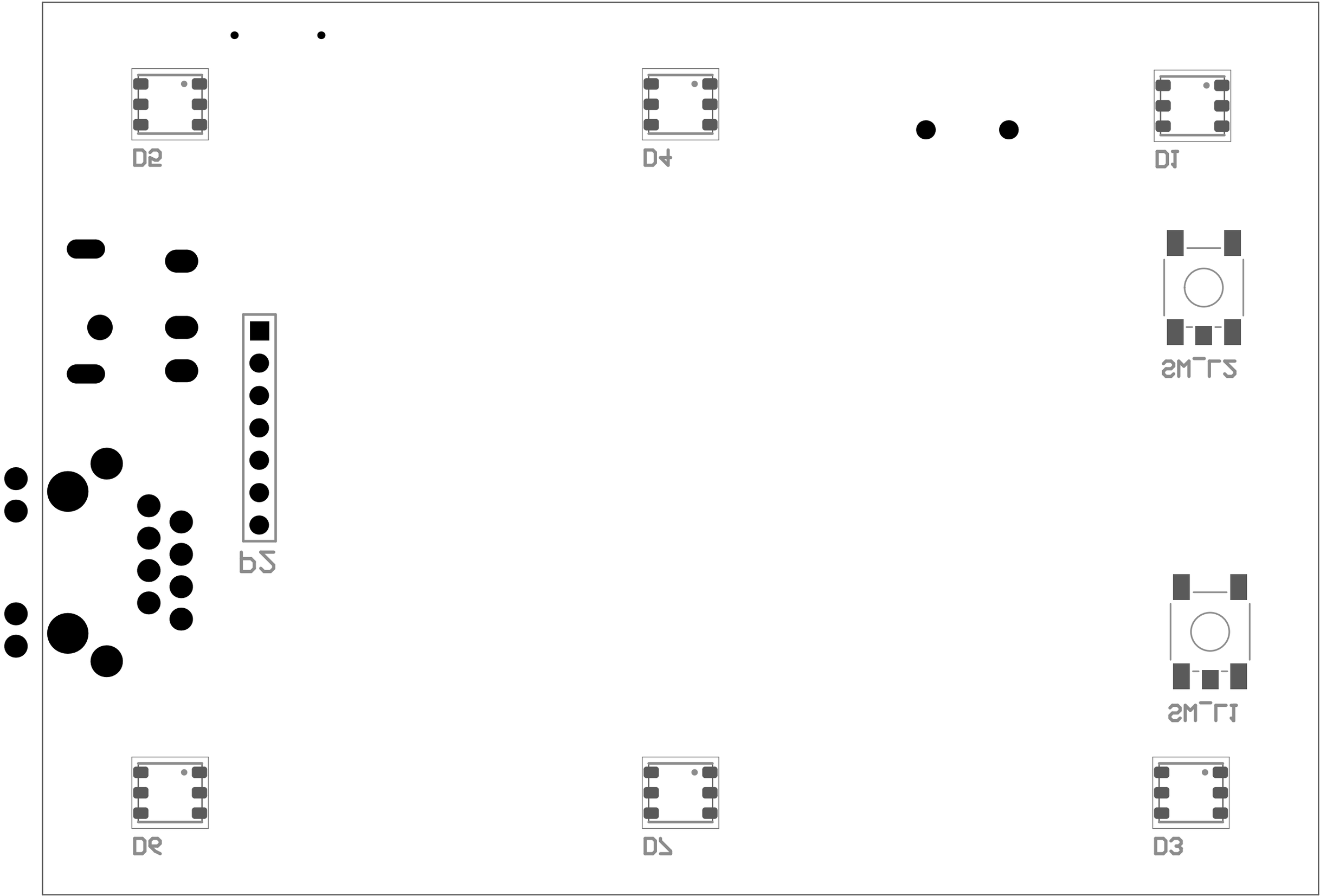
Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.182mm < 0.254mm) Between Arc (36.4mm,40.45mm) on Top Overlay And Text "U1
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R19" (15.537mm,27.871mm) on Top Overlay An

Room Sheet2 (Bounding Region = (90mm, 65mm, 197mm, 135mm) (InComponentClass('Sheet2'))
Room Definition: Between Component J2-RJ45_59_8P8C_LED (98mm,43.935mm) on Top Layer And Room Sheet2

Electrical Rules Check Report

Class	Document	Message
Error	Sheet2.SchDoc	Net SPI1_MISO has only one pin (Pin U1-16)
Warning	power.SchDoc	Floating Power Object GND at (1000mil,1400mil)
Warning	power.SchDoc	Floating Power Object VBAT at (1000mil,1900mil)
Warning	Sheet2.SchDoc	Footprint of component Component OLED1 SSD1309 cannot be found
Warning	Sheet2.SchDoc	Net BOOT0 has no driving source (Pin R2-1, Pin U1-44)
Warning	Sheet2.SchDoc	Net SENSOR_TX+ has no driving source (Pin J2-1, Pin R7-1, Pin U5-7)
Warning	Sheet2.SchDoc	Net SENSOR_TX- has no driving source (Pin J2-2, Pin R7-2, Pin U5-8)

J1
C1
R2
C7
U1
R1
C8
TP4
R18
R17
R16
Q1
R19
R6
TP7
TP3
C9
TP6
Q3
R20
R13
TP8
Q2
R15
R5
S1
R3
L1
C2
R11
R12
R4
Q4
R21
R14
TP9
U4
C5
R9
R10
TP5
TP11
TP10
U3
C3
C4
D2
TP12
F1
SW1
TP1
TP2
C6
U5
R8
R7
J2
J3


D5
D4
D1
SW_TZ
J4
SW_T1
D6
D2
D3