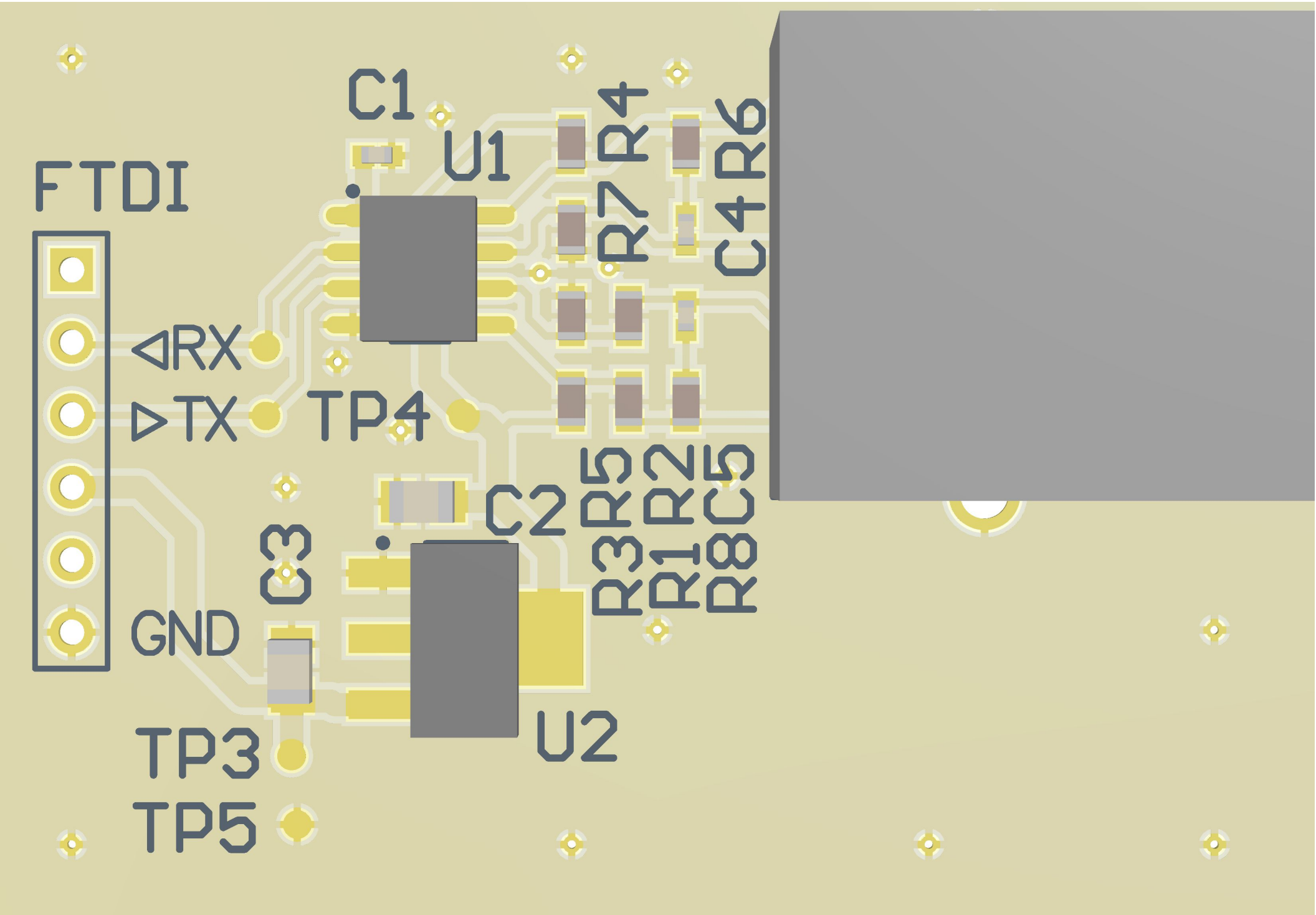
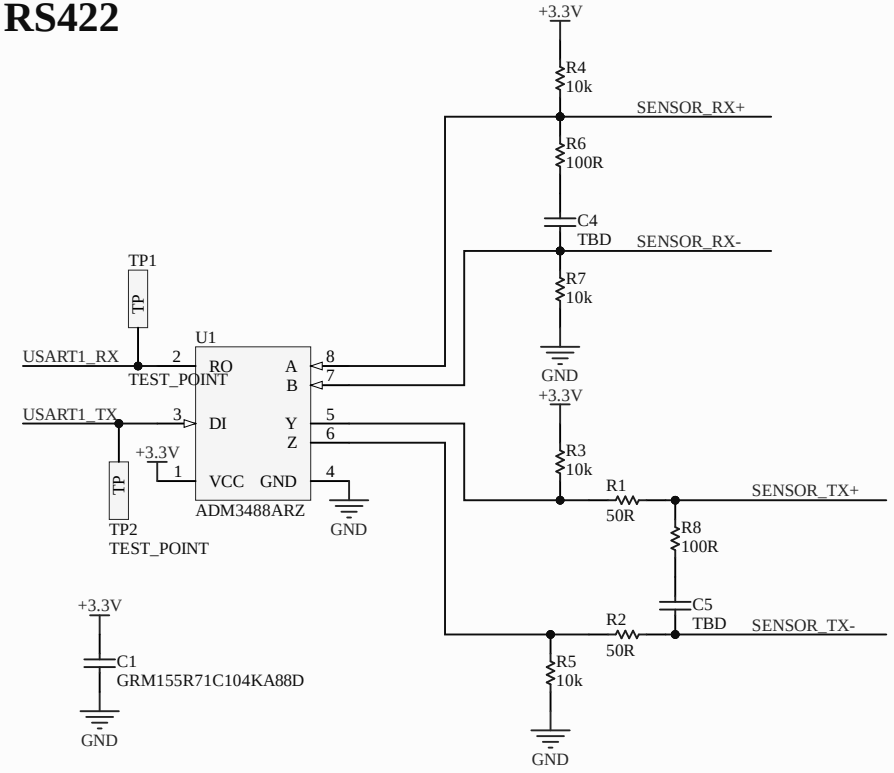
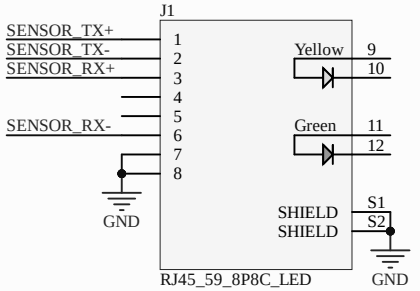

C1
U1
FTDI
R4
R7
R6
C4
RX
TX
TP4
C2
R5
R2
C5
C3
R3
R1
R8
GND
U2
TP3
TP5

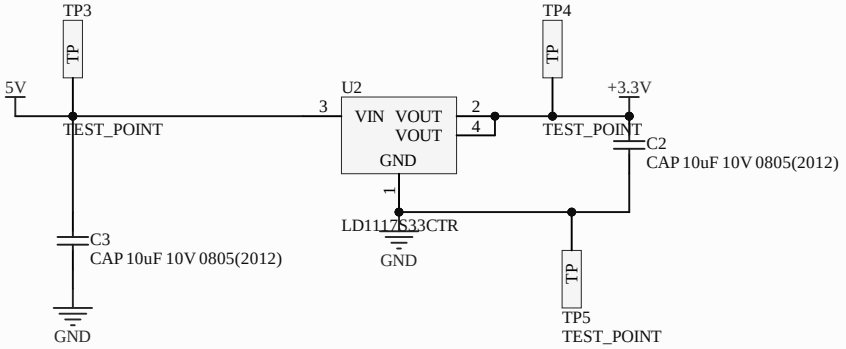
RS422



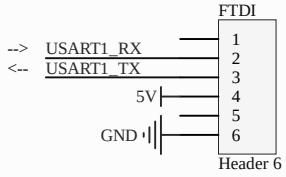


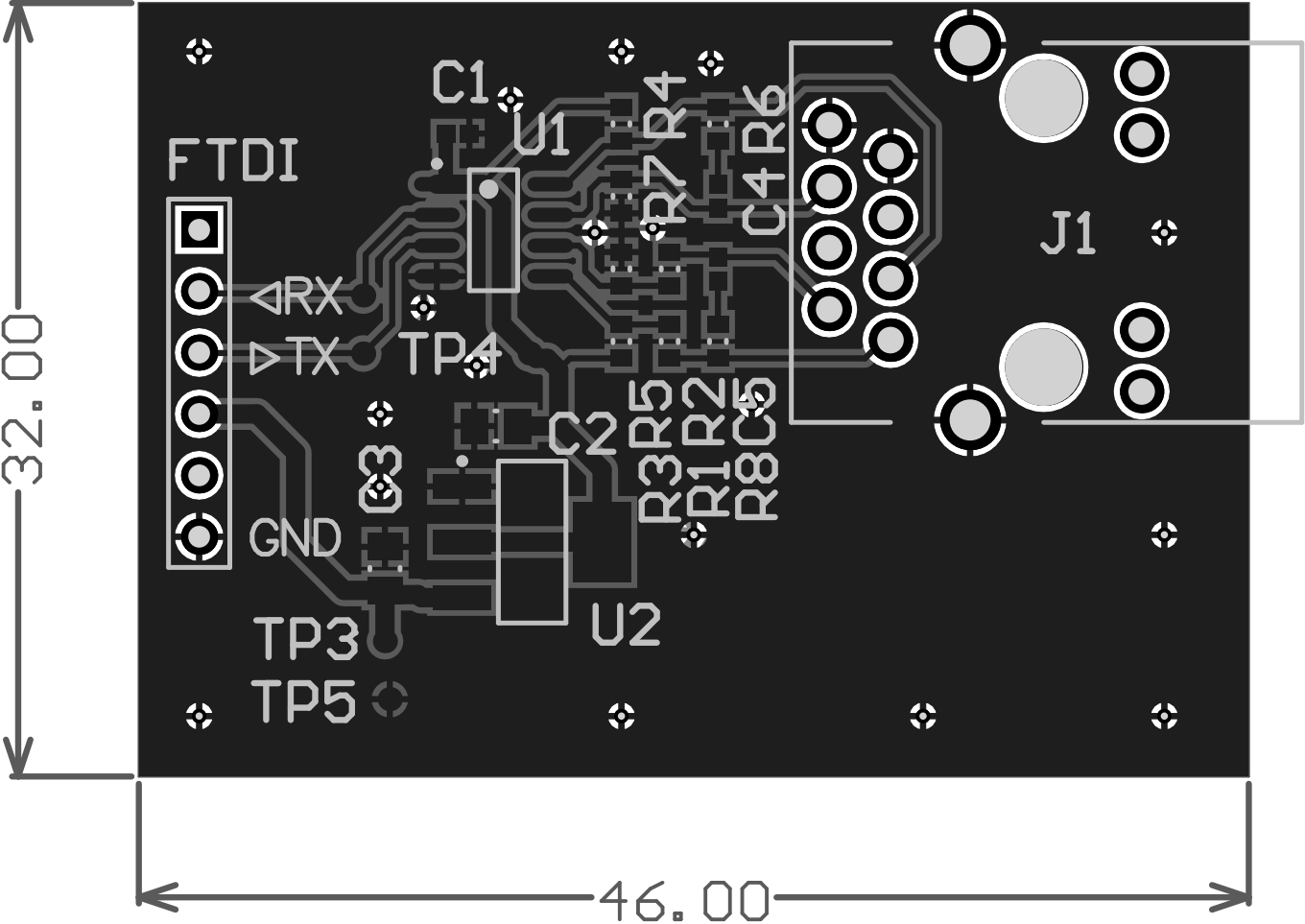
Note:
-Multiple termination topologies possible:
-Populate R3,R5 for pullup/down protection
-Populate R1,R2 for series termination
-Populate R4,C4 for AC termination, or short C4 for parallel termination

Power



FTDI




C1
U1
R4
R7
C4
R6
FTDI
J1
RX
TX
TP4
C2
R5
R2
R3
R1
C5
R8
C3
GND
TP3
U2
TP5
32.00
46.00

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Project\PCB\alarm_module\alarm_to_uart\alarm

Warnings 0
Rule Violations 63

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	3
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.8mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	2
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	6
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	44
Silk to Silk (Clearance=0.254mm) (All),(All)	8
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet4 (Bounding Region = (105mm, 83mm, 171mm, 135mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	63

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(128.7mm,121.6mm) on Top Layer And Pac
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C4-1(139mm,118.51mm) on Top Layer And Pac
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C5-1(139mm,116.49mm) on Top Layer And Pac

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS1(152.5mm,111.935mm) on Multi-Layer Actual Hole Size = 3.2mn
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS2(152.5mm,123.065mm) on Multi-Layer Actual Hole Size = 3.2mn

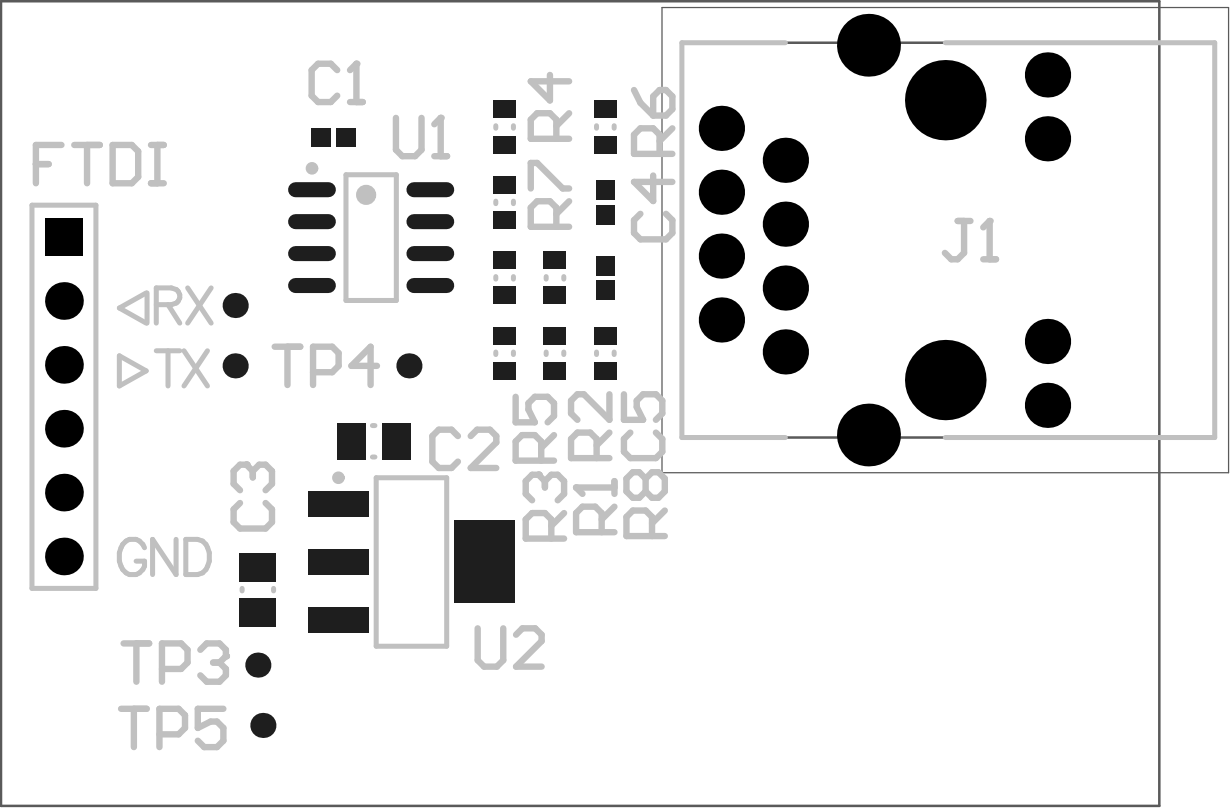
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(128.7mm,121.6mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(139mm,118.51mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C5-1(139mm,116.49mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.167mm < 0.254mm) Between Pad R2-1(137mm,116.7mm) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad R5-2(135mm,116.7mm) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad R7-2(135mm,118.3mm) on Top Layer And Via

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(128.9mm,109.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(128.9mm,109.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(130.7mm,109.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-2(130.7mm,109.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(125.2mm,104.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C3-1(125.2mm,104.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(125.2mm,102.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(125.2mm,102.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(137mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(137mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(137mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R1-2(137mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-1(137mm,116.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R2-1(137mm,116.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(137mm,115.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(137mm,115.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-1(135mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-1(135mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-2(135mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R3-2(135mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-1(135mm,122.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R4-1(135mm,122.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-2(135mm,121.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-2(135mm,121.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-1(135mm,115.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-1(135mm,115.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-2(135mm,116.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R5-2(135mm,116.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-1(139mm,122.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R6-1(139mm,122.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-2(139mm,121.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-2(139mm,121.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-1(135mm,119.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R7-1(135mm,119.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-2(135mm,118.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-2(135mm,118.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-1(139mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-1(139mm,112.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-2(139mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R8-2(139mm,113.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-1(128.4mm,107mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-2(128.4mm,104.7mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-3(128.4mm,102.4mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-4(134.2mm,104.7mm) on Top Layer An

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "<RX" (119.5mm,114mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text ">TX" (119.5mm,111.5mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (0.161mm < 0.254mm) Between Text "C2" (132.13mm,108.438mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.161mm < 0.254mm) Between Text "C2" (132.13mm,108.438mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.151mm < 0.254mm) Between Text "C4" (141.662mm,117.53mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "R1" (139.362mm,105.884mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "R1" (139.362mm,105.884mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.151mm < 0.254mm) Between Text "R6" (141.662mm,120.93mm) on Top Overlay An

Electrical Rules Check Report

Class	Document	Message
Warning	alarm_to_uart.SchDoc	Net SENSOR_RX+ has no driving source (Pin J1-3, Pin R4-2, Pin R6-1, Pin U1-8)
Warning	alarm_to_uart.SchDoc	Net SENSOR_RX- has no driving source (Pin C4-1, Pin J1-6, Pin R7-1, Pin U1-7)
Warning	alarm_to_uart.SchDoc	Net USART1_TX has no driving source (Pin FTDI-3, Pin TP2-1, Pin U1-3)


C1
U1
R4
R7
C4
R6
FTDI
J1
RX
TX
TP4
C2
R3
R5
R1
R2
R8
C5
C3
GND
U2
TP3
TP5

Alarm Board
Comms
2020-04-14
RevB