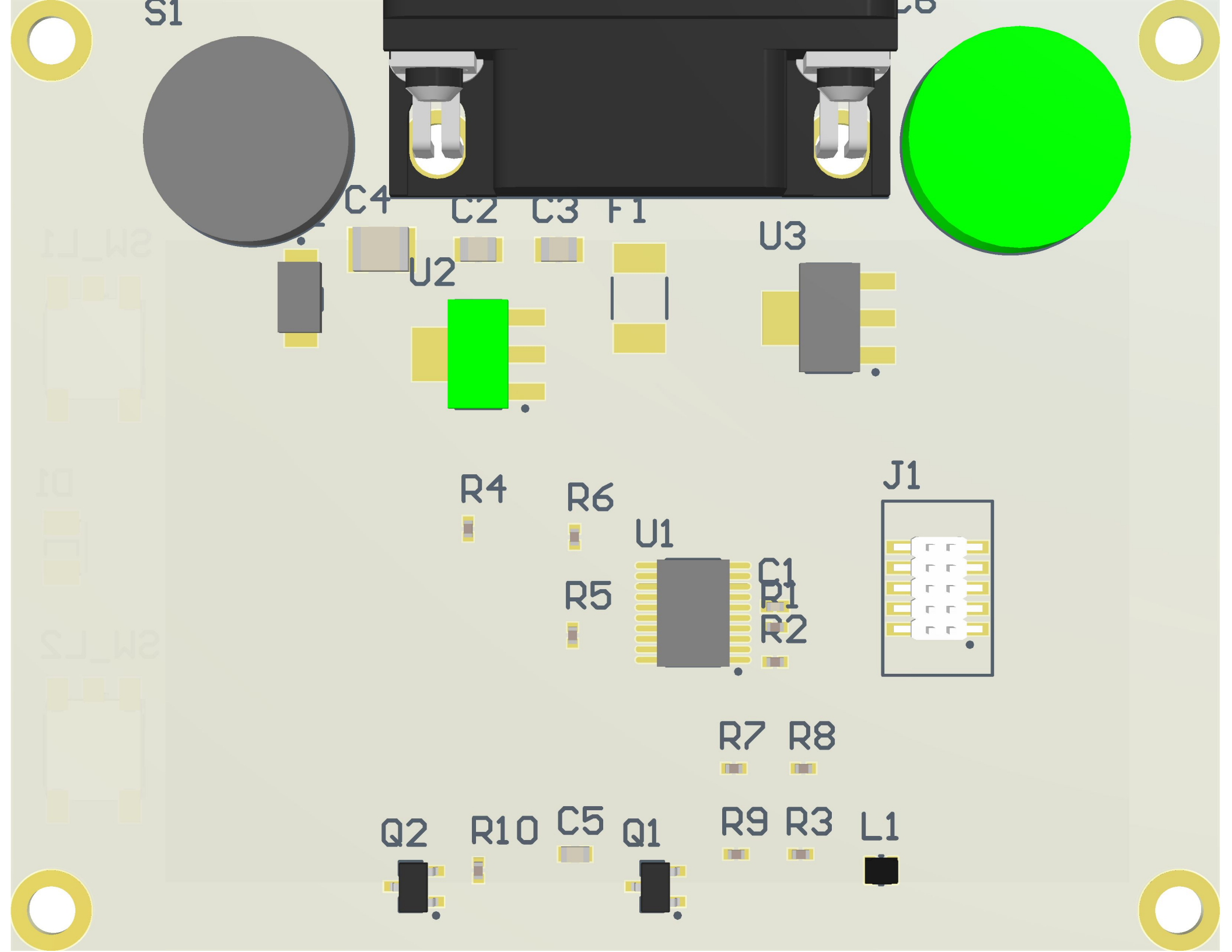
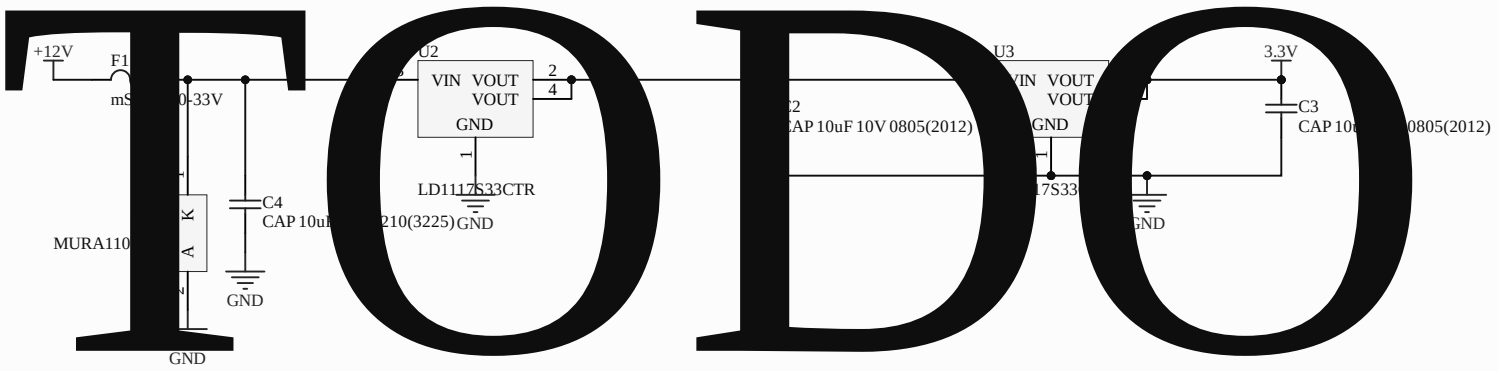
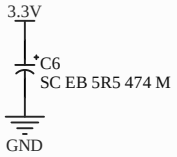

S1
C6
C4
C2
C3
F1
U3
U2
R4
R6
U1
J1
C1
R5
R1
R2
R7
R8
Q2
R10
C5
Q1
R9
R3
L1

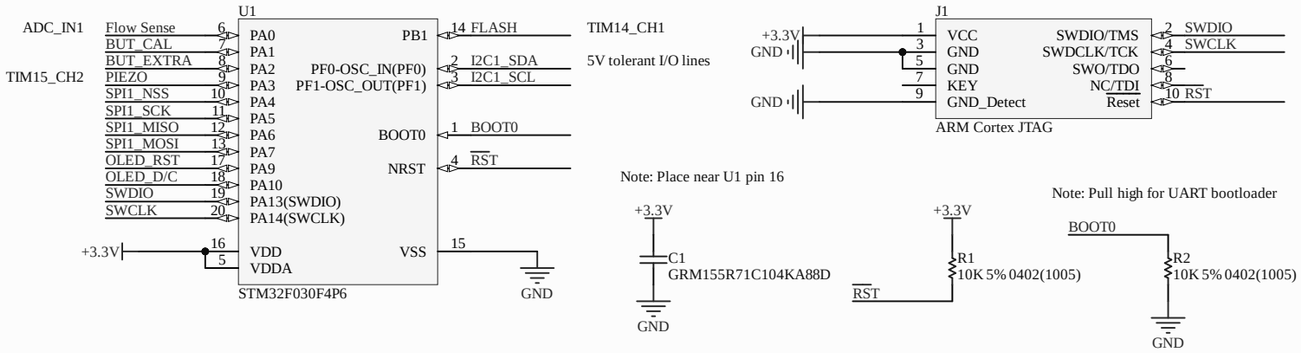


Supercap power backup



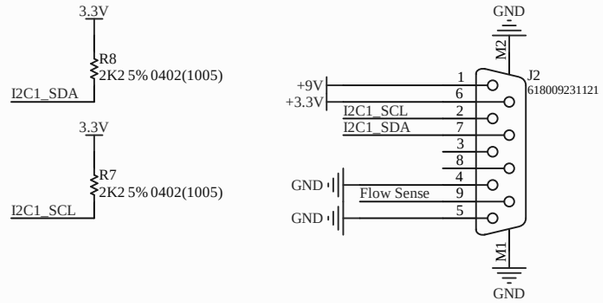
Notes:
-Device should be capable of flashing alarm for TBD seconds after power is depleted.
-Cap must stay above microcontroller brownout voltage TBD while drawing TBD current.

Microcontroller

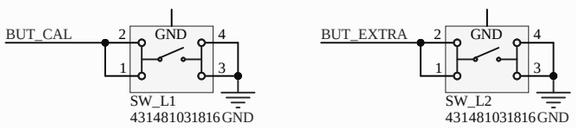


Notes:
-The specific STM32 part is generic, and could be replaced with a similar part from the F0 or F1 family.
-The microcontroller needs to sample an analog value at 200Hz, process it, and then show the results on a monochrome graphical display.
-In particular, it could be advantageous to switch to a part with a USB bootloader for easier field upgrades.

Sensor board connector



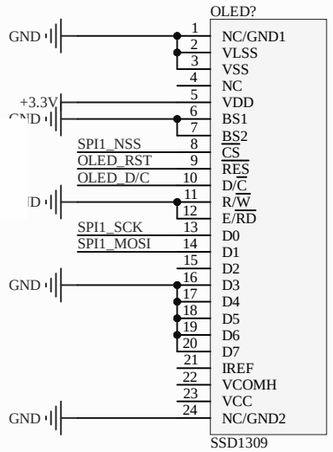
Buttons



Notes:
-This is a generic footprint, need to confirm that they integrate correctly with the mechanical design
-It would be desireable to use a sealed version if available

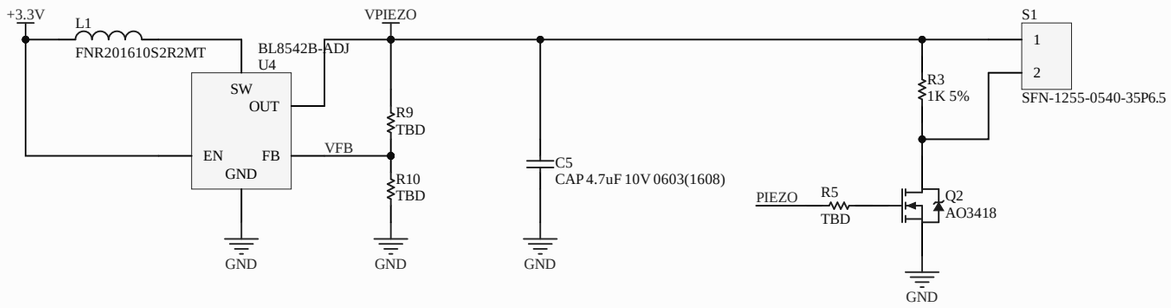
Display connector

TODO: Boost circuit



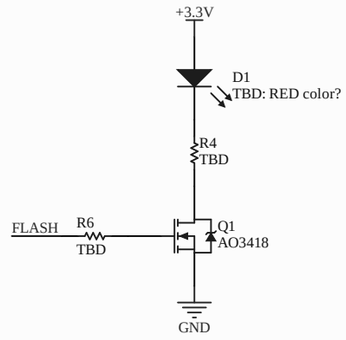
Notes:
-A 3" display is preferred by the spec
-This connector is for a 2.5" OLED device, which is believed to be widely available in China.
-If a 3" LCD is common/easily available, it could be swapped in.

Piezo Alarm

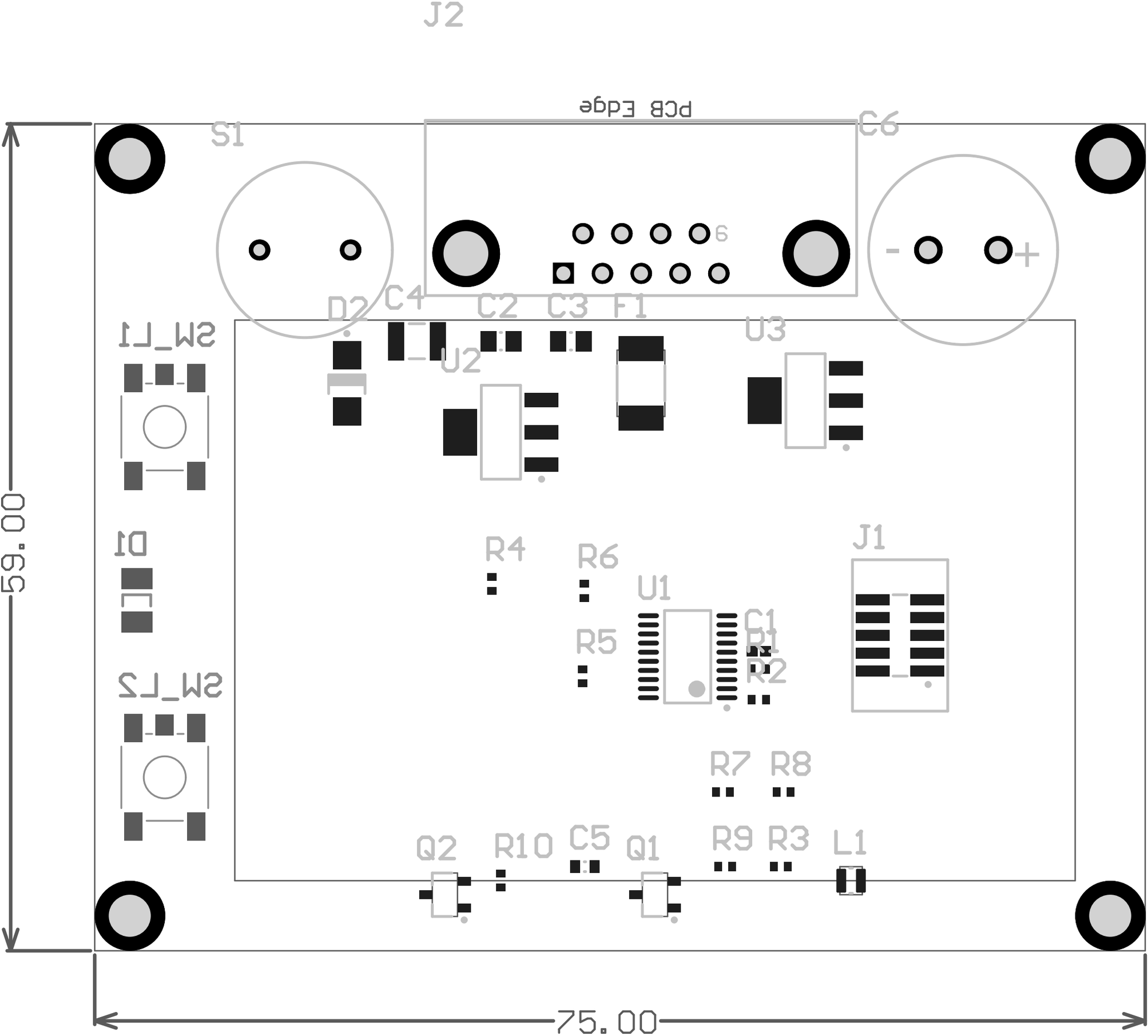


Notes:
-Need to produce drive voltage from +3.3V rail, to allow the alarm to work during a loss-of-power event.
-Peak voltage and current requirements should be adjusted based on chosen Piezo element
-Parallel resistive element R3 allows for a discharge cycle
-Drive transistor Q1 is generic

LED Alarm



Notes:
-Can be powered directly from +3.3V
-Needs to work during a loss-of-power event


J2
PCB Edge
S1
C6
D2
C4
C2
C3
F1
U2
U3
SW_PB1
D1
SW_PB2
R4
R6
U1
R5
C1
R1
R2
J1
R7
R8
Q2
R10
C5
Q1
R9
R3
L1
59.00
75.00

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\alarm_module\pcb\PCB2.PcbDoc

Warnings 2
Rule Violations 176

Warnings	
Unplated multi-layer pad(s) detected	2
Total	2

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	69
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	6
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	29
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	59
Silk to Silk (Clearance=0.254mm) (All),(All)	10
Net Antennae (Tolerance=0mm) (All)	0
Room power (Bounding Region = (106mm, 100.49mm, 151mm, 113.49mm)	2
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	176

Unplated multi-layer pad(s) detected
Pad S1-2(18.25mm,50mm) on Multi-Layer on Net NetQ2_3
Pad S1-1(11.75mm,50mm) on Multi-Layer on Net VPIEZO

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(47.904mm,21.36mm) on Top Layer And Pac

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint:
Un-Routed Net Constraint:
Un-Routed Net Constraint: Net GND Between Pad C1-1(47.904mm,21.36mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad C1-1(47.904mm,21.36mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U1-15(39.534mm,21.304mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad C1-2(46.924mm,21.36mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U1-5(45.134mm,20.654mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad C2-1(29.9mm,43.49mm) on Top Layer And Pad C3-1(34.9mm,43.49mm
Un-Routed Net Constraint: Net GND Between Pad C4-1(24.5mm,43.49mm) on Top Layer And Pad C2-1(29.9mm,43.49mm
Un-Routed Net Constraint: Net GND Between Pad C2-1(29.9mm,43.49mm) on Top Layer And Pad U2-1(31.9mm,34.7mm) or
Un-Routed Net Constraint: Net 9V Between Pad U2-4(26.1mm,37mm) on Top Layer And Pad C2-2(28.1mm,43.49mm) on To
Un-Routed Net Constraint: Net GND Between Pad C3-1(34.9mm,43.49mm) on Top Layer And Pad J2-4(41.77mm,48.33mm
Un-Routed Net Constraint: Net 3.3V Between Pad C3-2(33.1mm,43.49mm) on Top Layer And Pad U3-4(47.85mm,39.25mm
Un-Routed Net Constraint: Net GND Between Pad D2-2(18mm,38.49mm) on Top Layer And Pad C4-1(24.5mm,43.49mm) or
Un-Routed Net Constraint: Net GND Between Pad C4-1(24.5mm,43.49mm) on Top Layer And Pad J2-M2(26.5mm,49.75mm
Un-Routed Net Constraint: Net NetC4_2 Between Pad D2-1(18mm,42.49mm) on Top Layer And Pad C4-2(21.5mm,43.49mm
Un-Routed Net Constraint: Net NetC4_2 Between Pad C4-2(21.5mm,43.49mm) on Top Layer And Pad U2-3(31.9mm,39.3mm
Un-Routed Net Constraint: Net GND Between Pad C5-1(35.7mm,6mm) on Top Layer And Pad Q1-2(41.375mm,4.95mm) or
Un-Routed Net Constraint: Net GND Between Pad R10-1(29mm,5.5mm) on Top Layer And Pad C5-1(35.7mm,6mm) on To
Un-Routed Net Constraint: Pad C5-2(34.3mm,6mm) on Top Layer
Un-Routed Net Constraint: Net VPIEZO Between Pad C5-2(34.3mm,6mm) on Top Layer And Pad R9-2(44.5mm,6mm) on To
Un-Routed Net Constraint: Net 3.3V Between Pad U3-2(53.65mm,39.25mm) on Top Layer And Pad C6-1(64.5mm,50mm) or
Un-Routed Net Constraint: Net GND Between Pad J2-M1(51.5mm,49.75mm) on Multi-Layer And Pad C6-2(59.5mm,50mm) or
Un-Routed Net Constraint: Net +3.3V Between Pad D1-1(3mm,23.45mm) on Bottom Layer And Pad
Un-Routed Net Constraint: Net NetD1_2 Between Pad D1-2(3mm,26.55mm) on Bottom Layer And Pad
Un-Routed Net Constraint: Net GND Between Pad SW_L1-4(2.75mm,40.875mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net NetC4_2 Between Pad U2-3(31.9mm,39.3mm) on Top Layer And Pad F1-2(39mm,38mm) or
Un-Routed Net Constraint: Net +3.3V Between Pad L1-1(54.7mm,5mm) on Top Layer And Pad J1-1(59.45mm,19.96mm) or
Un-Routed Net Constraint: Net +3.3V Between Pad R1-1(47.914mm,20.09mm) on Top Layer And Pac
Un-Routed Net Constraint: Net \R\S\T Between Pad R1-2(46.914mm,20.09mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SWDIO Between Pad U1-19(39.534mm,18.704mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J1-3(59.45mm,21.23mm) on Top Layer And Pad J1-5(59.45mm,22.5mm
Un-Routed Net Constraint: Net SWCLK Between Pad U1-20(39.534mm,18.054mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J1-5(59.45mm,22.5mm) on Top Layer And Pad J1-9(59.45mm,25.04mm
Un-Routed Net Constraint: Net GND Between Pad U3-1(53.65mm,36.95mm) on Top Layer And Pad J1-9(59.45mm,25.04mm
Un-Routed Net Constraint: Net I2C1_SCL Between Pad J2-2(36.23mm,48.33mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J2-4(41.77mm,48.33mm) on Multi-Layer And Pad J2-5(44.54mm,48.33mm
Un-Routed Net Constraint: Net GND Between Pad J2-5(44.54mm,48.33mm) on Multi-Layer And Pad
Un-Routed Net Constraint: Net +3.3V Between Pad J2-6(34.845mm,51.17mm) on Multi-Layer And Pad
Un-Routed Net Constraint: Net I2C1_SDA Between Pad J2-7(37.615mm,51.17mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net Flow Sense Between Pad J2-9(43.155mm,51.17mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J2-M1(51.5mm,49.75mm) on Multi-Layer And Pad
Un-Routed Net Constraint: Net NetQ1_1 Between Pad R6-2(34.968mm,25.178mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U1-15(39.534mm,21.304mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetQ1_3 Between Pad R4-1(28.364mm,26.686mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad Q2-2(26.375mm,4.95mm) on Top Layer And Pad R10-1(29mm,5.5mm) or
Un-Routed Net Constraint: Pad Q2-3(23.625mm,4mm) on Top Layer
Un-Routed Net Constraint: Net NetQ2_3 Between Pad Q2-3(23.625mm,4mm) on Top Layer And Pad R3-1(49.5mm,6mm) or
Un-Routed Net Constraint: Net VFB Between Pad R10-2(29mm,4.5mm) on Top Layer And Pad R9-1(45.5mm,6mm) on To
Un-Routed Net Constraint: Net \R\S\T Between Pad U1-4(45.134mm,20.004mm) on Top Layer And Pac
Un-Routed Net Constraint: Net BOOT0 Between Pad U1-1(45.134mm,18.054mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VPIEZO Between Pad R9-2(44.5mm,6mm) on Top Layer And Pad R3-2(48.5mm,6mm) on To

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net PIEZO Between Pad R5-1(34.841mm,20.082mm) on Top Layer And Pac
Un-Routed Net Constraint: Net FLASH Between Pad R6-1(34.968mm,26.178mm) on Top Layer And Pac
Un-Routed Net Constraint: Net I2C1_SCL Between Pad U1-3(45.134mm,19.354mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad R7-2(44.358mm,11.322mm) on Top Layer And Pac
Un-Routed Net Constraint: Net I2C1_SDA Between Pad U1-2(45.134mm,18.704mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U3-4(47.85mm,39.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net BUT_CAL Between Pad SW_L1-1(7.25mm,33.875mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net BUT_CAL Between Pad SW_L1-1(7.25mm,33.875mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net GND Between Pad SW_L1-3(2.75mm,33.875mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net GND Between Pad SW_L2-4(2.75mm,15.875mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net BUT_EXTRA Between Pad SW_L2-1(7.25mm,8.875mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net BUT_EXTRA Between Pad SW_L2-2(7.25mm,15.875mm) on Bottom Layer [Unplated] Anc
Un-Routed Net Constraint: Net GND Between Pad SW_L2-3(2.75mm,8.875mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U1-16(39.534mm,20.654mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad U2-4(26.1mm,37mm) on Top Layer And Pad U2-2(31.9mm,37mm) on Top
Un-Routed Net Constraint: Net 9V Between Pad U2-2(31.9mm,37mm) on Top Layer And Pad U3-3(53.65mm,41.55mm) or
Un-Routed Net Constraint: Net 3.3V Between Pad U3-4(47.85mm,39.25mm) on Top Layer And Pad U3-2(53.65mm,39.25mm)

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP1(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP2(2.5mm,56.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP3(72.5mm,56.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP4(72.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-M1(51.5mm,49.75mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-M2(26.5mm,49.75mm) on Multi-Layer Actual Hole Size = 3.2mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(47.904mm,21.36mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(29mm,5.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(47.914mm,20.09mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(46.914mm,17.931mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(49.5mm,6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R4-1(28.364mm,26.686mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R5-1(34.841mm,20.082mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R6-1(34.968mm,26.178mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R7-1(45.358mm,11.322mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R8-1(49.676mm,11.322mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R9-1(45.5mm,6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-1(45.134mm,18.054mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-10(45.134mm,23.904mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-11(39.534mm,23.904mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-12(39.534mm,23.254mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-13(39.534mm,22.604mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-14(39.534mm,21.954mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-15(39.534mm,21.304mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-16(39.534mm,20.654mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-17(39.534mm,20.004mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-18(39.534mm,19.354mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-19(39.534mm,18.704mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-2(45.134mm,18.704mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-3(45.134mm,19.354mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-4(45.134mm,20.004mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-5(45.134mm,20.654mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-6(45.134mm,21.304mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-7(45.134mm,21.954mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-8(45.134mm,22.604mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C1-1(47.904mm,21.36mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.13mm < 0.254mm) Between Pad C1-1(47.904mm,21.36mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C1-2(46.924mm,21.36mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad C1-2(46.924mm,21.36mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(29.9mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-1(29.9mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.034mm < 0.254mm) Between Pad C2-2(28.1mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(28.1mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(28.1mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(34.9mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C3-1(34.9mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(33.1mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(33.1mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C4-1(24.5mm,43.49mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-1(35.7mm,6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad C5-1(35.7mm,6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(34.3mm,6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(34.3mm,6mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.244mm < 0.254mm) Between Pad C6-1(64.5mm,50mm) on Multi-Layer And Tex
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(59.45mm,19.96mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(59.45mm,19.96mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(55.55mm,25.04mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(55.55mm,25.04mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(55.55mm,19.96mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(55.55mm,19.96mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(59.45mm,21.23mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(55.55mm,21.23mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(59.45mm,22.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(55.55mm,22.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(59.45mm,23.77mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(55.55mm,23.77mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-9(59.45mm,25.04mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(59.45mm,25.04mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(54.7mm,5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(54.7mm,5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad L1-2(53.3mm,5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad L1-2(53.3mm,5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R1-1(47.914mm,20.09mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R1-2(46.914mm,20.09mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L1-1(7.25mm,33.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L1-2(7.25mm,40.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L1-3(2.75mm,33.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-4(2.75mm,40.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(5mm,41.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(5mm,41.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L2-1(7.25mm,8.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L2-2(7.25mm,15.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L2-3(2.75mm,8.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-4(2.75mm,15.875mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(5mm,16.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(5mm,16.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-1(31.9mm,34.7mm) on Top Layer And Trac

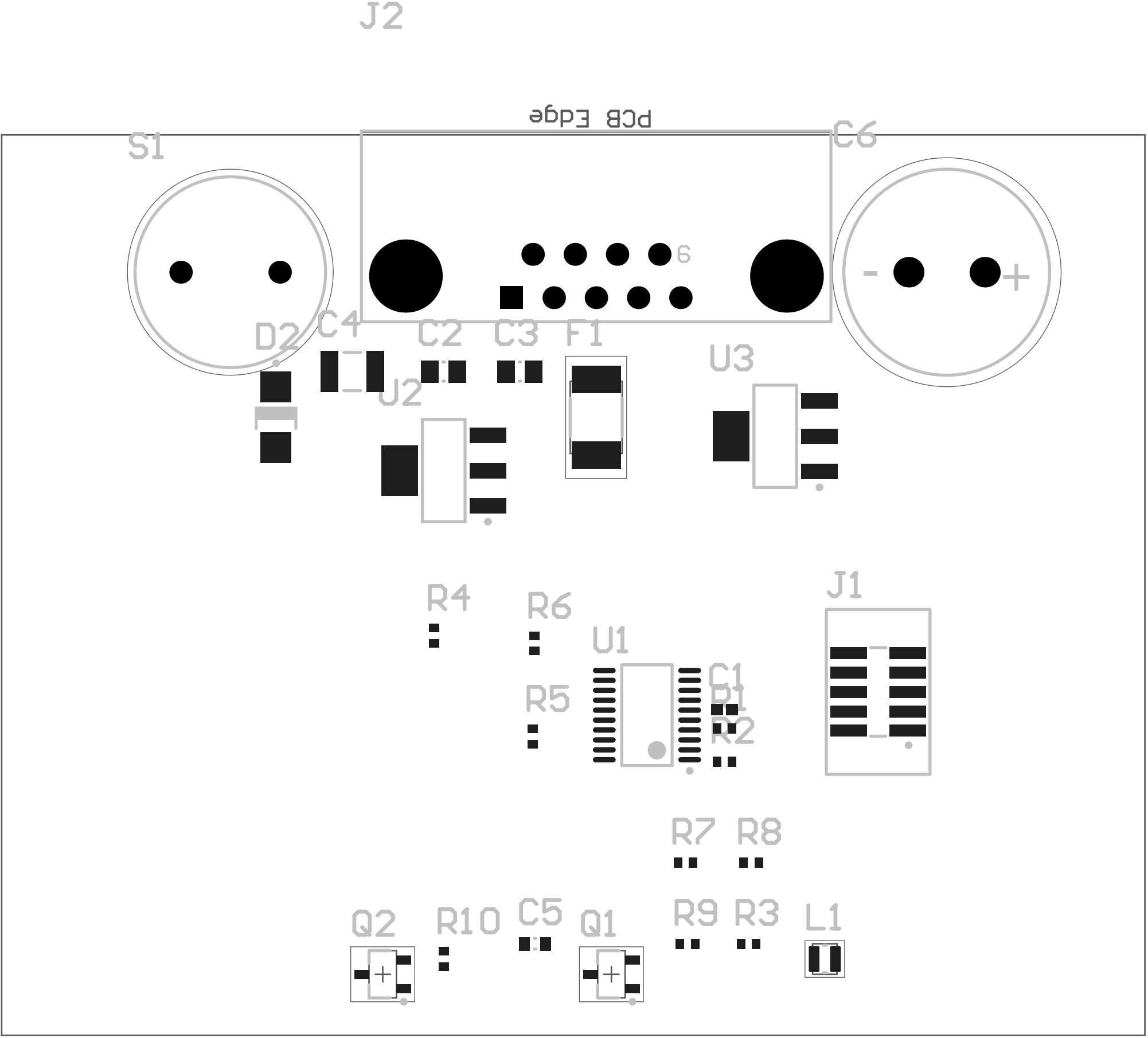
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-2(31.9mm,37mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-3(31.9mm,39.3mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-4(26.1mm,37mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-1(53.65mm,36.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-2(53.65mm,39.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-3(53.65mm,41.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-4(47.85mm,39.25mm) on Top Layer An

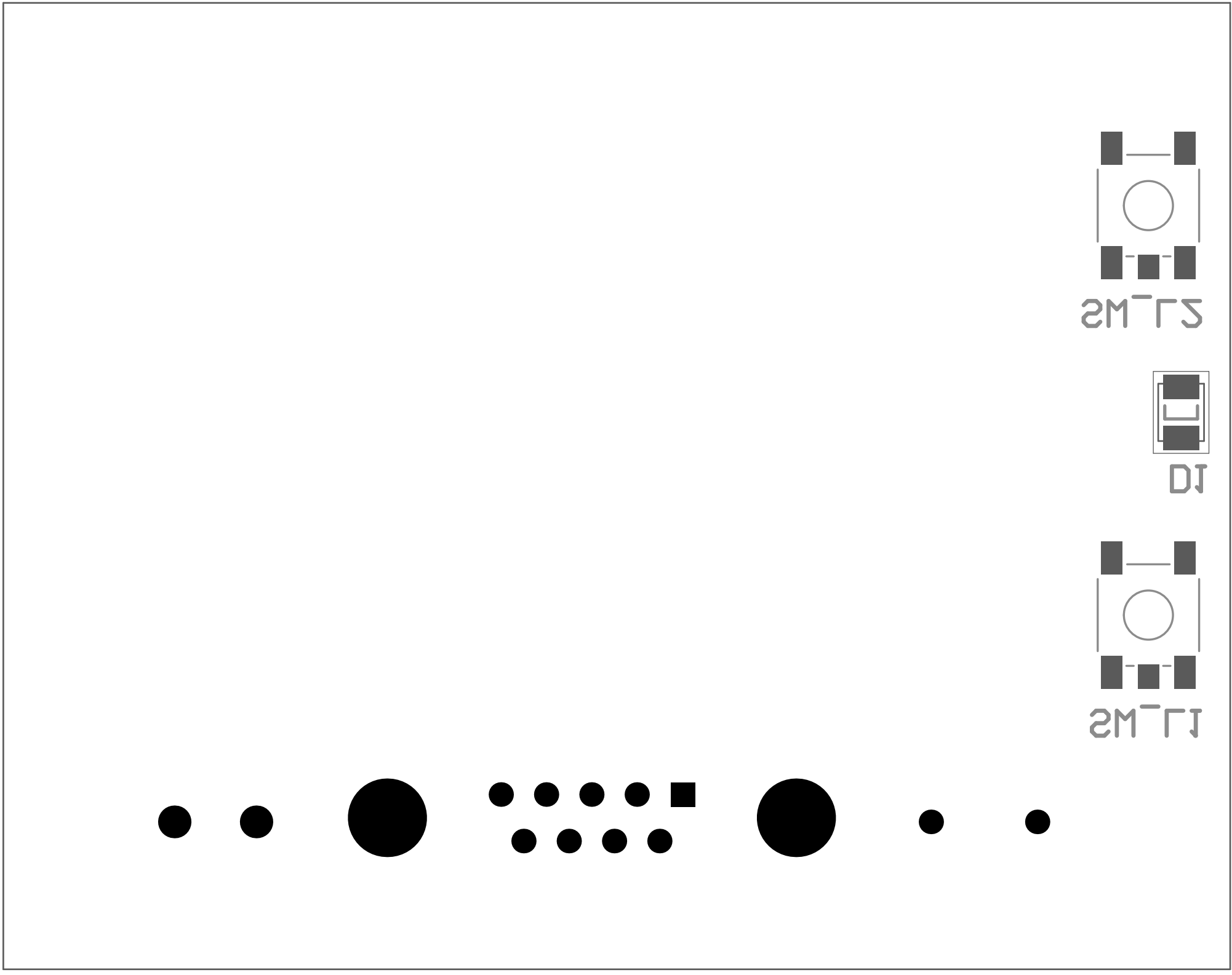
Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.063mm < 0.254mm) Between Arc (15mm,50mm) on Top Overlay And Text "C4
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (15mm,50mm) on Top Overlay And Text "D2
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C1" (46.538mm,22.744mm) on Top Overlay And Te
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C2" (27.489mm,45.281mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C3" (32.489mm,45.281mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C4" (20.879mm,45.865mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C4" (20.879mm,45.865mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.096mm < 0.254mm) Between Text "C6" (54.723mm,58.293mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.096mm < 0.254mm) Between Text "C6" (54.723mm,58.293mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "F1" (37.235mm,45.278mm) on Top Overlay And Trac

Room power (Bounding Region = (106mm, 100.49mm, 151mm, 113.49mm) (InComponentClass('pow
Room Definition: Between Component U2-LD1117S33CTR (29mm,37mm) on Top Layer And Room power (Bounding Regio
Room Definition: Between Room power (Bounding Region = (106mm, 100.49mm, 151mm, 113.49mm)

Electrical Rules Check Report

Class	Document	Message
Error	Sheet2.SchDoc	Net +9V has only one pin (Pin J2-1)
Error	power.SchDoc	Net +12V has only one pin (Pin F1-1)
Error	Sheet2.SchDoc	Net SPI1_MISO has only one pin (Pin U1-12)
Warning	Sheet2.SchDoc	Footprint of component Component OLED? SSD1309 cannot be found
Warning	Sheet2.SchDoc	Net BOOT0 has no driving source (Pin R2-1, Pin U1-1)
Warning	Sheet2.SchDoc	Un-Designated Part OLED?


J2
PCB Edge
S1
C6
6
-
+
D2
C4
C2
C3
F1
U2
U3
R4
R6
U1
J1
C1
R1
R5
R2
R7
R8
Q2
R10
C5
Q1
R9
R3
L1


SW_PUSH
LED
SW_PUSH