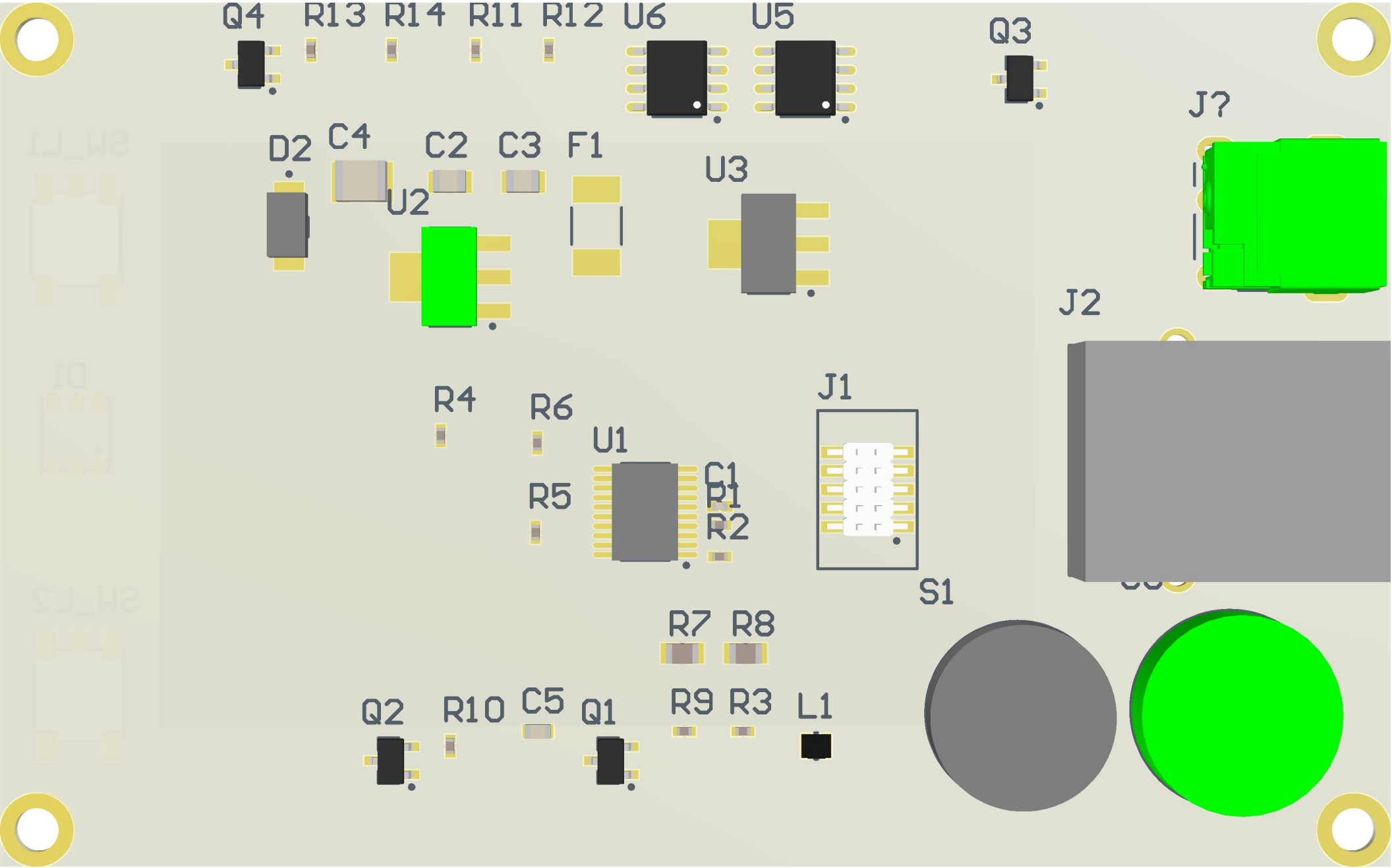
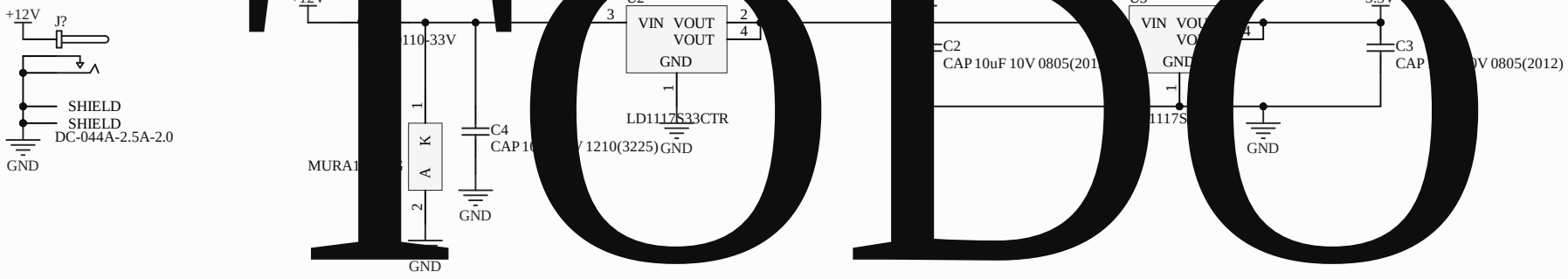
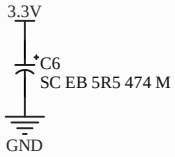

Q4
R13
R14
R11
R12
U6
U5
Q3
J?
D2
C4
C2
C3
F1
U2
U3
J2
R4
R6
U1
J1
C1
R5
R1
R2
S1
R7
R8
Q2
R10
C5
Q1
R9
R3
L1

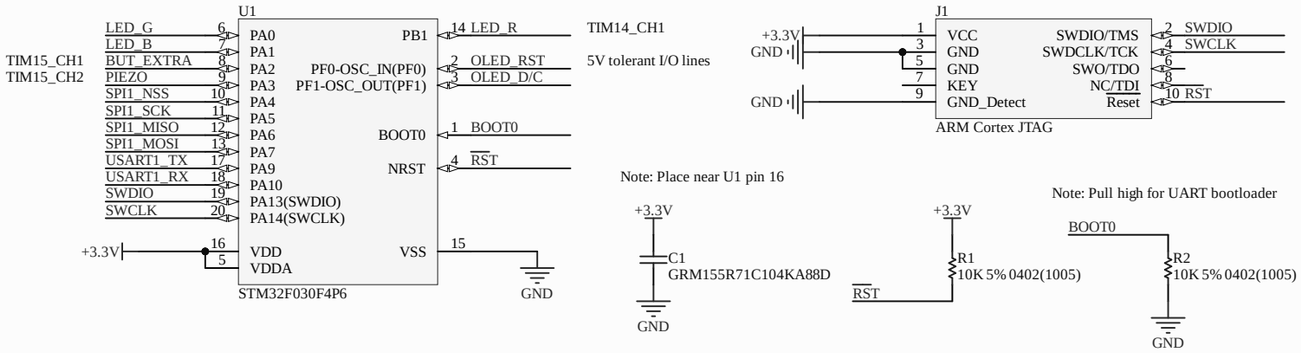


Supercap power backup



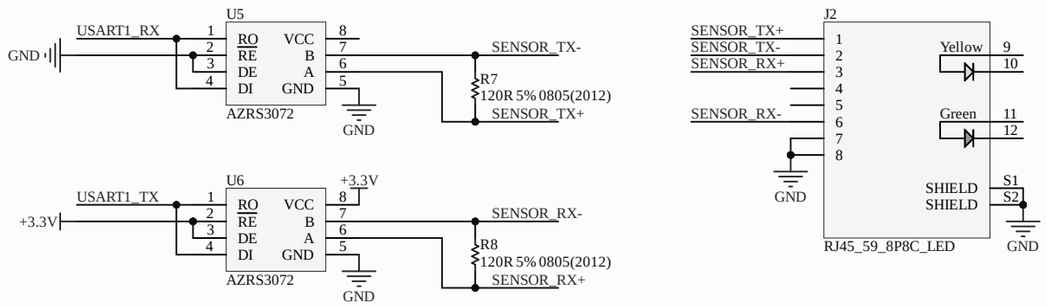
Notes:
-Device should be capable of flashing alarm for TBD seconds after power is depleted.
-Cap must stay above microcontroller brownout voltage TBD while drawing TBD current.

Microcontroller

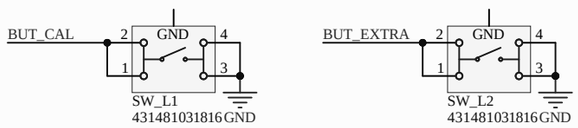


Notes:
-The specific STM32 part is generic, and could be replaced with a similar part from the F0 or F1 family.
-The microcontroller needs to sample an analog value at 200Hz, process it, and then show the results on a monochrome graphical display.
-In particular, it could be advantageous to switch to a part with a USB bootloader for easier field upgrades.

Sensor board connector

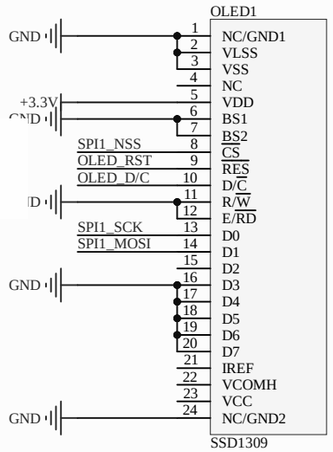


Buttons



Notes:
-This is a generic footprint, need to confirm that they integrate correctly with the mechanical design
-It would be desireable to use a sealed version if available

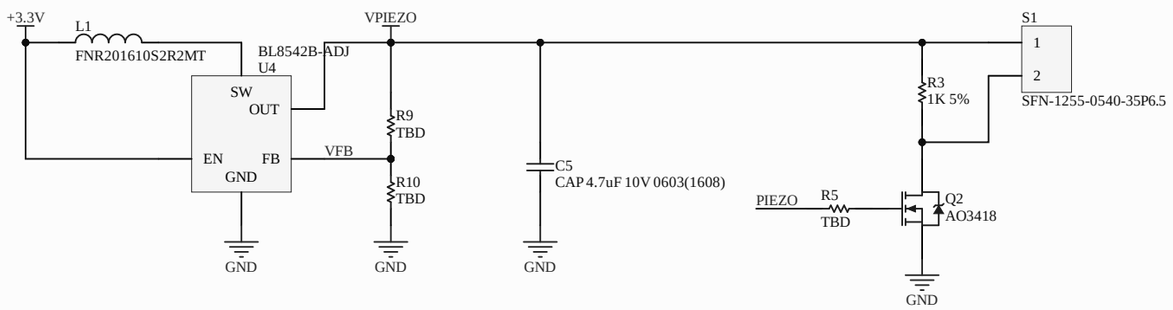
Display connector



TODO: Boost circuit

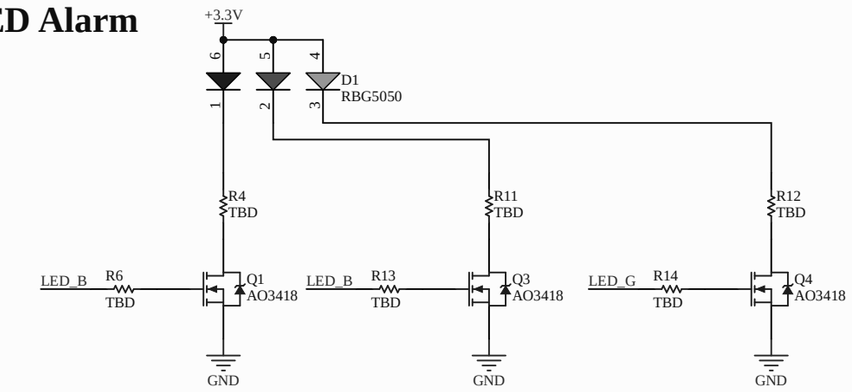
Notes:
-A 3" display is preferred by the spec
-This connector is for a 2.5" OLED device, which is believed to be widely available in China.
-If a 3" LCD is common/easily available, it could be swapped in.

Piezo Alarm

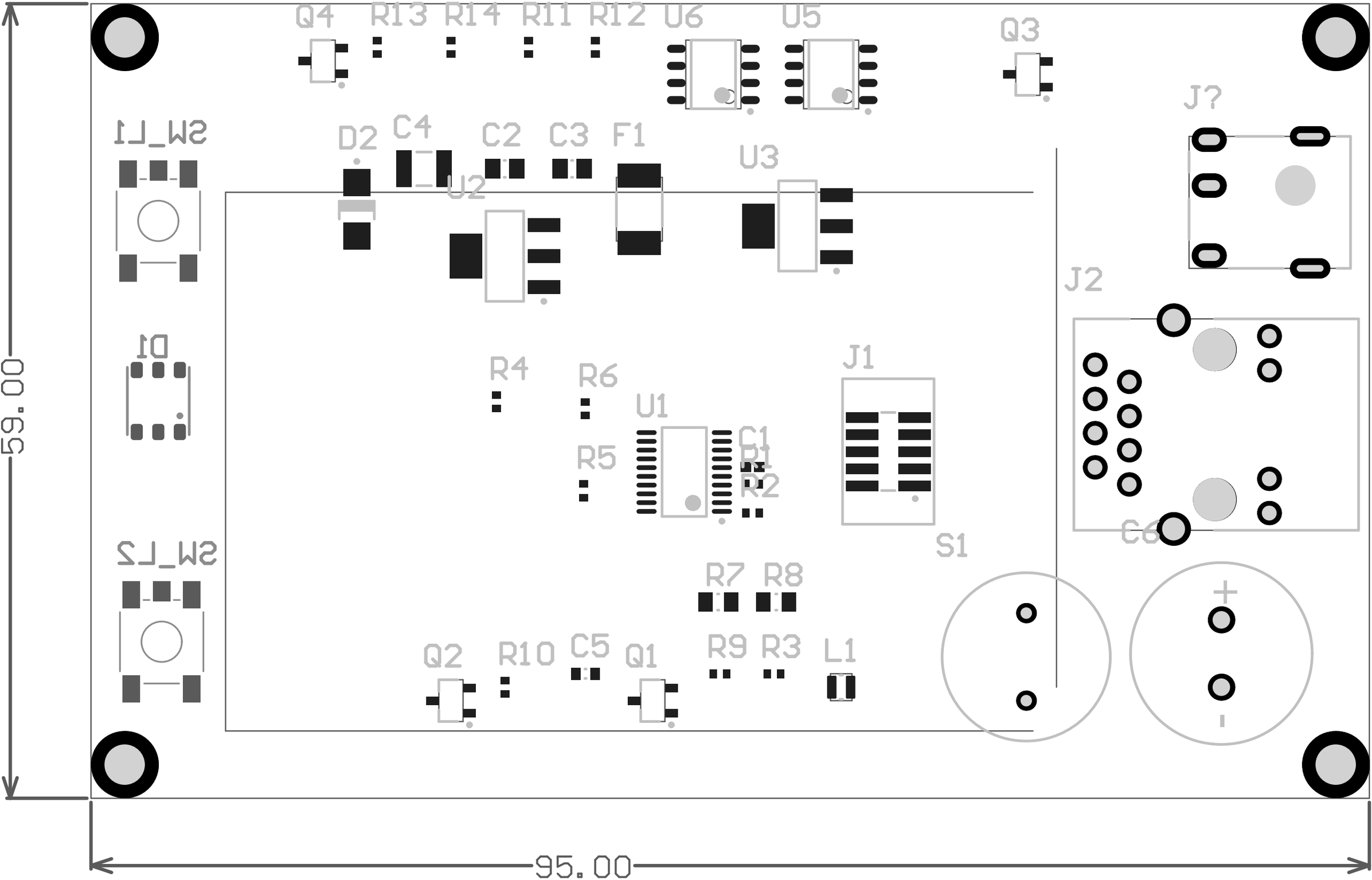


Notes:
-Need to produce drive voltage from +3.3V rail, to allow the alarm to work during a loss-of-power event.
-Peak voltage and current requirements should be adjusted based on chosen Piezo element
-Parallel resistive element R3 allows for a discharge cycle
-Drive transistor Q1 is generic

LED Alarm



Notes:
-Can be powered directly from +3.3V
-Needs to work during a loss-of-power event


Q4
R13
R14
R11
R12
U6
U5
Q3
J?
SW_LI
D2
C4
C2
C3
F1
U2
U3
J2
D1
R4
R6
U1
J1
C1
R1
R2
R5
C6
S1
SW_L2
R7
R8
Q2
R10
C5
Q1
R9
R3
L1
59.00
95.00

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\alarm_module\pcb\PCB2.PcbDoc

Warnings 2
Rule Violations 204

Warnings	
Unplated multi-layer pad(s) detected	2
Total	2

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	96
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	31
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	64
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Room power (Bounding Region = (107.75mm, 103.74mm, 152.75mm, 116.74mm)	3
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	204

Unplated multi-layer pad(s) detected
Pad S1-2(69.5mm,13.75mm) on Multi-Layer on Net NetQ2_3
Pad S1-1(69.5mm,7.25mm) on Multi-Layer on Net VPIEZO

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(49.654mm,24.61mm) on Top Layer And Pac

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint:
Un-Routed Net Constraint:
Un-Routed Net Constraint: Net GND Between Pad C1-1(49.654mm,24.61mm) on Top Layer And Pad J1-3(61.2mm,24.48mm)
Un-Routed Net Constraint: Net GND Between Pad C1-1(49.654mm,24.61mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U1-15(41.284mm,24.554mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad C1-2(48.674mm,24.61mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U1-5(46.884mm,23.904mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad C1-2(48.674mm,24.61mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad C2-1(31.65mm,46.74mm) on Top Layer And Pad C3-1(36.65mm,46.74mm
Un-Routed Net Constraint: Net GND Between Pad C4-1(26.25mm,46.74mm) on Top Layer And Pad C2-1(31.65mm,46.74mm
Un-Routed Net Constraint: Net GND Between Pad C2-1(31.65mm,46.74mm) on Top Layer And Pad U2-1(33.65mm,37.95mm
Un-Routed Net Constraint: Net 9V Between Pad U2-4(27.85mm,40.25mm) on Top Layer And Pad C2-2(29.85mm,46.74mm
Un-Routed Net Constraint: Net GND Between Pad C3-1(36.65mm,46.74mm) on Top Layer And Pad U6-5(43.5mm,55.655mm
Un-Routed Net Constraint: Net 3.3V Between Pad C3-2(34.85mm,46.74mm) on Top Layer And Pad U3-4(49.6mm,42.5mm
Un-Routed Net Constraint: Net GND Between Pad D2-2(19.75mm,41.74mm) on Top Layer And Pad C4-1(26.25mm,46.74mm
Un-Routed Net Constraint: Net NetC4_2 Between Pad D2-1(19.75mm,45.74mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC4_2 Between Pad C4-2(23.25mm,46.74mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad C5-1(37.45mm,9.25mm) on Top Layer And Pad Q1-2(43.125mm,8.2mm
Un-Routed Net Constraint: Net GND Between Pad R10-1(30.75mm,8.75mm) on Top Layer And Pad C5-1(37.45mm,9.25mm
Un-Routed Net Constraint: Net VPIEZO Between Pad C5-2(36.05mm,9.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U3-2(55.4mm,42.5mm) on Top Layer And Pad C6-1(84mm,13.25mm) or
Un-Routed Net Constraint: Net GND Between Pad J2-S1(80.45mm,20mm) on Multi-Layer And Pad C6-2(84mm,8.25mm) or
Un-Routed Net Constraint: Net NetD1_1 Between Pad D1-1(6.6mm,27.3mm) on Bottom Layer And Pac
Un-Routed Net Constraint: Net NetD1_2 Between Pad D1-2(5mm,27.3mm) on Bottom Layer And Pac
Un-Routed Net Constraint: Net NetD1_3 Between Pad D1-3(3.4mm,27.3mm) on Bottom Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad D1-4(3.4mm,31.7mm) on Bottom Layer And Pad D1-5(5mm,31.7mm) or
Un-Routed Net Constraint: Net +3.3V Between Pad D1-5(5mm,31.7mm) on Bottom Layer And Pad D1-6(6.6mm,31.7mm) or
Un-Routed Net Constraint: Net +3.3V Between Pad D1-6(6.6mm,31.7mm) on Bottom Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad Q4-2(18.625mm,55.7mm) on Top Layer And Pad D2-2(19.75mm,41.74mm
Un-Routed Net Constraint: Net GND Between Pad SW_L1-3(2.75mm,39.375mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net +12V Between Pad F1-1(40.75mm,46.23mm) on Top Layer And Pad J?-1(83.1mm,48.9mm
Un-Routed Net Constraint: Net NetC4_2 Between Pad U2-3(33.65mm,42.55mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J?-2(83.1mm,40.3mm) on Multi-Layer And Pad J?-3(83.1mm,45.5mm) or
Un-Routed Net Constraint: Net GND Between Pad J?-2(83.1mm,40.3mm) on Multi-Layer And Pad J?-5(90.6mm,39.35mm) or
Un-Routed Net Constraint: Net GND Between Pad J2-S2(80.45mm,35.5mm) on Multi-Layer And Pad J?-2(83.1mm,40.3mm)
Un-Routed Net Constraint: Net GND Between Pad J?-5(90.6mm,39.35mm) on Multi-Layer And Pad J?-4(90.6mm,49.15mm)
Un-Routed Net Constraint: Net +3.3V Between Pad L1-1(56.45mm,8.25mm) on Top Layer And Pad J1-1(61.2mm,23.21mm
Un-Routed Net Constraint: Net +3.3V Between Pad R1-1(49.664mm,23.34mm) on Top Layer And Pac
Un-Routed Net Constraint: Net \R\S\T Between Pad R1-2(48.664mm,23.34mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SWDIO Between Pad U1-19(41.284mm,21.954mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J1-3(61.2mm,24.48mm) on Top Layer And Pad J1-5(61.2mm,25.75mm) or
Un-Routed Net Constraint: Net SWCLK Between Pad U1-20(41.284mm,21.304mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J1-5(61.2mm,25.75mm) on Top Layer And Pad J1-9(61.2mm,28.29mm) or
Un-Routed Net Constraint: Net GND Between Pad J1-9(61.2mm,28.29mm) on Top Layer And Pad J2-8(74.61mm,32.195mm
Un-Routed Net Constraint: Net GND Between Pad U3-1(55.4mm,40.2mm) on Top Layer And Pad J1-9(61.2mm,28.29mm) or
Un-Routed Net Constraint: Net SENSOR_TX+ Between Pad R7-1(47.558mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX- Between Pad R7-2(45.658mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX+ Between Pad R8-1(51.876mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX- Between Pad R8-2(49.976mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J2-8(74.61mm,32.195mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J2-7(77.15mm,30.925mm) on Multi-Layer And Pad J2-S1(80.45mm,20mm)
Un-Routed Net Constraint: Net GND Between Pad J2-7(77.15mm,30.925mm) on Multi-Layer And Pac

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net NetQ1_1 Between Pad R6-2(36.718mm,28.428mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U1-15(41.284mm,24.554mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetQ1_3 Between Pad R4-1(30.114mm,29.936mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad Q2-2(28.125mm,8.2mm) on Top Layer And Pad R10-1(30.75mm,8.75mm
Un-Routed Net Constraint: Net NetQ2_3 Between Pad Q2-3(25.375mm,7.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetQ3_1 Between Pad R13-2(21.25mm,55.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U5-3(57.75mm,54.385mm) on Top Layer And Pad Q3-2(71mm,54.7mm) or
Un-Routed Net Constraint: Net NetQ3_3 Between Pad R11-1(32.5mm,56.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetQ4_1 Between Pad Q4-1(18.625mm,53.8mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetQ4_3 Between Pad Q4-3(15.875mm,54.75mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VFB Between Pad R10-2(30.75mm,7.75mm) on Top Layer And Pad R9-1(47.25mm,9.25mm
Un-Routed Net Constraint: Net \R\S\T Between Pad U1-4(46.884mm,23.254mm) on Top Layer And Pac
Un-Routed Net Constraint: Net LED_B Between Pad R13-1(21.25mm,56.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net LED_G Between Pad R14-1(26.75mm,56.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net BOOT0 Between Pad U1-1(46.884mm,21.304mm) on Top Layer And Pac
Un-Routed Net Constraint: Pad R3-1(51.25mm,9.25mm) on Top Layer
Un-Routed Net Constraint: Pad R3-2(50.25mm,9.25mm) on Top Layer
Un-Routed Net Constraint: Net VPIEZO Between Pad R9-2(46.25mm,9.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net PIEZO Between Pad R5-1(36.591mm,23.332mm) on Top Layer And Pac
Un-Routed Net Constraint: Net LED_B Between Pad R6-1(36.718mm,29.428mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX+ Between Pad R7-1(47.558mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX- Between Pad R7-2(45.658mm,14.572mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX+ Between Pad U6-6(43.5mm,54.385mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX- Between Pad U6-7(43.5mm,53.115mm) on Top Layer And Pac
Un-Routed Net Constraint: Net BUT_CAL Between Pad SW_L1-1(7.25mm,39.375mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net GND Between Pad SW_L1-3(2.75mm,39.375mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net GND Between Pad SW_L1-3(2.75mm,39.375mm) on Bottom Layer [Unplated] And Pad
Un-Routed Net Constraint: Net BUT_EXTRA Between Pad SW_L2-1(7.5mm,8.125mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net BUT_EXTRA Between Pad SW_L2-2(7.5mm,15.125mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net GND Between Pad SW_L2-3(3mm,8.125mm) on Bottom Layer [Unplated] And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U1-16(41.284mm,23.904mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_TX Between Pad U1-17(41.284mm,23.254mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_RX Between Pad U1-18(41.284mm,22.604mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad U2-4(27.85mm,40.25mm) on Top Layer And Pad U2-2(33.65mm,40.25mm
Un-Routed Net Constraint: Net 9V Between Pad U2-2(33.65mm,40.25mm) on Top Layer And Pad U3-3(55.4mm,44.8mm) or
Un-Routed Net Constraint: Net GND Between Pad U3-1(55.4mm,40.2mm) on Top Layer And Pad U5-2(57.75mm,53.115mm
Un-Routed Net Constraint: Net 3.3V Between Pad U3-4(49.6mm,42.5mm) on Top Layer And Pad U3-2(55.4mm,42.5mm) or
Un-Routed Net Constraint: Net USART1_RX Between Pad U5-1(57.75mm,51.845mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U5-2(57.75mm,53.115mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U5-5(52.25mm,55.655mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad U6-5(43.5mm,55.655mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_TX Between Pad U6-1(49mm,51.845mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U6-2(49mm,53.115mm) on Top Layer And Pad U6-3(49mm,54.385mm
Un-Routed Net Constraint: Net +3.3V Between Pad U6-8(43.5mm,51.845mm) on Top Layer And Pad U6-2(49mm,53.115mm

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP1(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP2(2.5mm,56.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP3(92.5mm,56.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-MP4(92.5mm,2.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad J?-MNT(89.5mm,45.5mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS1(83.5mm,22.185mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS2(83.5mm,33.315mm) on Multi-Layer Actual Hole Size = 3.2mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(49.654mm,24.61mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(30.75mm,8.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(49.664mm,23.34mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R11-1(32.5mm,56.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R12-1(37.5mm,56.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R13-1(21.25mm,56.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R14-1(26.75mm,56.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(48.664mm,21.181mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(51.25mm,9.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R4-1(30.114mm,29.936mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R5-1(36.591mm,23.332mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R6-1(36.718mm,29.428mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R9-1(47.25mm,9.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-1(46.884mm,21.304mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-10(46.884mm,27.154mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-11(41.284mm,27.154mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-12(41.284mm,26.504mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-13(41.284mm,25.854mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-14(41.284mm,25.204mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-15(41.284mm,24.554mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-16(41.284mm,23.904mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-17(41.284mm,23.254mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-18(41.284mm,22.604mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-19(41.284mm,21.954mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-2(46.884mm,21.954mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-3(46.884mm,22.604mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-4(46.884mm,23.254mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-5(46.884mm,23.904mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-6(46.884mm,24.554mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-7(46.884mm,25.204mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U1-8(46.884mm,25.854mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C1-1(49.654mm,24.61mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.13mm < 0.254mm) Between Pad C1-1(49.654mm,24.61mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C1-2(48.674mm,24.61mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad C1-2(48.674mm,24.61mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(31.65mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-1(31.65mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.034mm < 0.254mm) Between Pad C2-2(29.85mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(29.85mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(29.85mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(36.65mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C3-1(36.65mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(34.85mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(34.85mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C4-1(26.25mm,46.74mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-1(37.45mm,9.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad C5-1(37.45mm,9.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(36.05mm,9.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C5-2(36.05mm,9.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.232mm < 0.254mm) Between Pad C6-1(84mm,13.25mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad D1-1(6.6mm,27.3mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.227mm < 0.254mm) Between Pad D1-3(3.4mm,27.3mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.23mm < 0.254mm) Between Pad D1-4(3.4mm,31.7mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad D1-6(6.6mm,31.7mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(61.2mm,23.21mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(61.2mm,23.21mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(57.3mm,28.29mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(57.3mm,28.29mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(57.3mm,23.21mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(57.3mm,23.21mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(61.2mm,24.48mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(57.3mm,24.48mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(61.2mm,25.75mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(57.3mm,25.75mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(61.2mm,27.02mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(57.3mm,27.02mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-9(61.2mm,28.29mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(61.2mm,28.29mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad J2-S1(80.45mm,20mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(56.45mm,8.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.196mm < 0.254mm) Between Pad L1-1(56.45mm,8.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad L1-2(55.05mm,8.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad L1-2(55.05mm,8.25mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R1-1(49.664mm,23.34mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R1-2(48.664mm,23.34mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L1-1(7.25mm,39.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L1-2(7.25mm,46.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L1-3(2.75mm,39.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-4(2.75mm,46.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(5mm,46.625mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L1-5(5mm,46.625mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad SW_L2-1(7.5mm,8.125mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.186mm < 0.254mm) Between Pad SW_L2-2(7.5mm,15.125mm) on Bottom

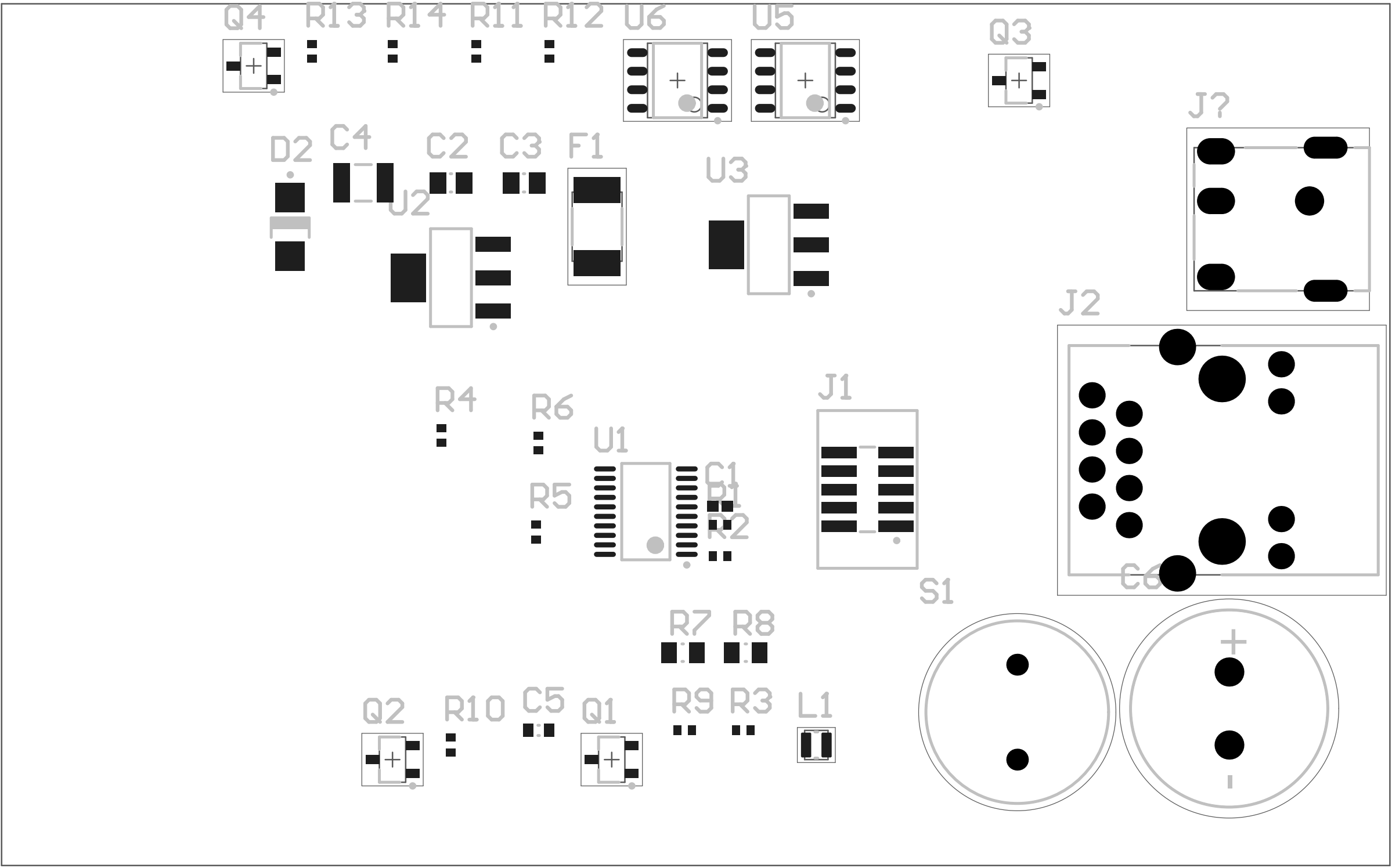
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad SW_L2-3(3mm,8.125mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-4(3mm,15.125mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(5.25mm,15.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad SW_L2-5(5.25mm,15.375mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-1(33.65mm,37.95mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-2(33.65mm,40.25mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-3(33.65mm,42.55mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-4(27.85mm,40.25mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-1(55.4mm,40.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-2(55.4mm,42.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-3(55.4mm,44.8mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U3-4(49.6mm,42.5mm) on Top Layer And Trac

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C1" (48.288mm,25.994mm) on Top Overlay And Te
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C6" (76.738mm,19.045mm) on Top Overlay An

Room power (Bounding Region = (107.75mm, 103.74mm, 152.75mm, 116.74mm) (InComponentClass
Room Definition: Between Component J?-DC-044A-2.5A-2.0 (93.6mm,45.5mm) on Top Layer And Room power (Bounding
Room Definition: Between Component U2-LD1117S33CTR (30.75mm,40.25mm) on Top Layer And Room power (Bounding
Room Definition: Between Room power (Bounding Region = (107.75mm, 103.74mm, 152.75mm, 116.74mm)

Electrical Rules Check Report

Class	Document	Message
Error	Sheet2.SchDoc	Net LED_R has only one pin (Pin U1-14)
Error	Sheet2.SchDoc	Net SPI1_MISO has only one pin (Pin U1-12)
Warning	Sheet2.SchDoc	Footprint of component Component OLED1 SSD1309 cannot be found
Warning	Sheet2.SchDoc	Net BOOT0 has no driving source (Pin R2-1, Pin U1-1)
Warning	power.SchDoc	Un-Designated Part J?


Q4
R13
R14
R11
R12
U6
U5
Q3
J?
D2
C4
C2
C3
F1
U2
U3
J2
R4
R6
J1
U1
C1
R5
R2
C6
S1
R7
R8
Q2
R10
C5
Q1
R9
R3
L1


SW_L1
D1
SW_L2