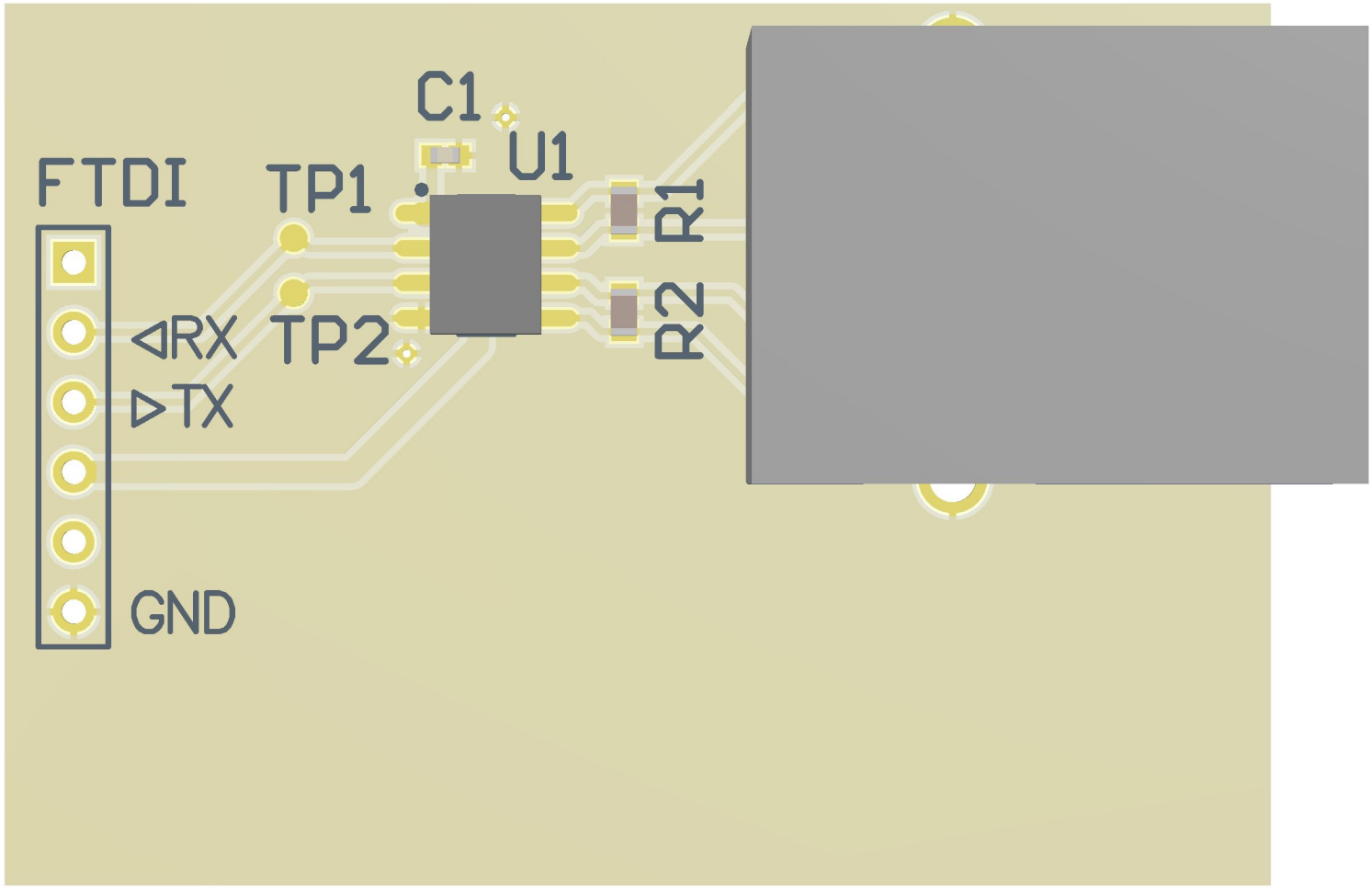
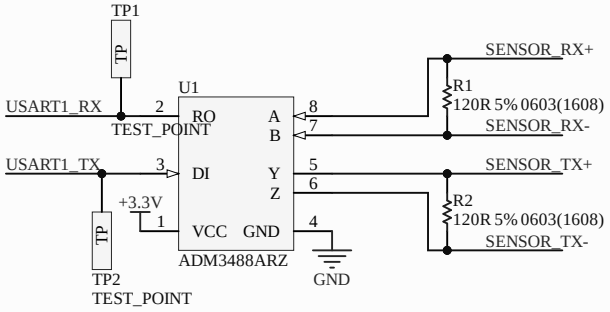
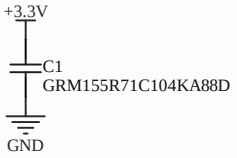
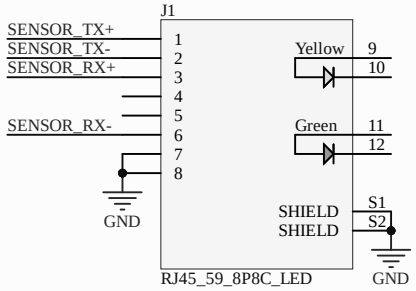
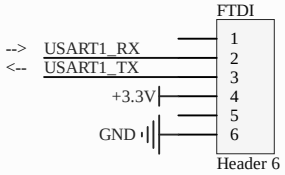

C1
U1
FTDI
TP1
R1
R2
RX
TP2
TX
GND

Sensor board connector

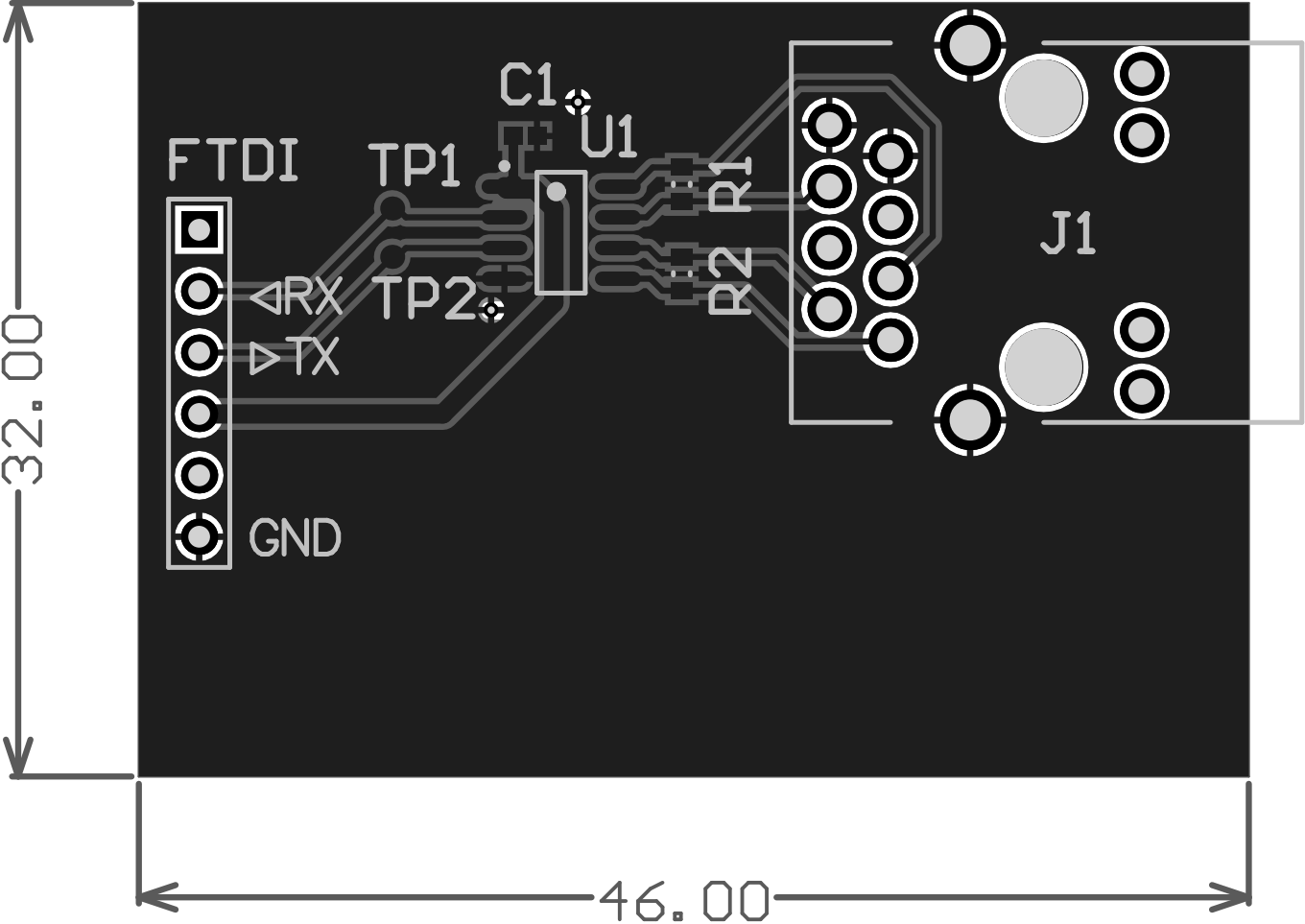








Title: *		BLINKINLABS
Project: alarm_to_uart.PrjPcb	Revision: *	
Date: 4/7/2020 Time: 7:29:14 PM	Sheet * of *	


C1
U1
FTDI
TP1
R1
R2
J1
RX
TP2
TX
GND
32.00
46.00

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\alarm_module\alarm_to_uart\PCB1.P

Warnings 0
Rule Violations 14

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=314.961mil) (Preferred=10mil) (All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	2
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	1
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	8
Silk to Silk (Clearance=10mil) (All),(All)	2
Net Antennae (Tolerance=0mil) (All)	0
Room Sheet4 (Bounding Region = (4133.858mil, 3267.716mil, 6732.283mil, 5314.961mil)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	14

Clearance Constraint (Gap=10mil) (All),(All)
Clearance Constraint: (8.662mil < 10mil) Between Pad C1-1(5177.165mil,4783.465mil) on Top Layer And Pac

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (125.984mil > 100mil) Pad J1-POS1(6003.937mil,4406.89mil) on Multi-Layer Actual Hole Size =
Hole Size Constraint: (125.984mil > 100mil) Pad J1-POS2(6003.937mil,4845.079mil) on Multi-Layer Actual Hole Size =

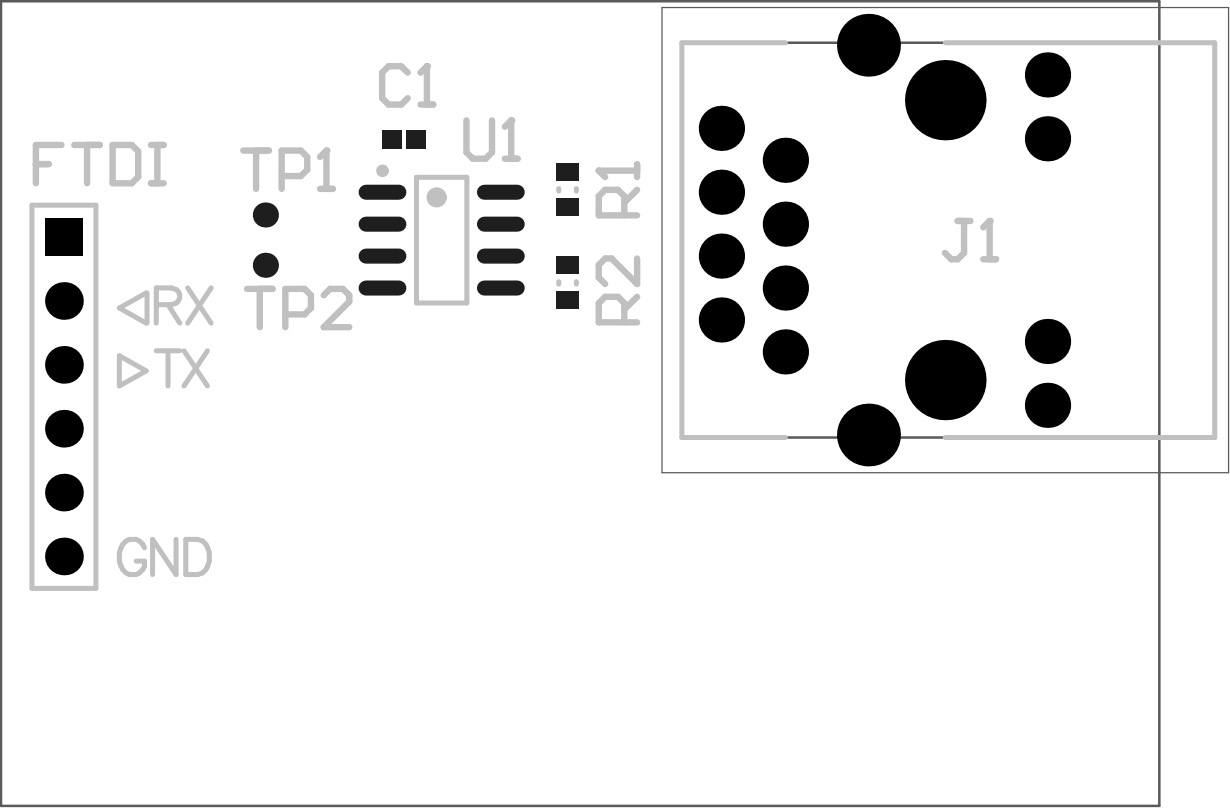
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.662mil < 10mil) Between Pad C1-1(5177.165mil,4783.465mil) on Top Layer And

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R1-1(5413.386mil,4677.165mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R1-1(5413.386mil,4677.165mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R1-2(5413.386mil,4732.283mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R1-2(5413.386mil,4732.283mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R2-1(5413.386mil,4586.614mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R2-1(5413.386mil,4586.614mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R2-2(5413.386mil,4531.496mil) on Top Layer And
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R2-2(5413.386mil,4531.496mil) on Top Layer And

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "<RX" (4704.725mil,4488.189mil) on Top Overlay And
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text ">TX" (4704.725mil,4389.764mil) on Top Overlay And

Electrical Rules Check Report

Class	Document	Message
Warning	Sheet4.SchDoc	Net SENSOR_RX+ has no driving source (Pin J1-3, Pin R1-2, Pin U1-8)
Warning	Sheet4.SchDoc	Net SENSOR_RX- has no driving source (Pin J1-6, Pin R1-1, Pin U1-7)
Warning	Sheet4.SchDoc	Net USART1_TX has no driving source (Pin FTDI-3, Pin TP2-1, Pin U1-3)


C1
U1
FTDI
TP1
R1
R2
J1
RX
TX
TP2
GND

Alarm Board
Comms
2020-04-07
RevA