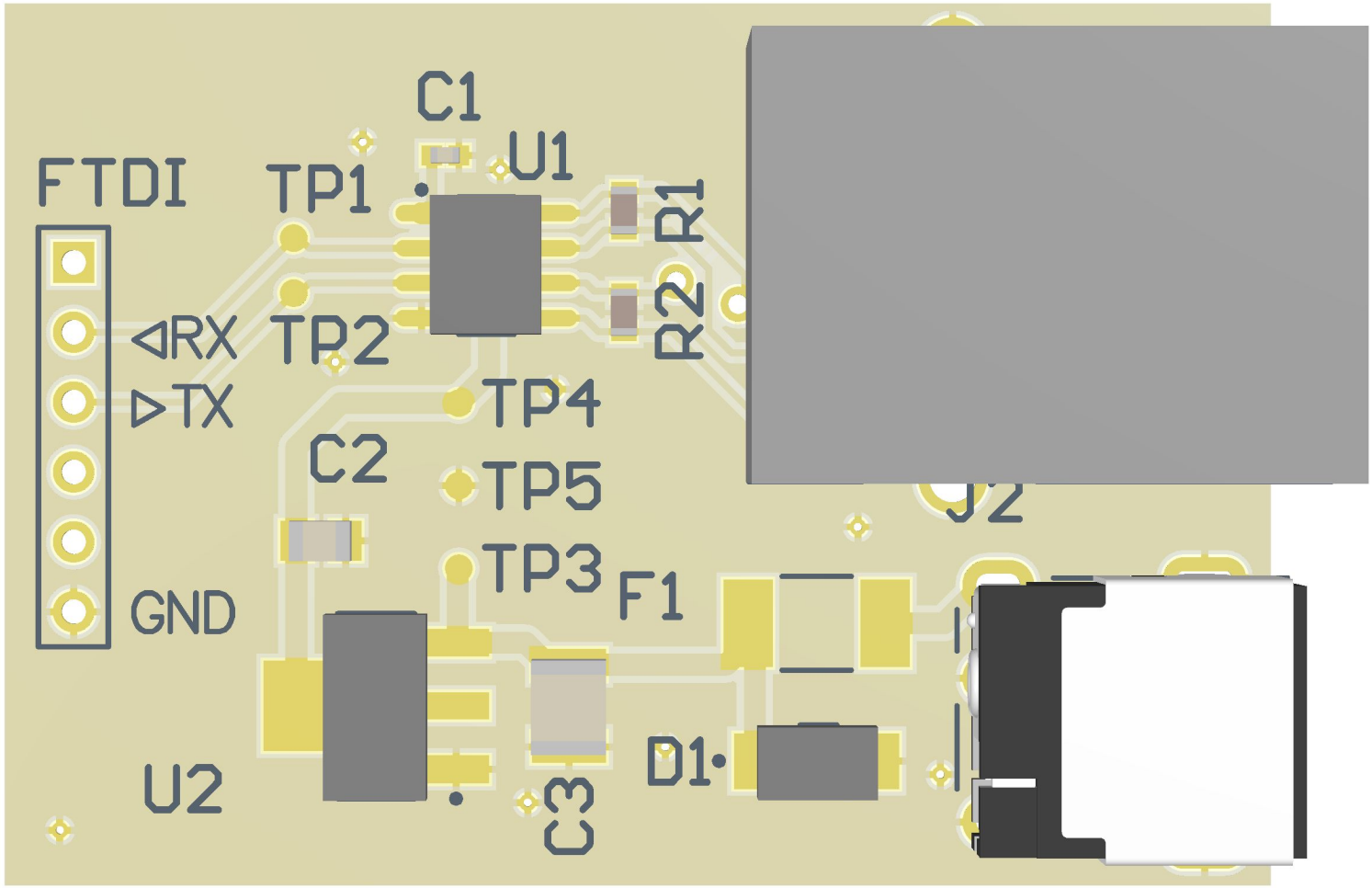
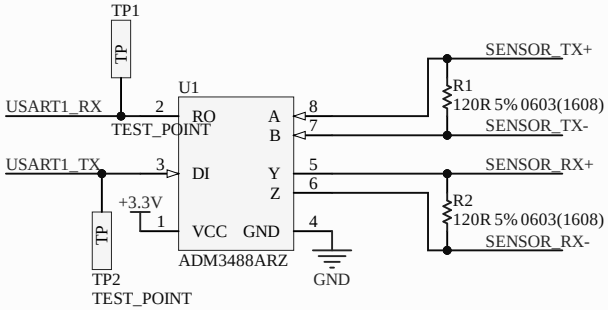
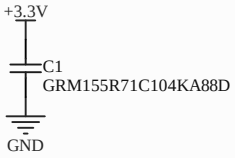
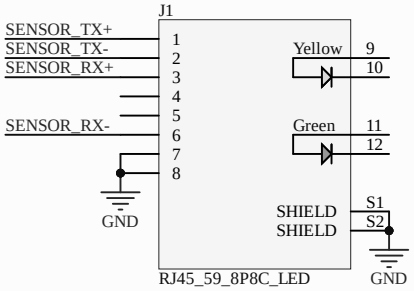
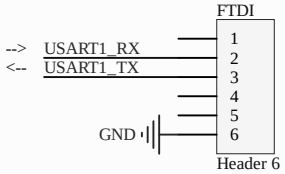

C1
U1
FTDI
TP1
R1
R2
RX
TP2
TX
TP4
C2
TP5
TP3
F1
GND
U2
C3
D1

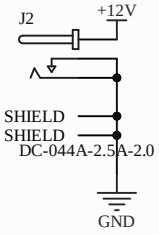
Sensor board connector

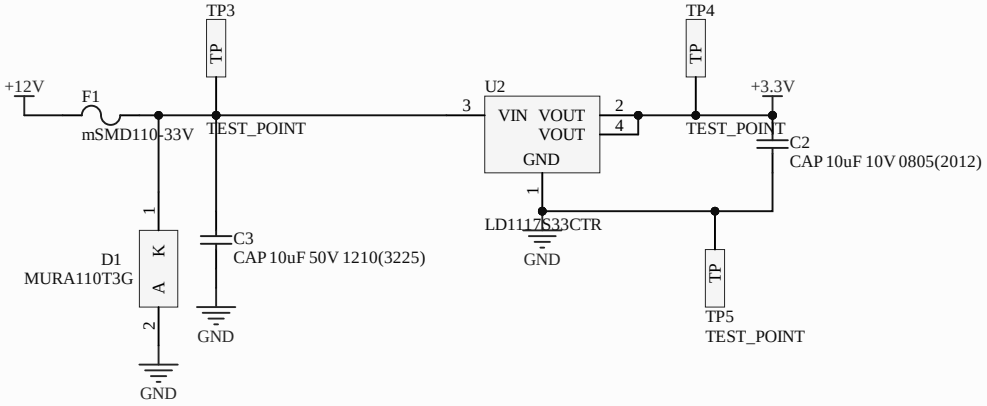






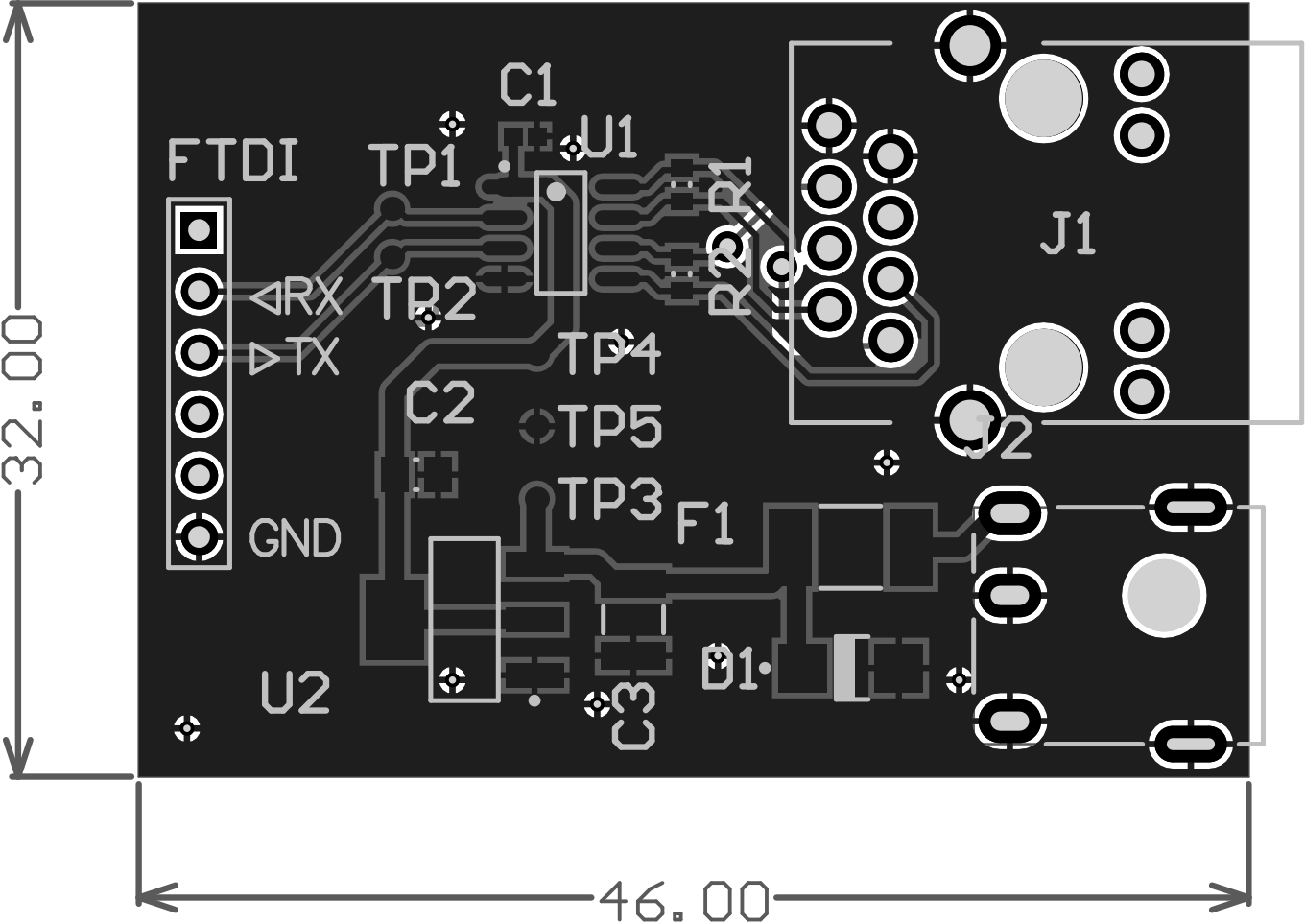






Title: *		
Project: sensor_to_uart.PrjPcb	Revision: *	
Date: 4/7/2020 Time: 7:26:29 PM	Sheet * of *	

BLIN KIN LABS


C1
U1
FTDI
TP1
R1
R2
J1
RX
TP2
TX
TP4
C2
TP5
J2
TP3
F1
GND
U2
D1
C3
32.00
46.00

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\sensor_module\sensor_to_uart\PCB3.

Warnings 0
Rule Violations 24

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.8mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	3
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	1
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	17
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet3 (Bounding Region = (102.5mm, 90mm, 152.5mm, 125.503mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	24

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(16.5mm,26.5mm) on Top Layer And Pac

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS1(37.5mm,16.935mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS2(37.5mm,28.065mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3mm > 2.54mm) Pad J2-MNT(42.5mm,7.5mm) on Multi-Layer Actual Hole Size = 3mm

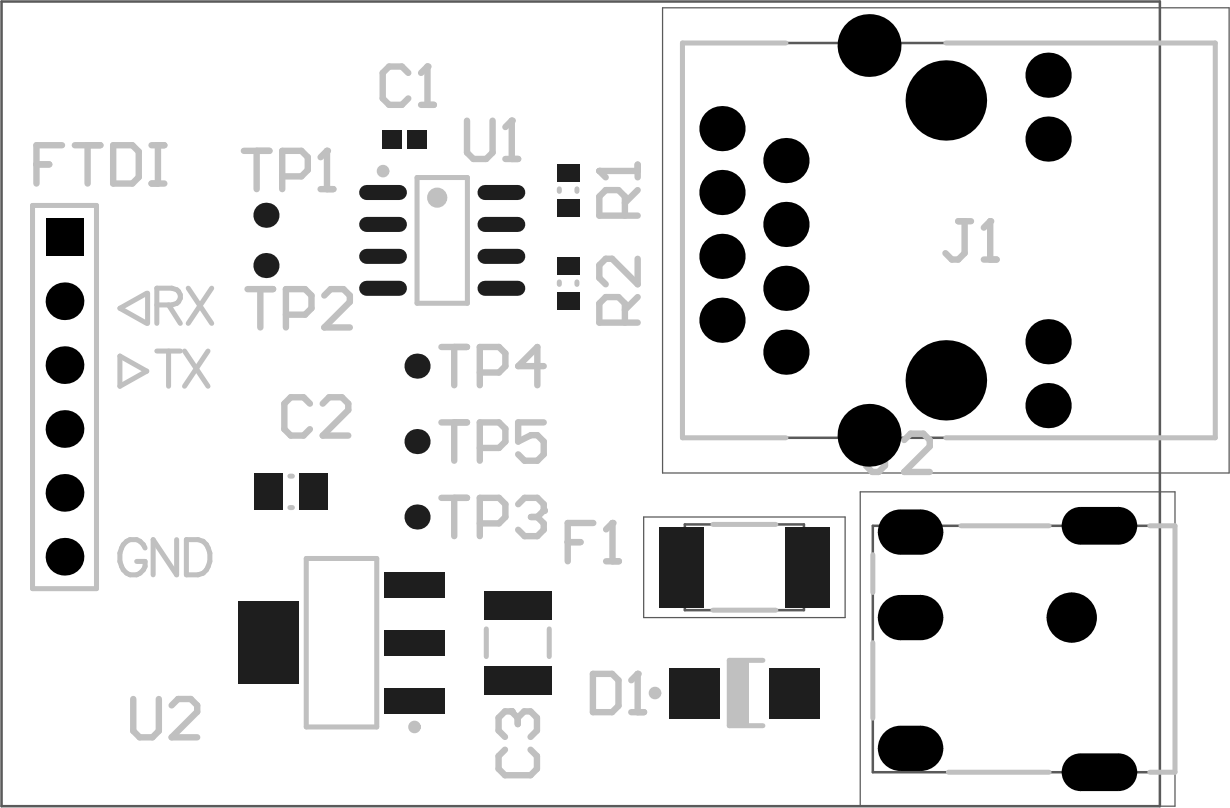
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(16.5mm,26.5mm) on Top Layer And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(12.4mm,12.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-1(12.4mm,12.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(10.6mm,12.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(10.6mm,12.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad J1-S1(34.45mm,14.75mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(22.5mm,23.8mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(22.5mm,23.8mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(22.5mm,25.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R1-2(22.5mm,25.2mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-1(22.5mm,21.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R2-1(22.5mm,21.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(22.5mm,20.1mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(22.5mm,20.1mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-1(16.4mm,4.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-2(16.4mm,6.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-3(16.4mm,8.8mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-4(10.6mm,6.5mm) on Top Layer And Trac

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "<RX" (4.5mm,19mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text ">TX" (4.5mm,16.5mm) on Top Overlay And Trac

Electrical Rules Check Report

Class	Document	Message
Warning	Sheet3.SchDoc	Net SENSOR_TX+ has no driving source (Pin J1-1, Pin R1-2, Pin U1-8)
Warning	Sheet3.SchDoc	Net SENSOR_TX- has no driving source (Pin J1-2, Pin R1-1, Pin U1-7)
Warning	Sheet3.SchDoc	Net USART1_TX has no driving source (Pin FTDI-3, Pin TP2-1, Pin U1-3)


C1
U1
FTDI
TP1
R1
R2
RX
TX
TP2
J1
TP4
C2
TP5
TP3
F1
GND
U2
C3
D1

Sensor Board
Comms
2020-04-07
RevA