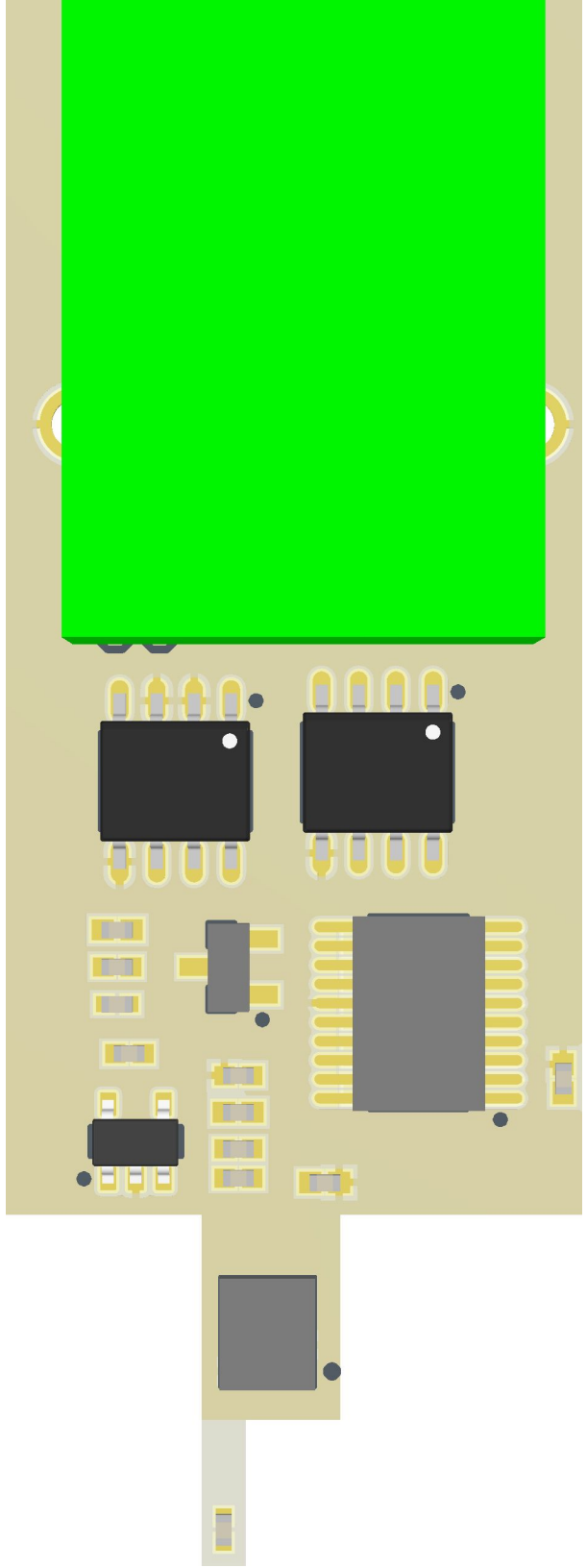
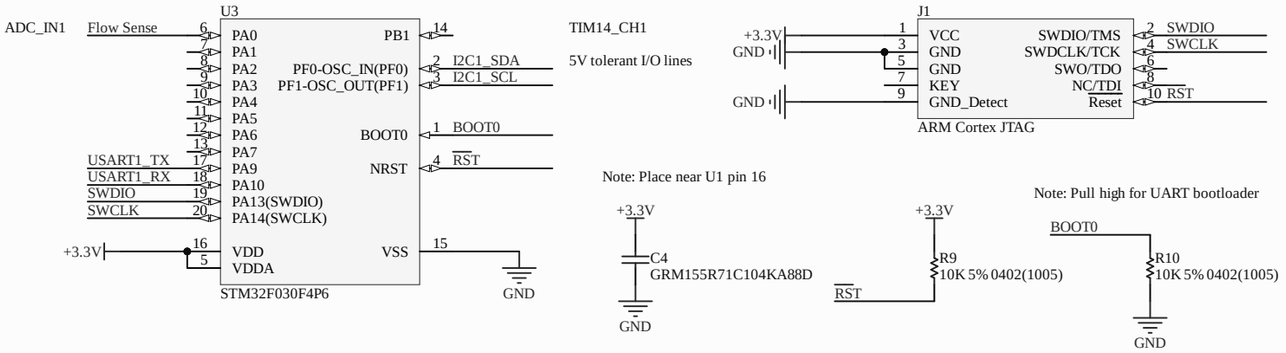
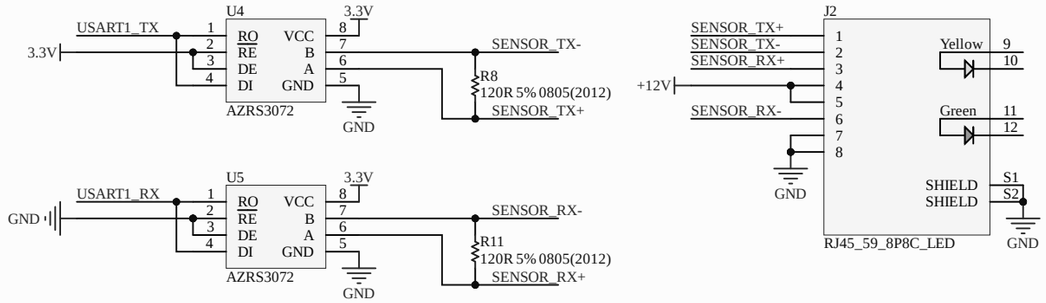


Microcontroller



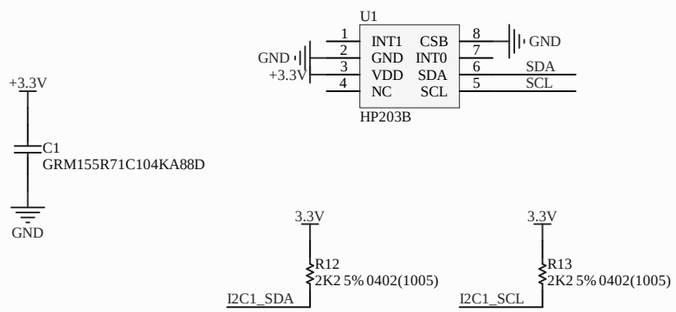
Notes:
-The specific STM32 part is generic, and could be replaced with a similar part from the F0 or F1 family.
-The microcontroller needs to sample an analog value at 200Hz, process it, and then show the results on a monochrome graphical display.
-In particular, it could be advantageous to switch to a part with a USB bootloader for easier field upgrades.

Sensor board connector



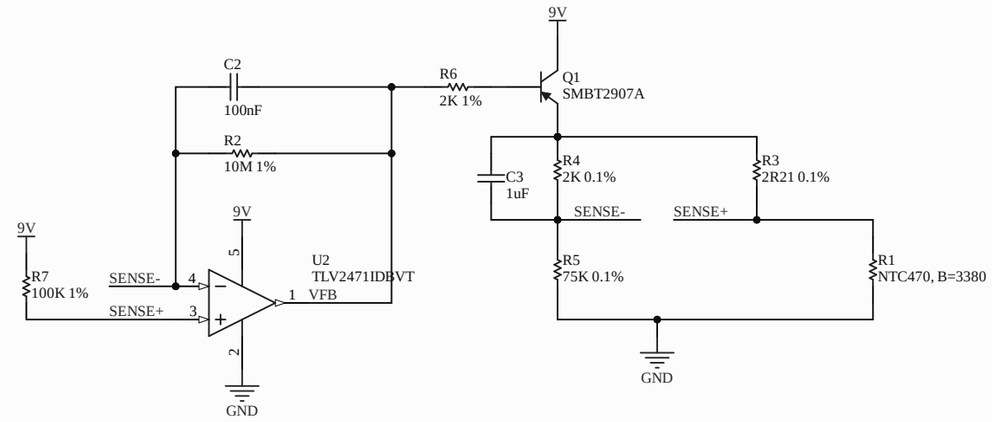
Notes:
-RJ485 Power wiring referenced from passive POE, using pinout from 802.3af Mode B
-RJ45 Data wiring referenced from DMX over Cat5

Pressure Sensor

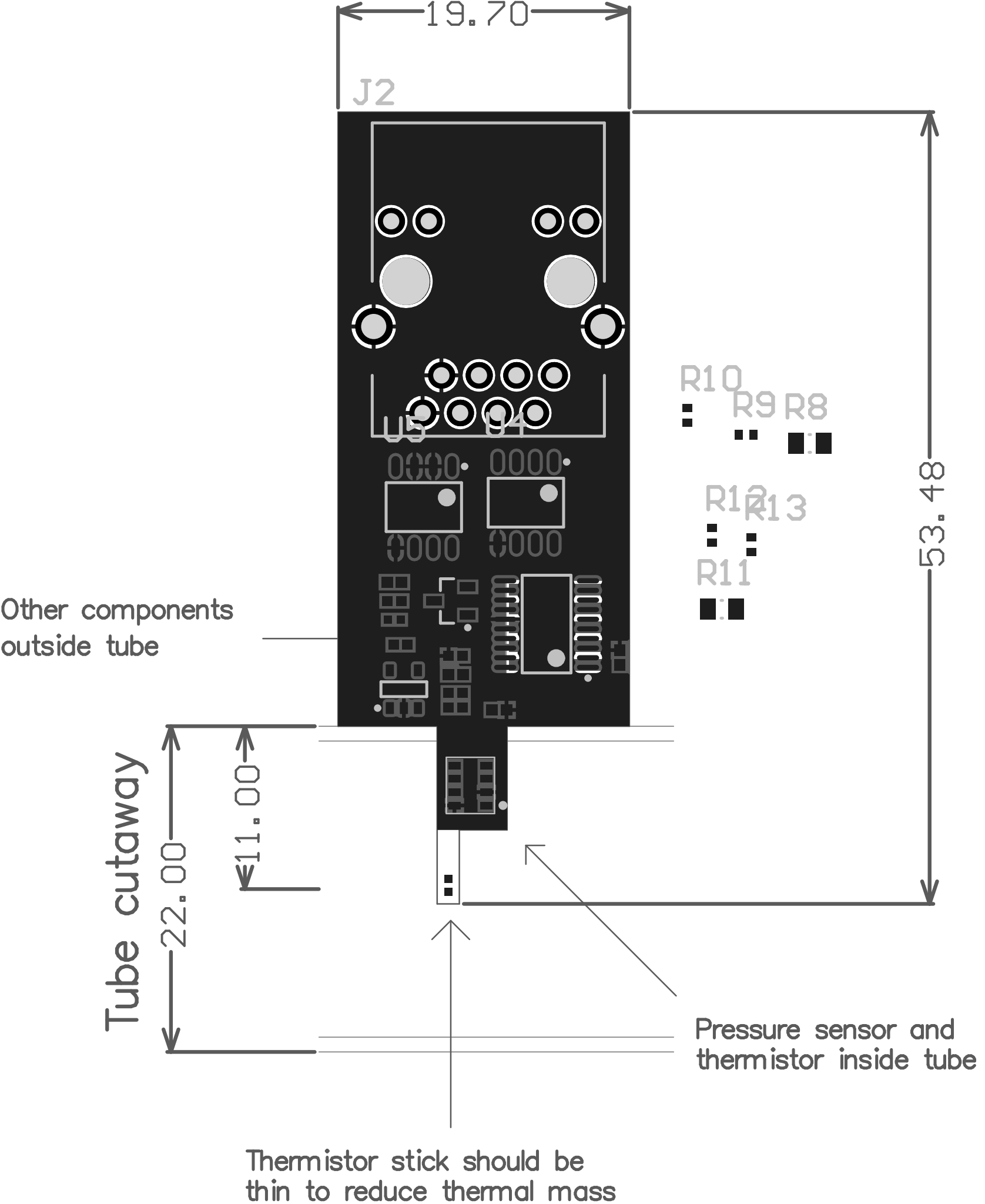


Notes:
-Maximum BIPAP output pressure is 30cm/H20 = 3 kPa
-Sensor should have ideally thousands of counts (?) of sensitivity over this range
-Sensor should withstand high Oxygen environments if possible

Airflow Sensor



Notes:
-Air speed roughly 0 - .5m/s (could adjust by modifying the mechanical port?)
-Thermal response needs to be fast enough to detect .17-.67 Hz tidal flow
-Circuit will be exposed to Oxygen rich environment


19.70
J2
R10
R9
R8
R12
R13
R11
53.48
Other components
outside tube
Tube cutaway
22.00
11.00
Pressure sensor and
thermistor inside tube
Thermistor stick should be
thin to reduce thermal mass

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\sensor_module\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 133

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	50
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.6mm) (Preferred=0.4mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	2
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	45
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	30
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet1 (Bounding Region = (114mm, 100.25mm, 146.25mm, 142mm)	2
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	133

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net +3.3V Between Pad C1-2(124.71mm,117.1mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U1-3(124.33mm,112.45mm) on Top Layer [Unplated] And Pac
Un-Routed Net Constraint: Net VFB Between Pad R2-1(119mm,121.5mm) on Top Layer And Pad C2-1(121.76mm,119.5mm
Un-Routed Net Constraint: Net SENSE- Between Pad R4-1(122.725mm,118.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad R5-2(122.725mm,120.75mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad U2-4(119.7mm,119.775mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad C3-1(118.6mm,125.73mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad C3-2(117.62mm,125.73mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U3-5(131.2mm,122.575mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U3-16(125.6mm,122.575mm) on Top Layer And Pac
Un-Routed Net Constraint: Net \R\S\T Between Pad J1-10(130.95mm,125.24mm) on Bottom Layer And Pad
Un-Routed Net Constraint: Net \R\S\T Between Pad J1-10(130.95mm,125.24mm) on Bottom Layer And Pad
Un-Routed Net Constraint: Net SWDIO Between Pad U3-19(125.6mm,120.625mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SWCLK Between Pad U3-20(125.6mm,119.975mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX+ Between Pad J2-1(128.905mm,139.7mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX+ Between Pad U4-6(126.365mm,128.35mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_TX- Between Pad J2-2(127.635mm,137.16mm) on Multi-Layer And Pad
Un-Routed Net Constraint: Net SENSOR_TX- Between Pad U4-7(127.635mm,128.35mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX+ Between Pad U5-6(119.465mm,128.05mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +12V Between Pad J2-5(123.825mm,139.7mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX- Between Pad U5-7(120.735mm,128.05mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad J2-S1(132.21mm,143mm) on Multi-Layer And Pac
Un-Routed Net Constraint: Net NetQ1_1 Between Pad R6-1(118.56mm,123.19mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad R4-2(121.775mm,118.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad R7-1(118.585mm,124.46mm) on Top Layer And Pac
Un-Routed Net Constraint: Net BOOT0 Between Pad U3-1(131.2mm,119.975mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad R1-1(121.75mm,105.7mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX+ Between Pad U5-6(119.465mm,128.05mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSOR_RX- Between Pad U5-7(120.735mm,128.05mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad R1-2(121.75mm,104.8mm) on Top Layer And Pac
Un-Routed Net Constraint: Net I2C1_SDA Between Pad U3-2(131.2mm,120.625mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad R12-2(139.6mm,128.4mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U4-8(128.905mm,128.35mm) on Top Layer And Pac
Un-Routed Net Constraint: Net I2C1_SCL Between Pad U3-3(131.2mm,121.275mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VFB Between Pad R6-2(117.66mm,123.19mm) on Top Layer And Pad R2-1(119mm,121.5mm
Un-Routed Net Constraint: Net VFB Between Pad U2-1(117.8mm,117.225mm) on Top Layer And Pad R2-1(119mm,121.5mm
Un-Routed Net Constraint: Net SENSE- Between Pad R2-2(118.05mm,121.5mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad U2-3(119.7mm,117.225mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad R3-2(121.775mm,117.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad U2-5(117.8mm,119.775mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad R7-2(117.635mm,124.46mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U3-5(131.2mm,122.575mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad U3-16(125.6mm,122.575mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_TX Between Pad U4-4(125.095mm,133.85mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_RX Between Pad U5-1(122.005mm,133.55mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_TX Between Pad U4-4(125.095mm,133.85mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U4-3(126.365mm,133.85mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U4-2(127.635mm,133.85mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 3.3V Between Pad U5-8(122.005mm,128.05mm) on Top Layer And Pac
Un-Routed Net Constraint: Net USART1_RX Between Pad U5-4(118.195mm,133.55mm) on Top Layer And Pac

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS1(130.025mm,146.05mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J2-POS2(118.895mm,146.05mm) on Multi-Layer Actual Hole Size = 3.2mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(125.69mm,117.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C2-1(121.76mm,119.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(118.6mm,125.73mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(133.35mm,121.14mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(137.9mm,137.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(121.75mm,105.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R12-1(139.6mm,129.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R13-1(142.24mm,128.77mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R2-1(119mm,121.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.154mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.154mm < 0.254mm) Between Pad R3-2(121.775mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-2(121.775mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R4-1(122.725mm,118.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R5-1(121.775mm,120.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R6-1(118.56mm,123.19mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R7-1(118.585mm,124.46mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R9-1(142.4mm,135.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-2(124.33mm,111.55mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-3(124.33mm,112.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-6(122.17mm,112.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-7(122.17mm,111.55mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-1(117.8mm,117.225mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-2(118.75mm,117.225mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-1(131.2mm,119.975mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-10(131.2mm,125.825mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-11(125.6mm,125.825mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-12(125.6mm,125.175mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-13(125.6mm,124.525mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-14(125.6mm,123.875mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-15(125.6mm,123.225mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-16(125.6mm,122.575mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-17(125.6mm,121.925mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-18(125.6mm,121.275mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-19(125.6mm,120.625mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-2(131.2mm,120.625mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-3(131.2mm,121.275mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-4(131.2mm,121.925mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-5(131.2mm,122.575mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-6(131.2mm,123.225mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-7(131.2mm,123.875mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-8(131.2mm,124.525mm) on Top Layer And

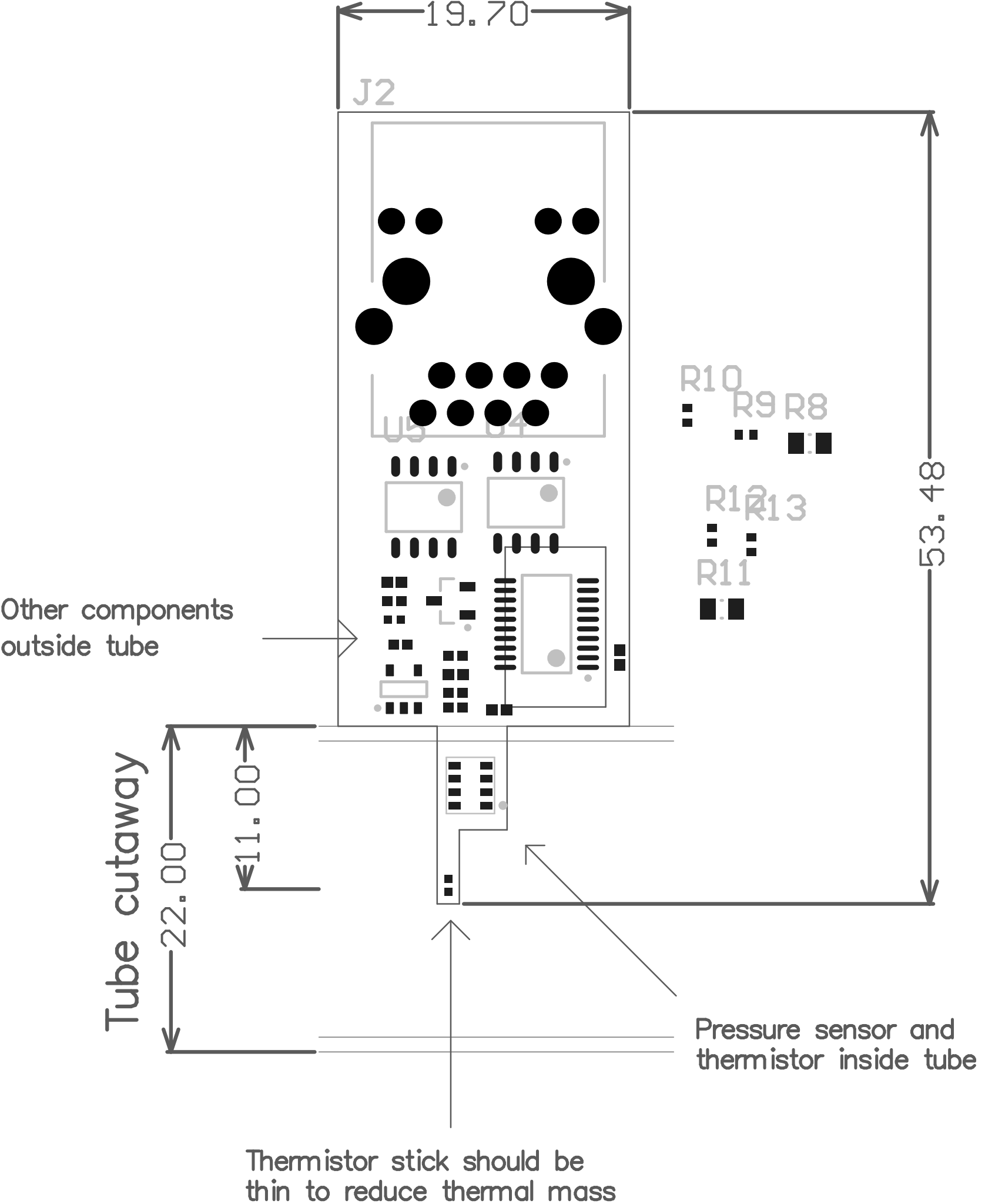
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(127.05mm,120.16mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(127.05mm,120.16mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-10(130.95mm,125.24mm) on Bottom
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(130.95mm,125.24mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(130.95mm,120.16mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(130.95mm,120.16mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(127.05mm,121.43mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(130.95mm,121.43mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(127.05mm,122.7mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(130.95mm,122.7mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(127.05mm,123.97mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(130.95mm,123.97mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(127.05mm,125.24mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(127.05mm,125.24mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.025mm < 0.254mm) Between Pad J2-2(127.635mm,137.16mm) on Multi-Laye
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad J2-4(125.095mm,137.16mm) on Multi-Laye
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad J2-8(120.015mm,137.16mm) on Multi-Laye
Silk To Solder Mask Clearance Constraint: (0.229mm < 0.254mm) Between Pad R13-2(142.24mm,127.77mm) on Top Laye
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-2(124.33mm,111.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-3(124.33mm,112.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-4(124.33mm,113.35mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-4(124.33mm,113.35mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-6(122.17mm,112.45mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-7(122.17mm,111.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-8(122.17mm,110.65mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-8(122.17mm,110.65mm) on Top Layer An

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R10" (137.633mm,138.74mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R12" (139.333mm,130.64mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "U4" (124.419mm,135.598mm) on Top Overlay An
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "U5" (117.529mm,135.3mm) on Top Overlay An

Room Sheet1 (Bounding Region = (114mm, 100.25mm, 146.25mm, 142mm) (InComponentClass('She
Room Definition: Between Component J2-RJ45_59_8P8C_LED (124.46mm,146.05mm) on Top Layer And Room Sheet1
Room Definition: Between Room Sheet1 (Bounding Region = (114mm, 100.25mm, 146.25mm, 142mm)

Electrical Rules Check Report

Class	Document	Message
Error	Sheet1.SchDoc	Net Flow Sense has only one pin (Pin U3-6)
Error	Sheet1.SchDoc	Net SCL has only one pin (Pin U1-5)
Error	Sheet1.SchDoc	Net SDA has only one pin (Pin U1-6)
Warning	Sheet1.SchDoc	Net BOOT0 has no driving source (Pin R10-1, Pin U3-1)
Warning	Sheet1.SchDoc	Net SENSE+ has no driving source (Pin R1-2, Pin R3-1, Pin R7-2, Pin U2-3)
Warning	Sheet1.SchDoc	Net SENSE- has no driving source (Pin C2-2, Pin C3-2, Pin R2-2, Pin R4-1, Pin R5-2, Pin U2-4)


19.70
J2
R10
R9
R8
U5
U4
R12
R13
R11
53.48
Other components
outside tube
Tube cutaway
22.00
11.00
Pressure sensor and
thermistor inside tube
Thermistor stick should be
thin to reduce thermal mass