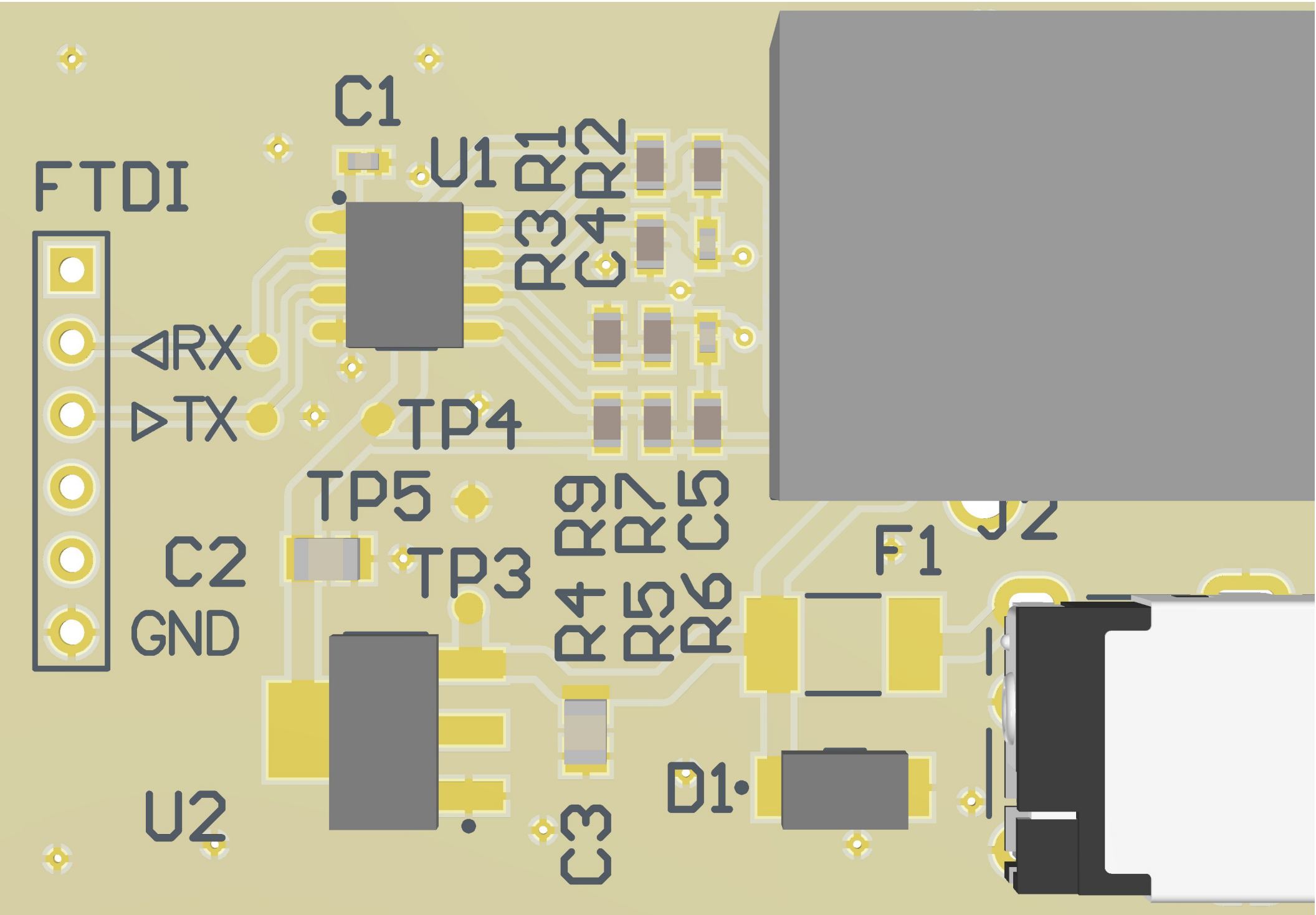
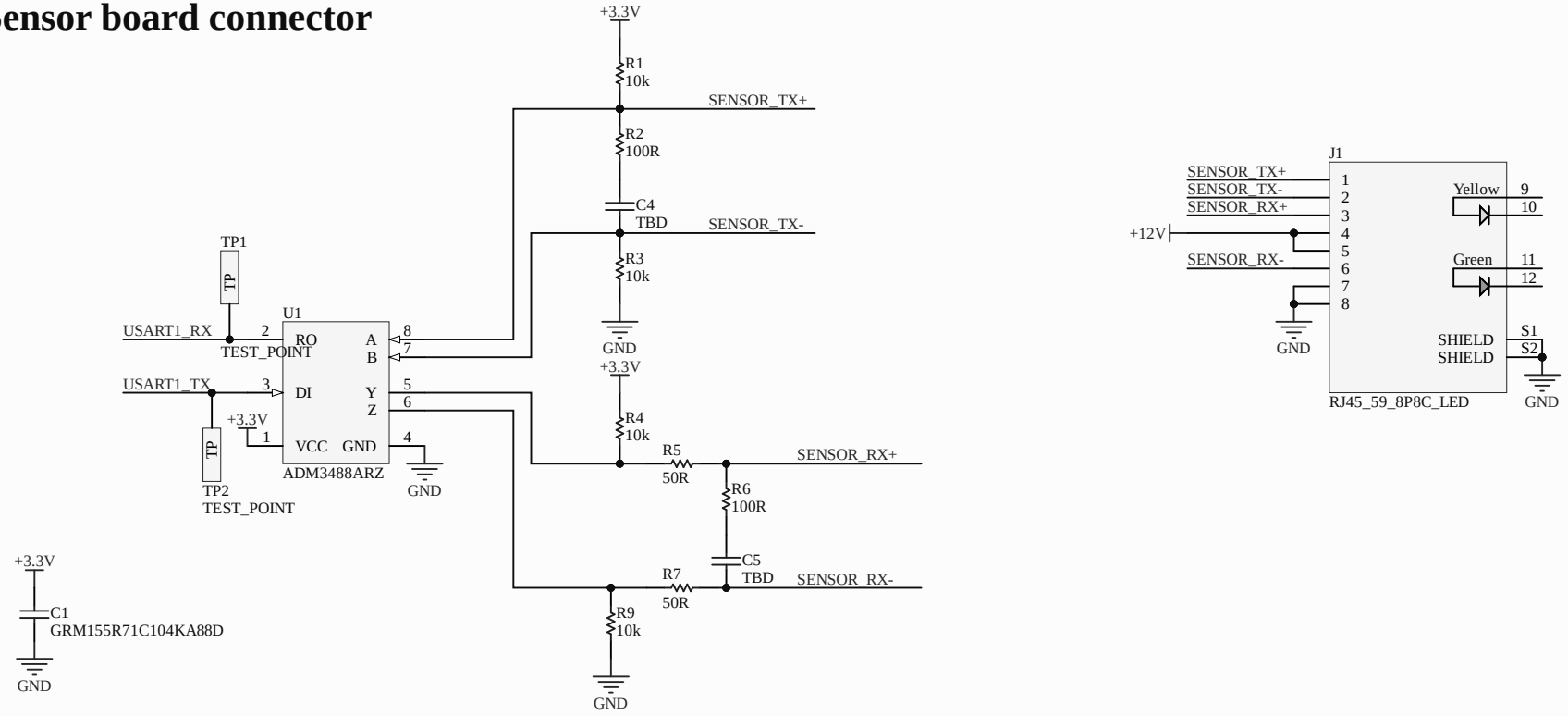
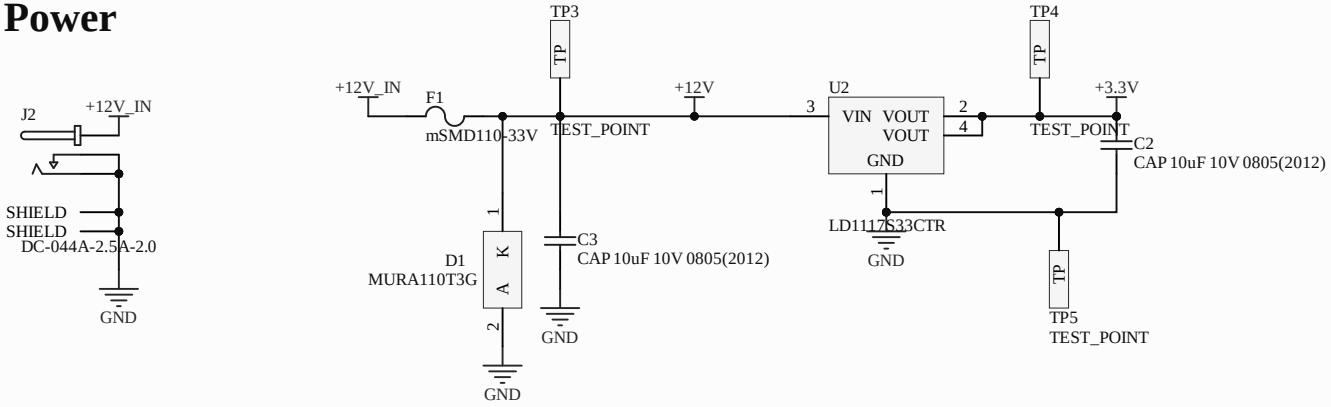

C1
U1
R1
R2
R3
C4
FTDI
RX
TX
TP4
TP5
C2
GND
TP3
R4
R9
R7
C5
R5
R6
F1
U2
C3
D1

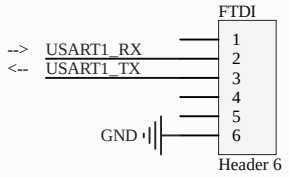
Sensor board connector

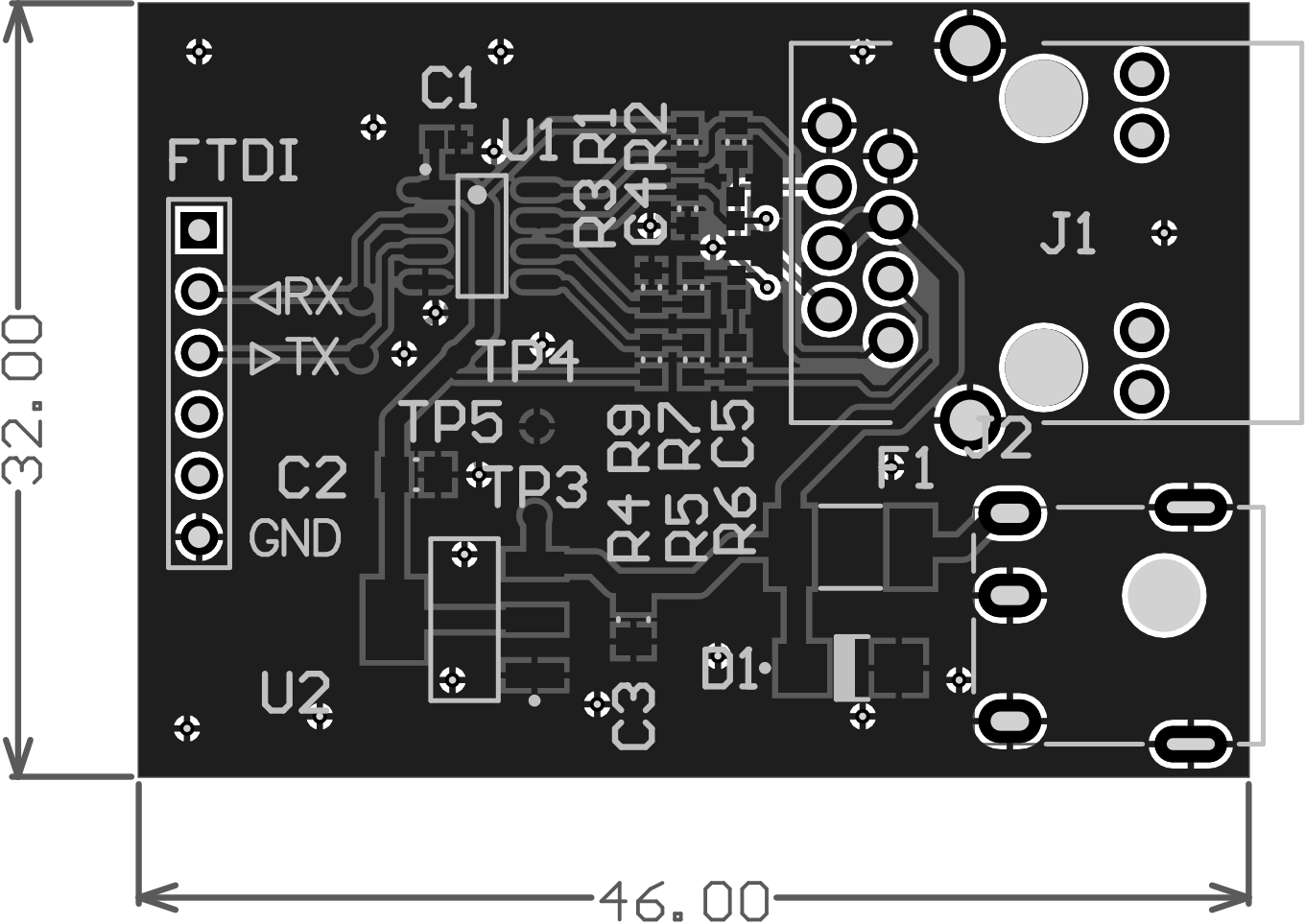


Power



FTDI




C1
U1
R1
R2
R3
R4
FTDI
RX
TX
TP4
TP5
TP3
C2
GND
R9
R7
C5
R4
R5
R6
J1
J2
F1
D1
U2
C3
32.00
46.00

Design Rules Verification Report

Filename : C:\Users\matt\Other-Repos\sensor_module\sensor_to_uart\sensor_to_uart.PcbD

Warnings 0
Rule Violations 59

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	3
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.8mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	3
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	4
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	46
Silk to Silk (Clearance=0.254mm) (All),(All)	3
Net Antennae (Tolerance=0mm) (All)	0
Room sensor_to_uart (Bounding Region = (102.5mm, 90mm, 152.5mm, 125.503mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	59

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(13.225mm,26.375mm) on Top Layer And Pac
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C4-1(24.75mm,23.01mm) on Top Layer And Pac
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C5-1(24.75mm,20.74mm) on Top Layer And Pac

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS1(37.5mm,16.935mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad J1-POS2(37.5mm,28.065mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3mm > 2.54mm) Pad J2-MNT(42.5mm,7.5mm) on Multi-Layer Actual Hole Size = 3mm

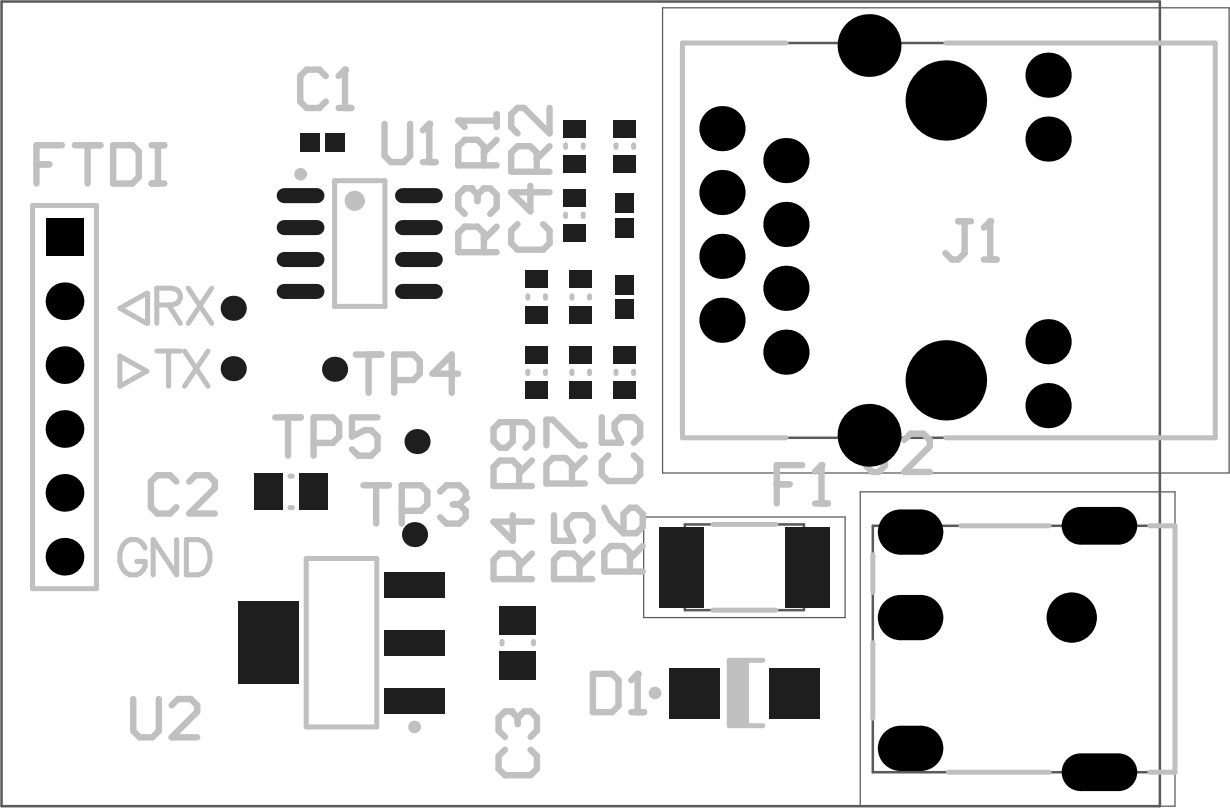
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(13.225mm,26.375mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(24.75mm,23.01mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C5-1(24.75mm,20.74mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.155mm < 0.254mm) Between Pad R7-1(23mm,20.95mm) on Top Layer And Via

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(12.4mm,12.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-1(12.4mm,12.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(10.6mm,12.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(10.6mm,12.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(20.5mm,5.6mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-1(20.5mm,5.6mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C3-2(20.5mm,7.4mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C3-2(20.5mm,7.4mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad J1-S1(34.45mm,14.75mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(22.75mm,26.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R1-1(22.75mm,26.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(22.75mm,25.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(22.75mm,25.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-1(24.75mm,26.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R2-1(24.75mm,26.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(24.75mm,25.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R2-2(24.75mm,25.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-1(22.75mm,24.2mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R3-1(22.75mm,24.2mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-2(22.75mm,22.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R3-2(22.75mm,22.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-1(21.25mm,16.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-1(21.25mm,16.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R4-2(21.25mm,17.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R4-2(21.25mm,17.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-1(23mm,16.55mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-1(23mm,16.55mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R5-2(23mm,17.95mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R5-2(23mm,17.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-1(24.75mm,16.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-1(24.75mm,16.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R6-2(24.75mm,17.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R6-2(24.75mm,17.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-1(23mm,20.95mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R7-1(23mm,20.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-2(23mm,19.55mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R7-2(23mm,19.55mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R9-1(21.25mm,19.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R9-1(21.25mm,19.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R9-2(21.25mm,20.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R9-2(21.25mm,20.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.06mm < 0.254mm) Between Pad TP3-1(16.4mm,10.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-1(16.4mm,4.2mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-2(16.4mm,6.5mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-3(16.4mm,8.8mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U2-4(10.6mm,6.5mm) on Top Layer And Trac

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "<RX" (4.5mm,19mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text ">TX" (4.5mm,16.5mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "R5" (23.462mm,9.03mm) on Top Overlay And Te

Electrical Rules Check Report

Class	Document	Message
Warning	sensor_to_uart.SchDoc	Net SENSOR_TX+ has no driving source (Pin J1-1, Pin R1-2, Pin R2-1, Pin U1-8)
Warning	sensor_to_uart.SchDoc	Net SENSOR_TX- has no driving source (Pin C4-1, Pin J1-2, Pin R3-1, Pin U1-7)
Warning	sensor_to_uart.SchDoc	Net USART1_TX has no driving source (Pin FTDI-3, Pin TP2-1, Pin U1-3)


C1
U1
R1
R2
R3
C4
FTDI
RX
TX
TP4
TP5
C2
TP3
GND
R9
R7
C5
R4
R5
R6
F1
J2
J1
U2
C3
D1

Sensor Board
Comms
2020-04-14
RevB