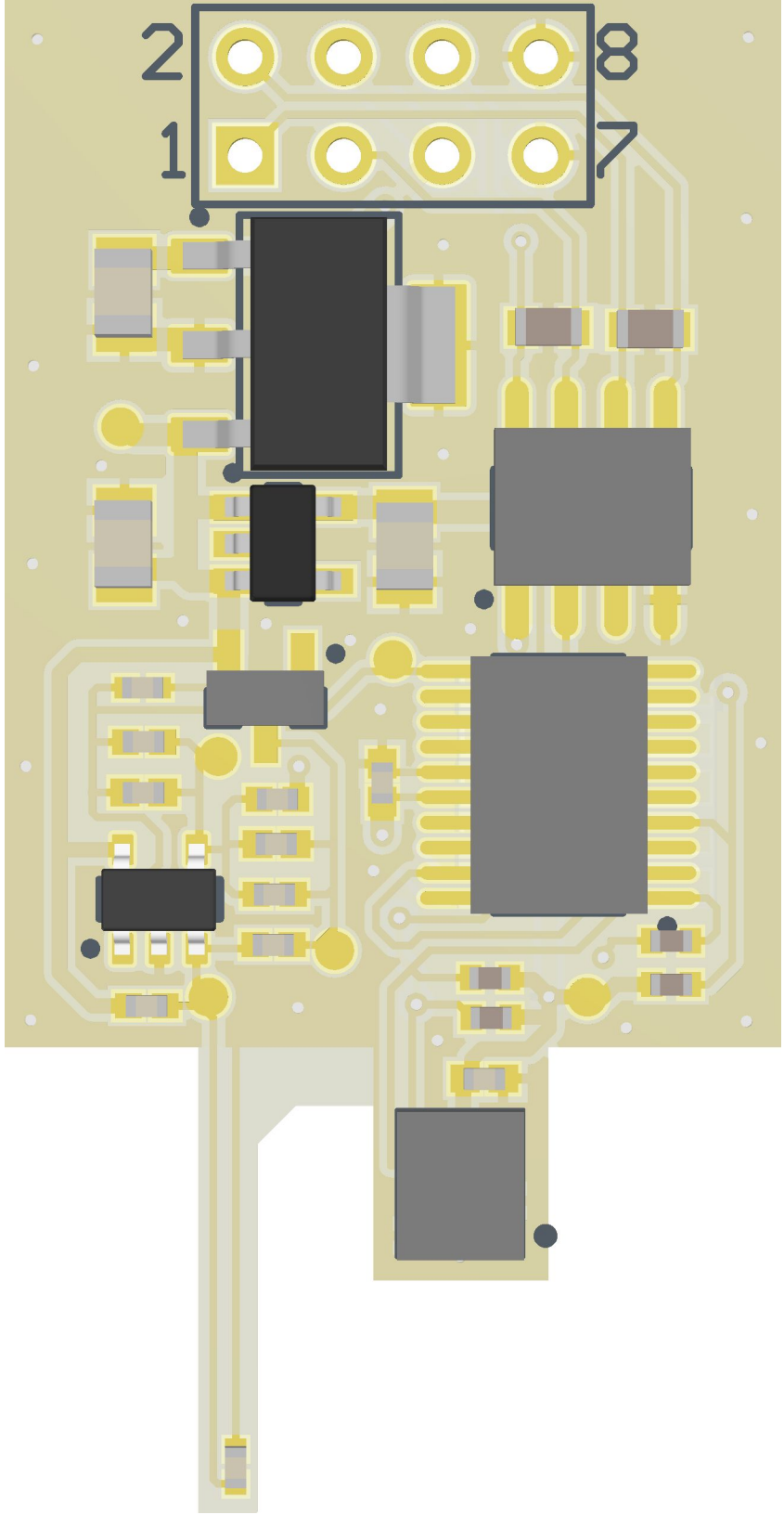
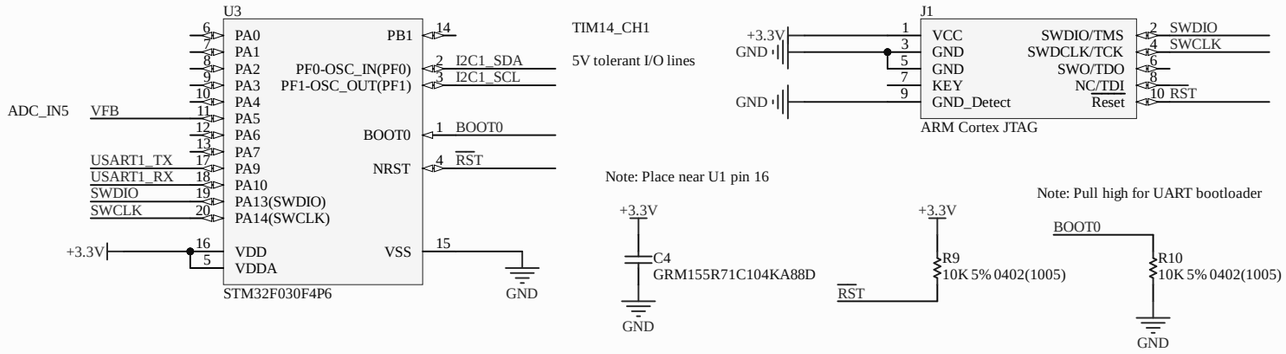
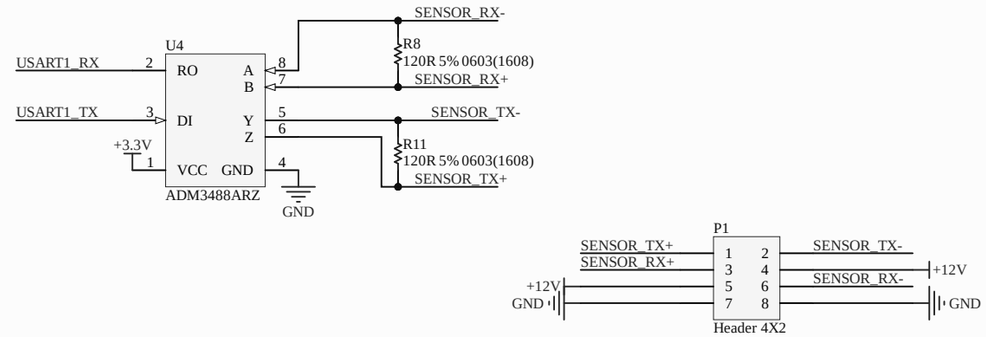

2
8
1
7

Microcontroller



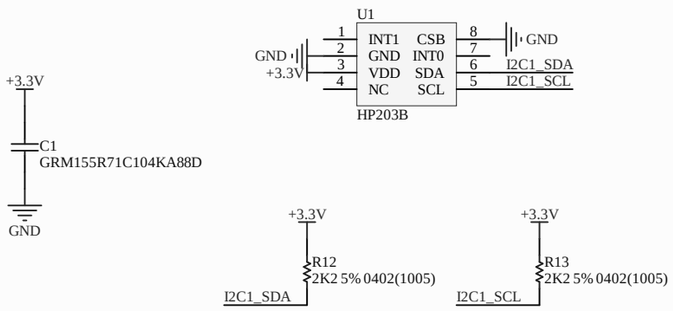
Notes:
-The specific STM32 part is generic, and could be replaced with a similar part from the F0 or F1 family.
-The microcontroller needs to sample an analog value at 200Hz, process it, and then show the results on a monochrome graphical display.
-In particular, it could be advantageous to switch to a part with a USB bootloader for easier field upgrades.

Sensor board connector



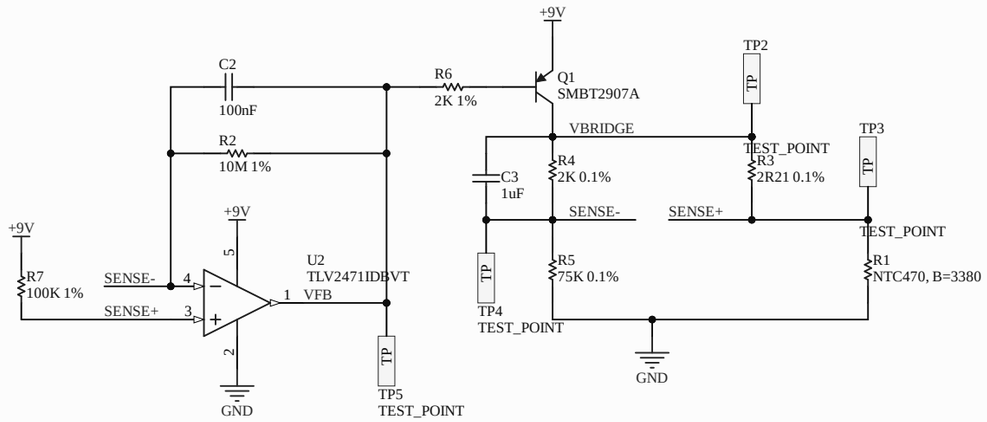
Notes:
-RJ485 Power wiring referenced from passive POE, using pinout from 802.3af Mode B
-RJ45 Data wiring referenced from DMX over Cat5

Pressure Sensor



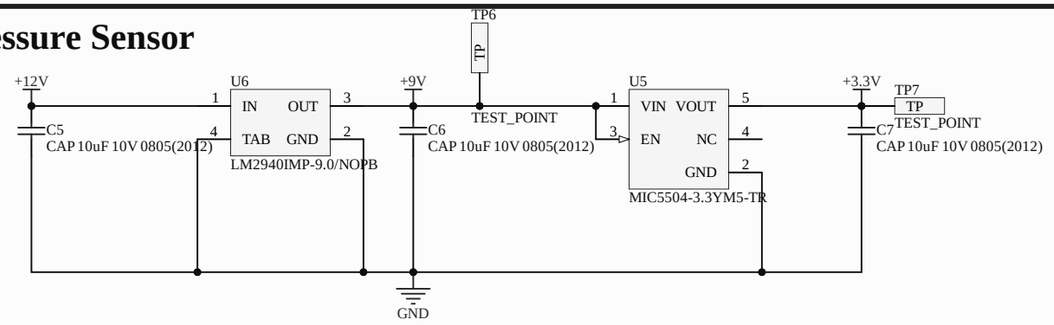
Notes:
-Maximum BIPAP output pressure is 30cm/H20 = 3 kPa
-Sensor should have ideally thousands of counts (?) of sensitivity over this range
-Sensor should withstand high Oxygen environments if possible

Airflow Sensor

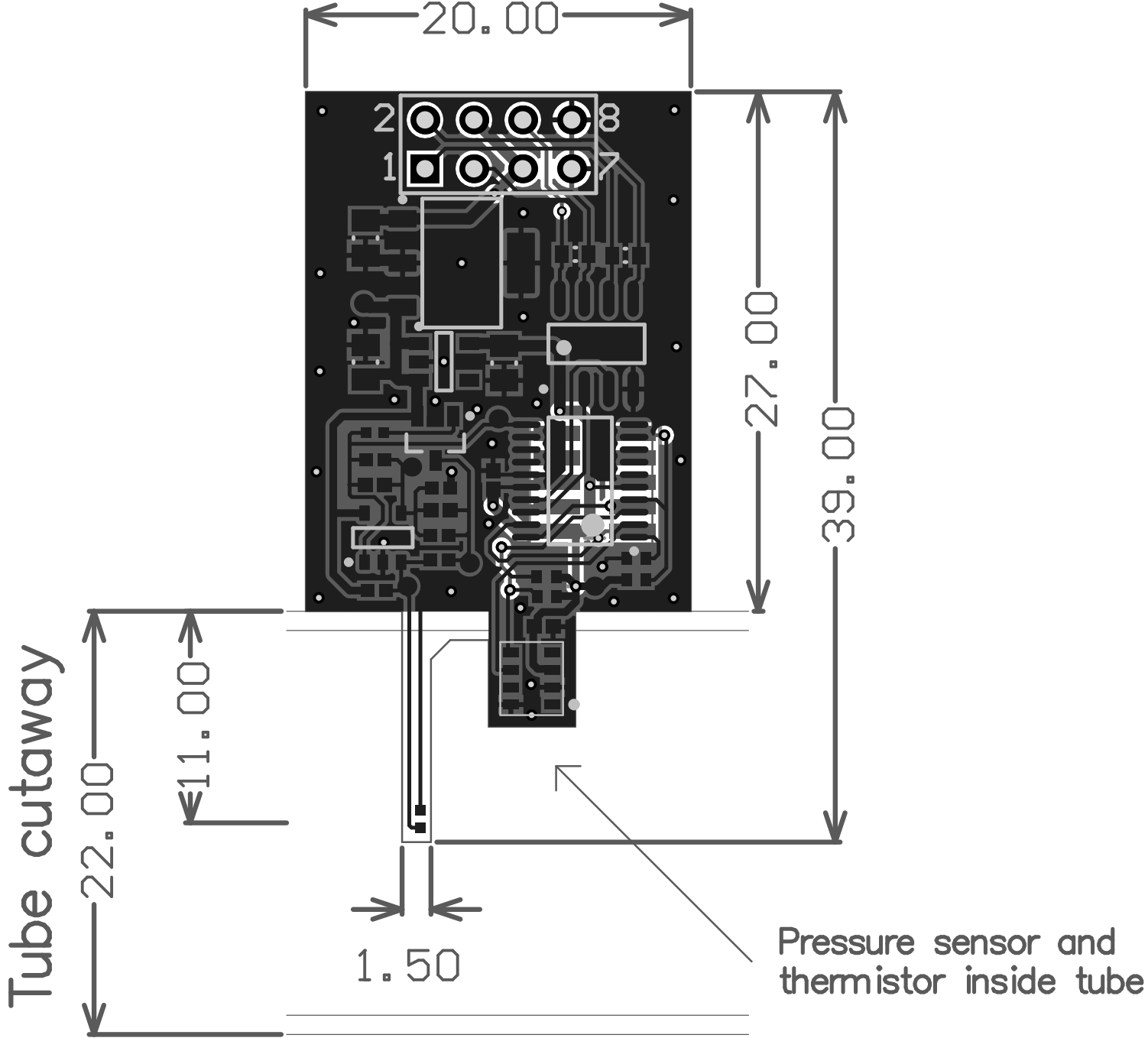


Notes:
-Air speed roughly 0 - .5m/s (could adjust by modifying the mechanical port?)
-Thermal response needs to be fast enough to detect .17-.67 Hz tidal flow
-Circuit will be exposed to Oxygen rich environment

Pressure Sensor



Notes:
-C5 must be replaced with a proper part- similar to 25V, 22uF
-C6 must be replaced with a proper part - similar to 25V, 22uF
-U6 might be hard to source, consider replacing
-U5 could replace with China local part


20.00
2
8
1
7
27.00
39.00
Tube cutaway
22.00
11.00
1.50
Pressure sensor and
thermistor inside tube

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\sensor_module\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 108

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.6mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	50
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	54
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet1 (Bounding Region = (114mm, 104mm, 134mm, 143mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	108

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(-7.16mm,-0.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C2-1(-16.89mm,6.575mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(-12.51mm,5.25mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(-10.275mm,7.315mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.254mm) Between Pad Q1-3(-13.275mm,7.85mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(-2.35mm,2.75mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(-14.05mm,-10.35mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R12-1(-8mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.254mm) Between Pad R12-1(-8mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.254mm) Between Pad R12-2(-7mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R13-1(-7.975mm,0.775mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R2-1(-16.875mm,7.875mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R3-1(-13.55mm,2.65mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R3-2(-12.6mm,2.65mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R4-1(-13.525mm,3.95mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R5-1(-12.5mm,6.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R6-1(-15.975mm,9.275mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R7-1(-16.8mm,1.075mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.053mm < 0.254mm) Between Pad R7-2(-15.85mm,1.075mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R9-1(-3.35mm,1.625mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.149mm < 0.254mm) Between Pad TP3-1(-14.744mm,1.302mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad TP5-1(-10mm,10mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-1(-7.19mm,-4.85mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-2(-7.19mm,-3.95mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-3(-7.19mm,-3.05mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-5(-9.35mm,-2.15mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-6(-9.35mm,-3.05mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-7(-9.35mm,-3.95mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-1(-16.95mm,2.55mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-2(-16mm,2.55mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-1(-2.95mm,3.85mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-10(-2.95mm,9.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-11(-8.55mm,9.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-12(-8.55mm,9.05mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-13(-8.55mm,8.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-14(-8.55mm,7.75mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-15(-8.55mm,7.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-16(-8.55mm,6.45mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-17(-8.55mm,5.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-18(-8.55mm,5.15mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-19(-8.55mm,4.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-2(-2.95mm,4.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-3(-2.95mm,5.15mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-4(-2.95mm,5.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-5(-2.95mm,6.45mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-6(-2.95mm,7.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-7(-2.95mm,7.75mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U3-8(-2.95mm,8.4mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.087mm < 0.254mm) Between Pad U5-1(-14.125mm,13.925mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.087mm < 0.254mm) Between Pad U5-2(-14.125mm,12.975mm) on Top Layer Anc

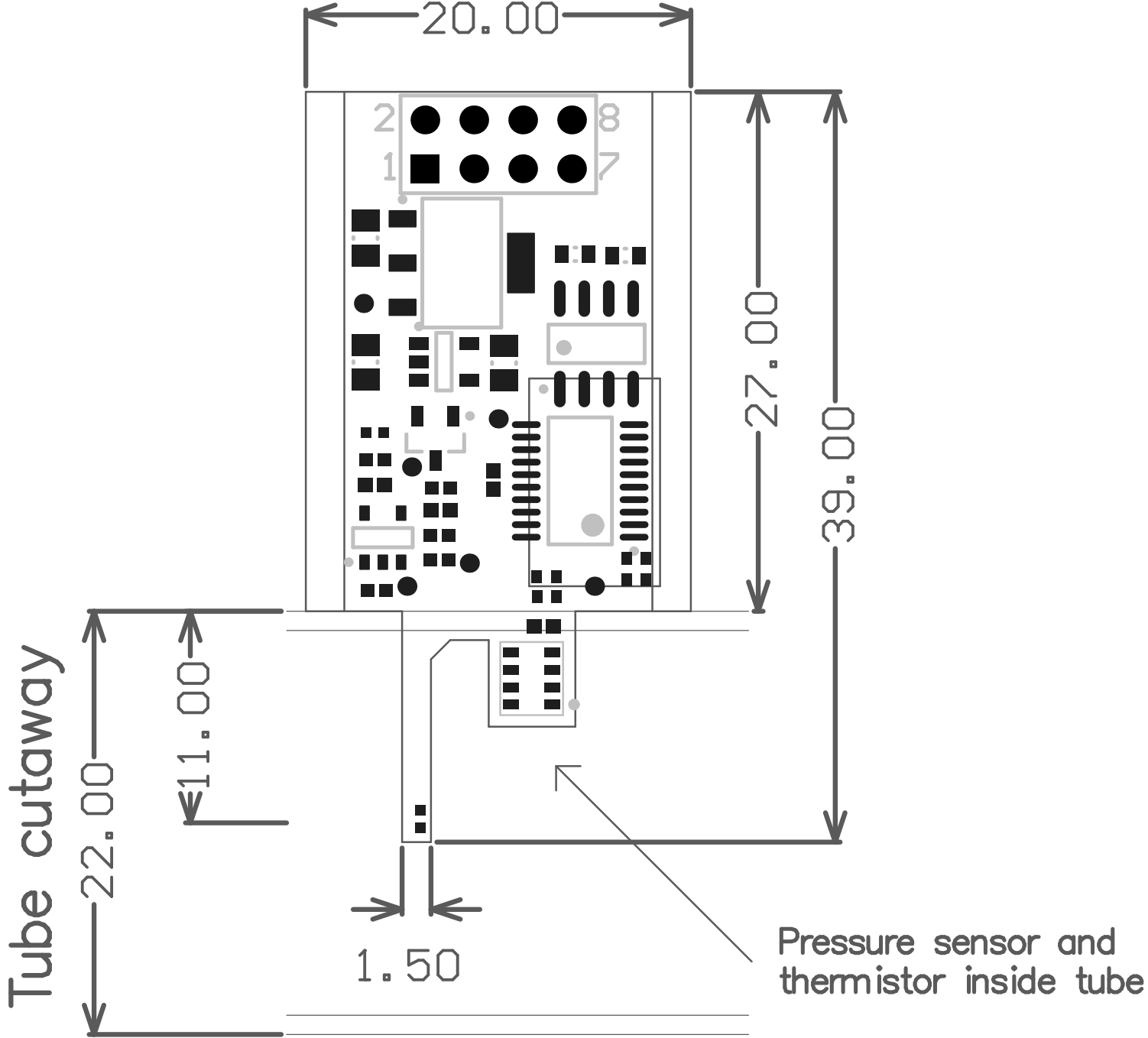
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.079mm < 0.254mm) Between Arc (-2.95mm,3.125mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (-2.95mm,3.125mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-1(-16.9mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-1(-16.9mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C5-2(-16.9mm,20.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-2(-16.9mm,20.3mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C6-1(-16.9mm,13.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C6-1(-16.9mm,13.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C6-2(-16.9mm,12.05mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C6-2(-16.9mm,12.05mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C7-1(-9.7mm,12mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C7-1(-9.7mm,12mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C7-2(-9.7mm,13.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C7-2(-9.7mm,13.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(-6.95mm,4.16mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(-6.95mm,4.16mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(-3.05mm,9.24mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-10(-3.05mm,9.24mm) on Bottom Laye
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(-3.05mm,4.16mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(-3.05mm,4.16mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(-6.95mm,5.43mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(-3.05mm,5.43mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(-6.95mm,6.7mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(-3.05mm,6.7mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(-6.95mm,7.97mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(-3.05mm,7.97mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(-6.95mm,9.24mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(-6.95mm,9.24mm) on Bottom Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R11-1(-4.1mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R11-1(-4.1mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R11-2(-2.7mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R11-2(-2.7mm,18.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-1(-5.3mm,18.555mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R8-1(-5.3mm,18.555mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-2(-6.7mm,18.555mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R8-2(-6.7mm,18.555mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.232mm < 0.254mm) Between Pad TP4-1(-14.5mm,7.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad TP4-1(-14.5mm,7.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-1(-7.19mm,-4.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-1(-7.19mm,-4.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-2(-7.19mm,-3.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-3(-7.19mm,-3.05mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-4(-7.19mm,-2.15mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-4(-7.19mm,-2.15mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-5(-9.35mm,-2.15mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-5(-9.35mm,-2.15mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-6(-9.35mm,-3.05mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-7(-9.35mm,-3.95mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-8(-9.35mm,-4.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-8(-9.35mm,-4.85mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U6-1(-14.975mm,20.4mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U6-2(-14.975mm,18.1mm) on Top Layer An

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U6-3(-14.975mm,15.8mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.22mm < 0.254mm) Between Pad U6-4(-8.825mm,18.1mm) on Top Layer An

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.137mm < 0.254mm) Between Text "1" (-15.842mm,22.492mm) on Top Overlay An
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "2" (-16.35mm,25.032mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "7" (-4.666mm,22.492mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "8" (-4.666mm,25.032mm) on Top Overlay And Trac

Electrical Rules Check Report

Class	Document	Message
Warning	Sheet1.SchDoc	Net BOOT0 has no driving source (Pin R10-1, Pin U3-1)
Warning	Sheet1.SchDoc	Net SENSE+ has no driving source (Pin R1-2, Pin R3-1, Pin R7-2, Pin TP3-1, Pin U2-3)
Warning	Sheet1.SchDoc	Net SENSE- has no driving source (Pin C2-2, Pin C3-2, Pin R2-2, Pin R4-1, Pin R5-2, Pin TP4-1, Pin U2-4)
Warning	Sheet1.SchDoc	Net SENSOR_RX+ has no driving source (Pin P1-3, Pin R8-1, Pin U4-7)
Warning	Sheet1.SchDoc	Net SENSOR_RX- has no driving source (Pin P1-6, Pin R8-2, Pin U4-8)
Warning	Sheet1.SchDoc	VFB contains IO Pin and Output Pin objects (Pin U3-11, Pin U2-1).


20.00
2
8
1
7
27.00
39.00
Tube cutaway
22.00
11.00
1.50
Pressure sensor and
thermistor inside tube

Sensor Module
2020-04-05
RevD