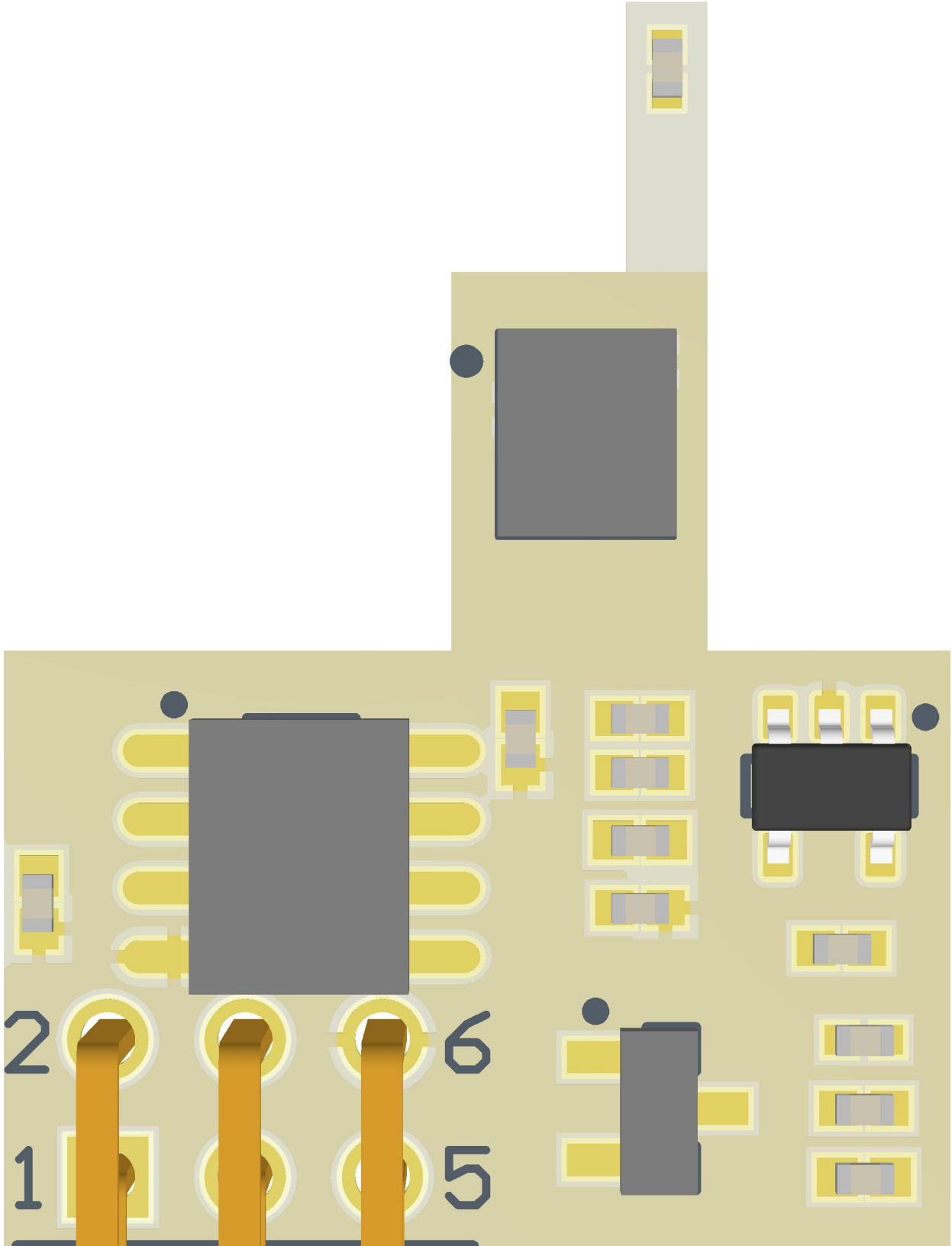
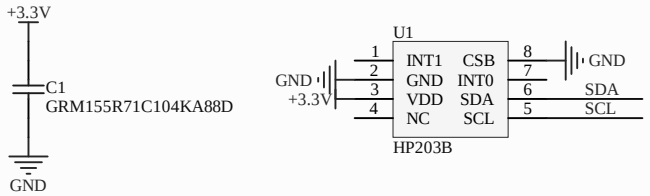
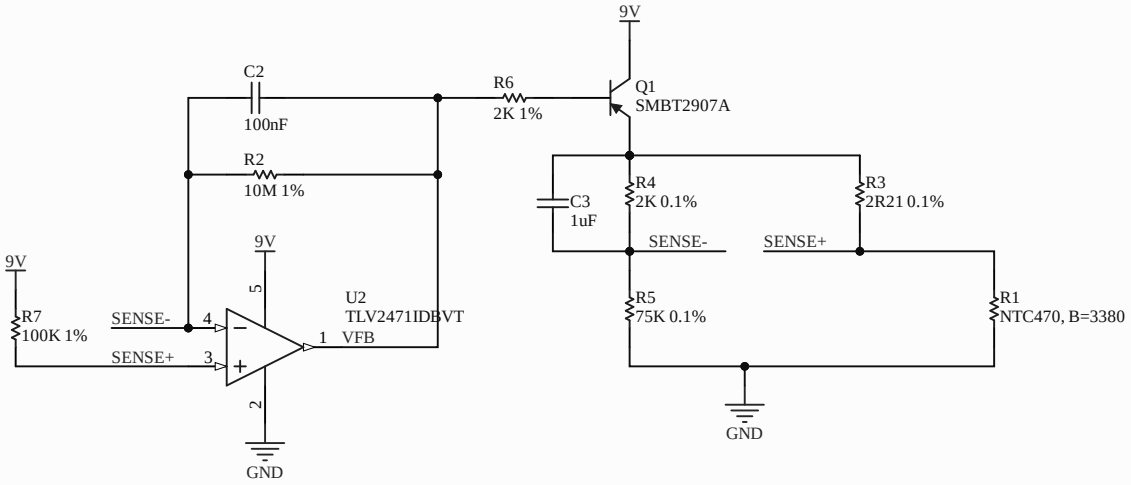

2
6
1
5

Pressure Sensor



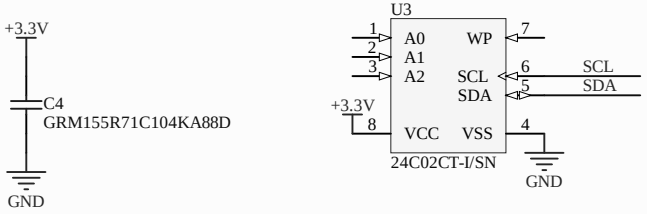
Pressure sensor notes:
-Maximum BIPAP output pressure is 30cm/H20 = 3 kPa
-Sensor should have ideally thousands of counts (?) of sensitivity over this range
-Sensor should withstand high Oxygen environments if possible

Airflow Sensor



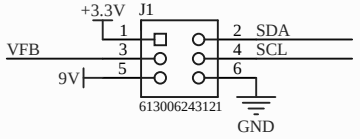
Notes:
-Air speed roughly 0 - .5m/s (could adjust by modifying the mechanical port?)
-Thermal response needs to be fast enough to detect .17-.67 Hz tidal flow
-Circuit will be exposed to Oxygen rich environment

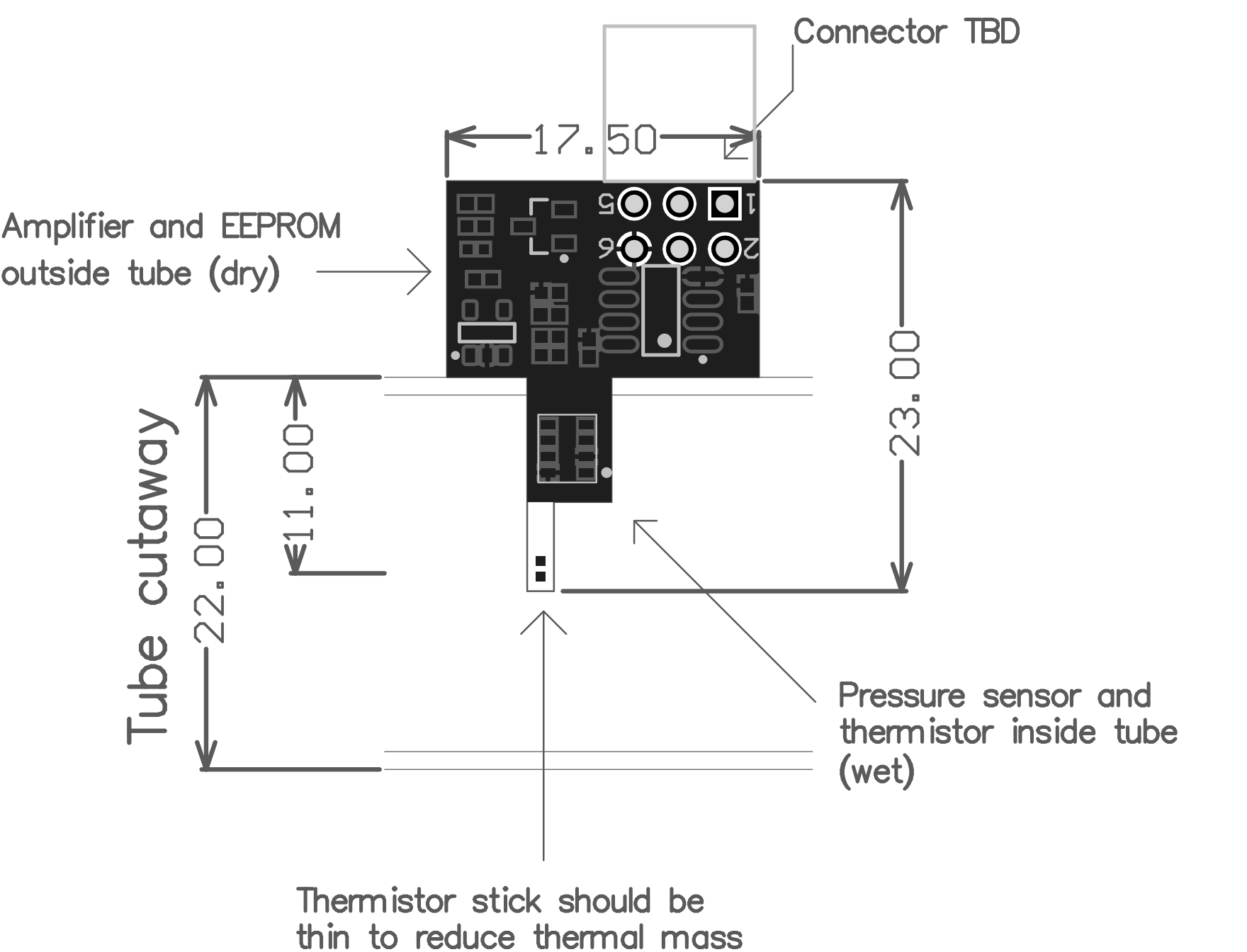
Calibration Data EEPROM



Notes:
-Part is a standin for a generic I2C memory
-Needs <1K of calibration space

Connector (placeholder)




Connector TBD
17.50
Amplifier and EEPROM
outside tube (dry)
23.00
Tube cutaway
22.00
11.00
Pressure sensor and
thermistor inside tube
(wet)
Thermistor stick should be
thin to reduce thermal mass

Design Rules Verification Report

Filename : C:\Users\matt\Dropbox\Ventilator Shit\PCB\sensor_module\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 69

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	28
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.6mm) (Preferred=0.4mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	25
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	16
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet1 (Bounding Region = (114mm, 100.25mm, 146.25mm, 142mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	69

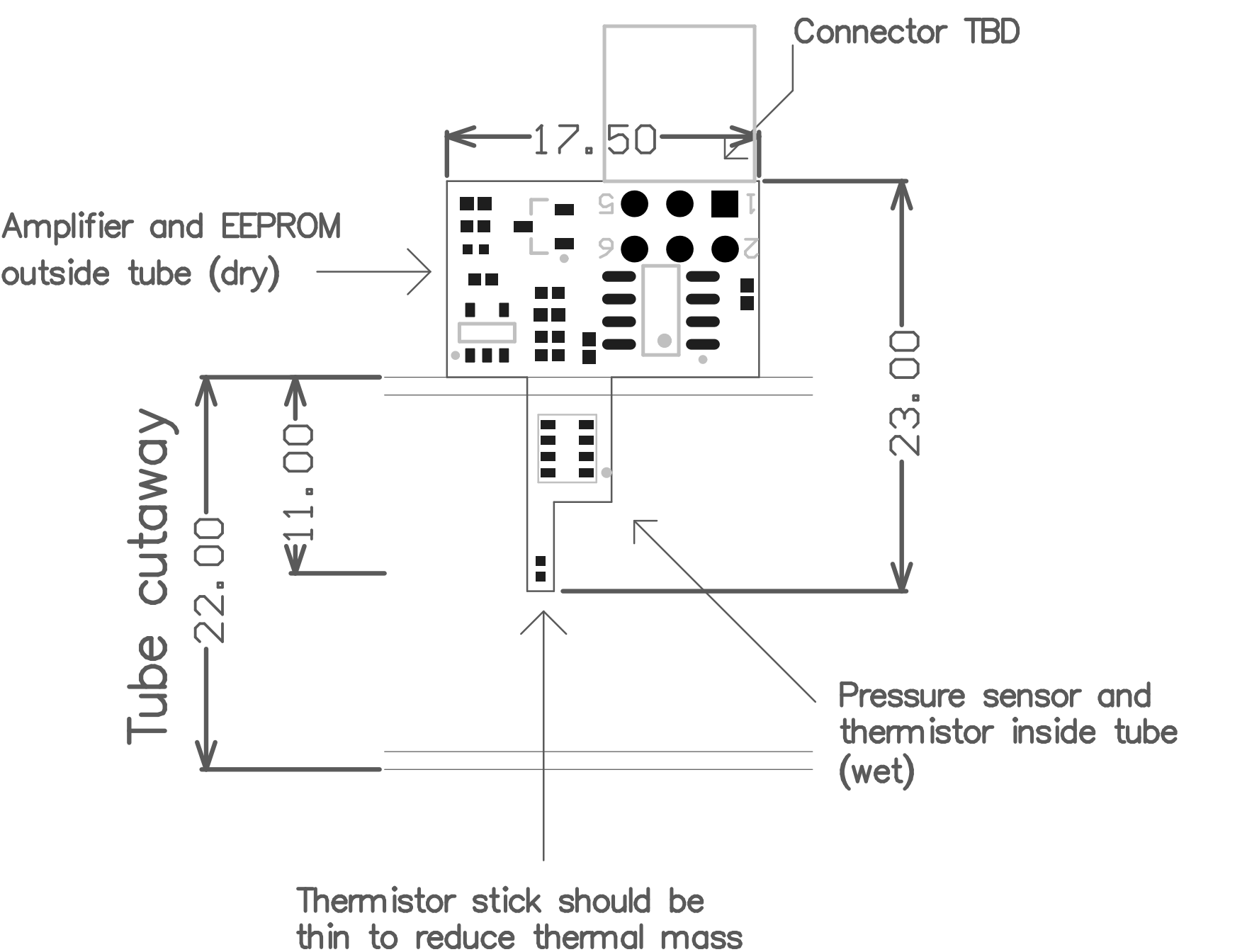
Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net +3.3V Between Pad U1-3(124.33mm,112.45mm) on Top Layer [Unplated] And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad C1-2(124.46mm,117.13mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VFB Between Pad C2-1(121.76mm,119.5mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VFB Between Pad R2-1(119mm,121.5mm) on Top Layer And Pad C2-1(121.76mm,119.5mm
Un-Routed Net Constraint: Net SENSE- Between Pad R4-1(122.725mm,118.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad R5-2(122.725mm,120.75mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad U2-4(119.7mm,119.775mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad C3-1(118.6mm,125.73mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE- Between Pad C3-2(117.62mm,125.73mm) on Top Layer And Pac
Un-Routed Net Constraint: Net +3.3V Between Pad J1-1(132.08mm,125.73mm) on Multi-Layer And Pad
Un-Routed Net Constraint: Net +3.3V Between Pad U3-8(126.15mm,117.845mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SDA Between Pad U3-5(126.15mm,121.655mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SCL Between Pad U3-6(126.15mm,120.385mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad Q1-3(120.77mm,124.46mm) on Top Layer And Pad J1-5(127mm,125.73mm
Un-Routed Net Constraint: Net NetQ1_1 Between Pad R6-1(118.56mm,123.19mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad R4-2(121.775mm,118.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad R7-1(118.585mm,124.46mm) on Top Layer And Pac
Un-Routed Net Constraint: Net GND Between Pad R1-1(121.75mm,105.7mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad R1-2(121.75mm,104.8mm) on Top Layer And Pac
Un-Routed Net Constraint: Net VFB Between Pad R6-2(117.66mm,123.19mm) on Top Layer And Pad R2-1(119mm,121.5mm
Un-Routed Net Constraint: Net VFB Between Pad U2-1(117.8mm,117.225mm) on Top Layer And Pad R2-1(119mm,121.5mm
Un-Routed Net Constraint: Net SENSE- Between Pad R2-2(118.05mm,121.5mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad U2-3(119.7mm,117.225mm) on Top Layer And Pac
Un-Routed Net Constraint: Net NetC3_1 Between Pad R3-2(121.775mm,117.25mm) on Top Layer And Pac
Un-Routed Net Constraint: Net 9V Between Pad U2-5(117.8mm,119.775mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SENSE+ Between Pad R7-2(117.635mm,124.46mm) on Top Layer And Pac
Un-Routed Net Constraint: Net SCL Between Pad U1-5(122.17mm,113.35mm) on Top Layer [Unplated] And Pac
Un-Routed Net Constraint: Net SDA Between Pad U1-6(122.17mm,112.45mm) on Top Layer [Unplated] And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(124.46mm,118.11mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C1-1(124.46mm,118.11mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.254mm) Between Pad C1-2(124.46mm,117.13mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C2-1(121.76mm,119.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(118.6mm,125.73mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(133.35mm,121.14mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(121.75mm,105.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R2-1(119mm,121.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.154mm < 0.254mm) Between Pad R3-1(122.725mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.154mm < 0.254mm) Between Pad R3-2(121.775mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-2(121.775mm,117.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R4-1(122.725mm,118.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R5-1(121.775mm,120.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R6-1(118.56mm,123.19mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad R7-1(118.585mm,124.46mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-2(124.33mm,111.55mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-3(124.33mm,112.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-6(122.17mm,112.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U1-7(122.17mm,111.55mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-1(117.8mm,117.225mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad U2-2(118.75mm,117.225mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad J1-4(129.54mm,123.19mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad J1-4(129.54mm,123.19mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad J1-6(127mm,123.19mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad J1-6(127mm,123.19mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-1(124.33mm,110.65mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-2(124.33mm,111.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-3(124.33mm,112.45mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-4(124.33mm,113.35mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-4(124.33mm,113.35mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-5(122.17mm,113.35mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-6(122.17mm,112.45mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-7(122.17mm,111.55mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-8(122.17mm,110.65mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-8(122.17mm,110.65mm) on Top Layer And

Electrical Rules Check Report

Class	Document	Message
Error	Sheet1.SchDoc	Net NetU3_1 contains floating input pins (Pin U3-1)
Error	Sheet1.SchDoc	Net NetU3_2 contains floating input pins (Pin U3-2)
Error	Sheet1.SchDoc	Net NetU3_3 contains floating input pins (Pin U3-3)
Error	Sheet1.SchDoc	Net NetU3_7 contains floating input pins (Pin U3-7)
Warning	Sheet1.SchDoc	Net NetU3_1 has no driving source (Pin U3-1)
Warning	Sheet1.SchDoc	Net NetU3_2 has no driving source (Pin U3-2)
Warning	Sheet1.SchDoc	Net NetU3_3 has no driving source (Pin U3-3)
Warning	Sheet1.SchDoc	Net NetU3_7 has no driving source (Pin U3-7)
Warning	Sheet1.SchDoc	Net SCL has no driving source (Pin J1-4, Pin U1-5, Pin U3-6)
Warning	Sheet1.SchDoc	Net SENSE+ has no driving source (Pin R1-2, Pin R3-1, Pin R7-2, Pin U2-3)
Warning	Sheet1.SchDoc	Net SENSE- has no driving source (Pin C2-2, Pin C3-2, Pin R2-2, Pin R4-1, Pin R5-2, Pin U2-4)
Warning	Sheet1.SchDoc	Unconnected Pin U3-1 at 2400mil,2600mil
Warning	Sheet1.SchDoc	Unconnected Pin U3-2 at 2400mil,2500mil
Warning	Sheet1.SchDoc	Unconnected Pin U3-3 at 2400mil,2400mil
Warning	Sheet1.SchDoc	Unconnected Pin U3-7 at 3400mil,2600mil


Connector TBD
17.50
Amplifier and EEPROM
outside tube (dry)
23.00
11.00
22.00
Tube cutaway
Pressure sensor and
thermistor inside tube
(wet)
Thermistor stick should be
thin to reduce thermal mass