Optimizing Low-Density Parity-Check (LDPC) Codes for High-Frequency Trading (HFT) Data Transmission

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***Abstract*—In the domain of High-Frequency Trading (HFT), where microsecond-level latency dictates profitability, data integrity is paramount. Even marginal transmission errors can precipitate substantial financial losses. This research explores the potential of Low-Density Parity-Check (LDPC) codes, recognized for their near-Shannon-limit error correction capabilities and demonstrated efficacy in high-throughput systems like 5G NR and optical networks, as a novel solution for enhancing HFT data reliability. Although direct applications within HFT are limited, we posit that strategically tailored LDPC code designs, incorporating quasi-cyclic structures and matrix splitting, can achieve the requisite balance between robust error correction and minimal latency overhead. We propose a methodological framework for adapting LDPC codes to the unique demands of HFT communication, emphasizing hardware acceleration via Field-Programmable Gate Arrays (FPGAs) to achieve sub-microsecond processing. This study seeks to bridge knowledge gap between advanced error correction methodologies and the specific challenges of financial data transmission, thereby laying the groundwork for future investigations into latency-optimized coding strategies within HFT environments.**

***Index Terms*—High-Frequency Trading (HFT), Low-Density Parity-Check (LDPC) Codes, Error Correction Codes, Field-Programmable Gate Arrays (FPGAs), Quasi-Cyclic LDPC Codes, Matrix Splitting, Financial Markets, Bit Error Rate (BER)**

I. Introduction

High-Frequency Trading (HFT) has transformed financial markets by leveraging ultra-low-latency systems to execute trades in microseconds or nanoseconds, capitalizing on fleeting price discrepancies. In 2025, HFT accounts for over 70% of U.S. equity trading volume, with latency reductions from milliseconds to microseconds driving competitive advantage [1]. This speed comes at a cost: data transmission errors—whether from noise in microwave links or packet loss in fiber-optic networks—can disrupt trade execution, leading to losses in the millions within moments.

Low-Density Parity-Check (LDPC) codes, first proposed by Gallager in 1962 [2], offer a compelling solution. These linear error-correcting codes, defined by sparse parity-check matrices, achieve near-Shannon-limit performance with efficient iterative decoding. Widely adopted in high-speed communication standards like 5G NR, Wi-Fi 802.11ax, and DVB-S2, LDPC codes deliver high throughput and reliability, making them a candidate for latency-sensitive applications. Recent advancements, such as quasi-cyclic designs and FPGA-based implementations, have reduced encoding times to nanoseconds [3], suggesting potential for HFT's stringent demands.

Despite their success in telecommunications, LDPC codes remain underexplored in HFT data transmission. Existing HFT literature focuses on infrastructure—low-latency switches, co-location, and multicast protocols [4][5][6]—with little attention to advanced error correction at the application level. This gap raises a critical question: can LDPC codes be optimized to enhance HFT reliability without sacrificing speed? Current systems likely rely on basic error detection or protocol-level recovery (e.g., TCP), which may suffice for occasional errors but falter under high noise or burst losses.

This paper investigates the feasibility of optimizing LDPC codes for HFT data transmission. Our objective is to propose a framework that balances error correction with minimal latency, leveraging hardware acceleration via Field-Programmable Gate Arrays (FPGAs). By adapting LDPC designs from high-speed domains, we aim to bridge the gap between communication theory and financial systems. Section II provides background on LDPC and HFT requirements, Section III details the proposed framework, Section IV evaluates its performance, and Section V concludes with future directions.

II. Background

Financial data transmission typically benefits from a relatively high Signal-to-Noise Ratio (SNR). The infrastructure supporting HFT, including dedicated fiber-optic networks and microwave links, is engineered for high fidelity and experiences significantly less ambient noise compared to wireless channels or public internet infrastructure.

This high-SNR characteristic has a significant implication for the choice of error correction techniques. While powerful codes capable of operating at very low SNR are essential for applications like deep-space communication or cellular networks, HFT's primary concern shifts towards achieving extremely low Bit Error Rates (BER) under these comparatively benign, yet still critical, conditions. Low-Density Parity-Check

(LDPC) codes are particularly well-suited for this regime. Their ability to achieve near-Shannon-limit performance [7], coupled with their flexible design parameters, allows for optimization towards achieving very low error floors even at moderate to high SNR values. This makes them a promising candidate for ensuring the stringent reliability demands of HFT without incurring excessive latency penalties associated with more complex error correction schemes designed for noisy channels.

Furthermore, the stringent latency requirements of HFT necessitate hardware-based implementations for any error correction mechanism. Software-based error correction introduces unacceptable delays due to processing overhead. Field-Programmable Gate Arrays (FPGAs) emerge as the ideal platform for implementing LDPC encoders and decoders in this context. FPGAs offer several key advantages:

- Parallel Processing: The inherent parallel architecture of FPGAs allows for the simultaneous execution of the numerous computations involved in LDPC encoding and, crucially, the iterative decoding process.
- Hardware Configurability: FPGAs provide the flexibility to implement custom hardware architectures tailored to the specific parameters of the chosen LDPC code. This allows for fine-grained optimization of the encoding and decoding algorithms.
- High Throughput: The combination of parallel processing and custom hardware design enables FPGAs to achieve significantly higher data processing rates compared to general-purpose processors, making them capable of handling the high-volume, high-velocity data streams characteristic of HFT.

The iterative nature of LDPC decoding, while contributing to their powerful error correction capabilities, can be computationally intensive. However, the parallel processing capabilities of FPGAs are particularly well-suited for efficiently implementing these iterative algorithms. By mapping the constituent check nodes and variable nodes of the LDPC code's Tanner graph onto the FPGA fabric and implementing the message-passing algorithm in parallel, significant reductions in decoding latency can be achieved.

The inherent suitability of LDPC codes for achieving low BER at moderate to high SNR, combined with the parallel processing and hardware configurability offered by FPGAs for high-throughput and low-latency implementations, forms a strong foundation for investigating their potential in the domain of financial markets.

III. Methods

Two approaches are investigated for tailoring Low-Density Parity-Check (LDPC) codes for efficient and low-latency implementation on Field-Programmable Gate Arrays (FPGAs): the utilization of Quasi-Cyclic (QC) LDPC codes and the application of parity-check matrix splitting techniques.

A. Quasi Cyclic (QC) LDPC Code

QC LDPC codes are characterized by a parity-check matrix ($\mathbf{H}$) composed of blocks of circulant permutation matrices or zero matrices. This specific structure presents notable advantages for hardware realization, particularly on FPGA platforms, as the circulant nature of the sub-matrices enables simplified encoding and decoding architectures with shift registers.

To further capitalize on the QC LDPC architecture, we will adopt and modify a matrix design from prior work [8]. The general QC LDPC of rate $R = (L-1)/L$ has the following structure:

$$G = \begin{bmatrix} P_2^T & \cdots & I_m & 0 & \cdots & 0 \\ P_3^T & \cdots & 0 & I_m & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ P_L^T & \cdots & 0 & 0 & \cdots & I_m \end{bmatrix}$$

The proposed change is that the general Quasi-Cyclic Generator matrix of rate $R = \frac{1}{2}$ has the structure:

$$G = \begin{bmatrix} 0 & \cdots & 0 & P_2^T & I_m & 0 & \cdots & 0 \\ 0 & \cdots & P_3^T & 0 & 0 & I_m & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ P_L^T & \cdots & 0 & 0 & 0 & 0 & \cdots & I_m \end{bmatrix}$$

As one of the requirements is $GH^T = 0$, we can re-write it as

$$\begin{bmatrix} 0 & \cdots & 0 & P_2^T & I_m & 0 & \cdots & 0 \\ 0 & \cdots & P_3^T & 0 & 0 & I_m & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ P_L^T & \cdots & 0 & 0 & 0 & 0 & \cdots & I_m \end{bmatrix} \begin{bmatrix} H_{L-1}^T \\ \vdots \\ H_2^T \\ H_1^T \\ H_2^T \\ \vdots \\ H_L^T \end{bmatrix} = 0$$

From the above, we can get several relations

$$P_2^T H_1^T = H_2^T$$
$$P_3^T H_2^T = H_3^T$$
$$\vdots$$
$$P_L^T H_{L-1}^T = H_L^T$$

When tested with the parameters below:

Simulation tool used	Matlab
Codeword Size	200-2000 bit
Code rate	½, ¼, 1/10
Iterations	10
Modulation	BPSK
Channel Model	AWGN
Maximum number of iterations	10
Number of rows in H matrix for Fig. 2 and Fig. 3	50
Number of rows in H matrix for Fig. 2 and Fig. 3	200
Number of 1's in each row per sub matrix	2
L for Fig. 2 and Fig. 3	3

Fig. 1. QC LDPC Test Parameters [8]

This construction yields a performance gain of approximately 1 dB at a Bit Error Rate (BER) of 10^{-4} in the higher Signal-to-Noise Ratio (SNR) regime relevant to our application.

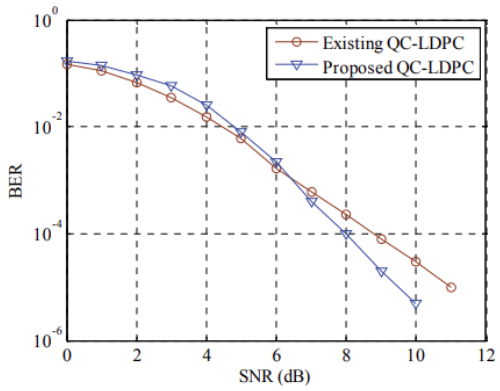

Fig. 2. Comparison between proposed and existing schemes using sum product decoding. [8]

B. Matrix Splitting

In addition to employing QC LDPC codes, the research proposes methods of splitting the parity-check matrix (H) to further optimize the encoding and decoding processes for FPGA implementation. Matrix splitting involves decomposing the large parity-check matrix into smaller, more manageable sub-matrices, which can facilitate parallel processing during both encoding and the iterative decoding process, potentially reducing the overall latency. Various matrix splitting techniques have been analyzed to determine their suitability for HFT's low-latency requirements and the architectural constraints of FPGAs. The evaluation of trade-offs between the complexity of the splitting scheme, the achievable degree of parallelism, and the resulting impact on error correction performance has led to the decision to implement Q/R-RAM splitting, as detailed in prior work [9].

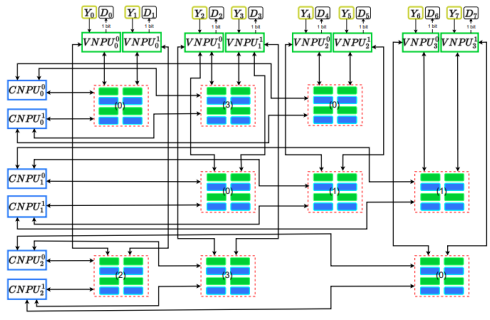

Fig. 3. Proposed Architecture [9]

The suggested method is to split the base matrix into s^2 small matrices, allowing the original serial schedule inner blocks and parallel process inter blocks in the decoder architecture to be retained. After splitting, the size of each block becomes Z/s, where Z is the cyclically shifted address values when Check Node Processing Units and Variable Node Processing Units read and write addresses. For a detailed walk-through of its mathematics, [9] can be reviewed.

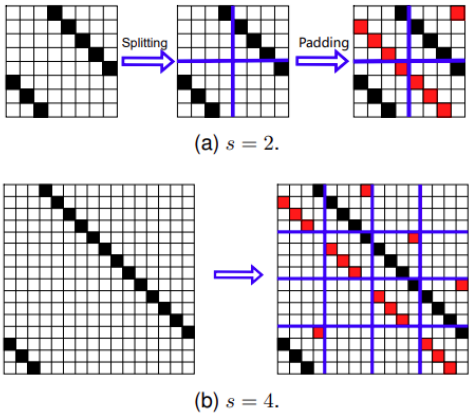

Fig. 4. The process of block splitting and padding for base matrix [9]

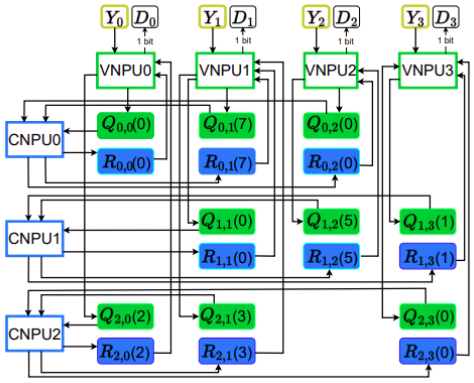

Fig. 5. Proposed Decoder Structure [9]

This implementation is expected to achieve a throughput of 6.072 Gbps at a clock frequency of 253 MHz. Furthermore, while the throughput of the Splitting Decoder is projected to be 12 times that of a Serial Processing Parity (SPP) Decoder, the overall resource utilization is only 3-4 times the original.

	LUTs	FF	F7 Muxes	Block RAM	η(Gbps)	$\tau(\mu s)$
SPP Decoder	41k	44k	246	351	0.506	16.7
Splitting Decoder (s=4)	61k	64k	538	549	2.024	4.2
Splitting Decoder (s=12)	131k	142k	726	1211	6.072	1.4
PipeShift Decoder	194k	252k	24k	0	2.65	2.7

Fig. 6. The comparison of Resource Occupancy for Different Decoders [9]

Therefore, the throughput and latency improvements achieved through the Q/R-RAM matrix splitting technique are anticipated to be significantly advantageous overall.

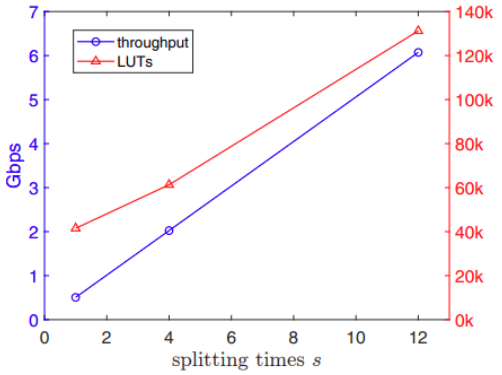

Fig. 7. The relationship between throughput and the number of LUTs with respect to the splitting [9].

IV. Experiment

To evaluate the feasibility and performance of the proposed LDPC-based framework for HFT data transmission, we will adapt an existing MATLAB simulation environment [10] originally designed for the DVB-S.2 standard. This simulation platform provides a comprehensive framework that includes channel coding and modulation schemes. Specifically, the DVB-S.2 simulation incorporates a Bose-Chaudhuri-Hocquenghem (BCH) outer encoder, which, as a type of cyclic code, shares structural similarities with the QC LDPC codes we intend to implement. Furthermore, the simulation includes buffering mechanisms to redistribute the input data across columns, effectively altering the frame size – a feature that allows us to model and analyze the impact of different LDPC code parameters and matrix splitting configurations. The characteristics of the communication channel within the simulation will be initially configured with arbitrary parameters, as the primary focus of this research is on the performance of the LDPC coding and decoding stages, particularly in the context of high SNR environments typical of HFT infrastructure.

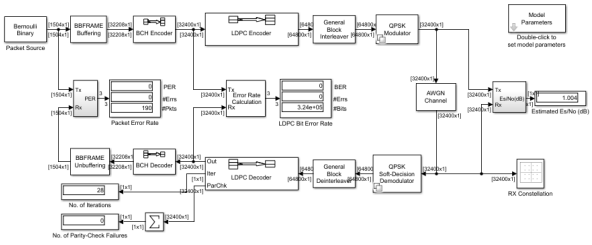

Fig. 8. Referenced [10] and Modified Simulink Model

A. Performance

The inherent error correction capability of LDPC codes can be readily demonstrated using the default simulation settings. By configuring the system with Quadrature Phase-Shift Keying (QPSK) modulation, a code rate of 1/2, an energy per symbol to noise power spectral density ratio E_s/N_o of 1 dB, and a maximum of 50 iterations for the LDPC decoder, we can observe the robust performance even under relatively noisy conditions. The resulting scatter plot visually illustrates the level of noise in the simulated channel. As expected with well-designed LDPC codes, the decoder exhibit a low scatter which equates to low error rate under these parameters.

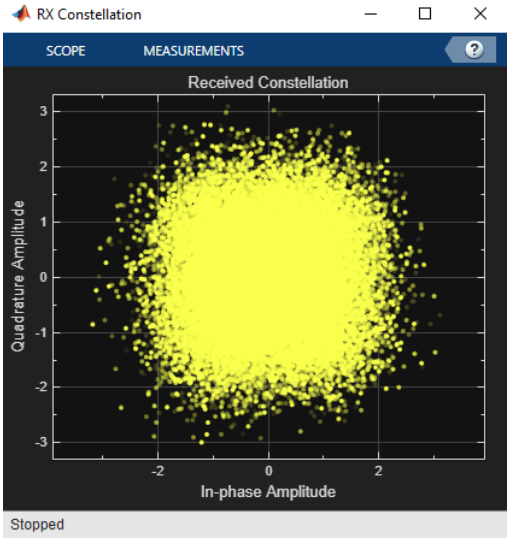

Fig. 9. Simulation Constellation Scatter Plot

To further analyze the performance characteristics, we systematically vary the E_s/N_o value. For instance, a slight decrease to 0.5 dB is expected to result in a significant increase in the Bit Error Rate (BER) at the output of the LDPC decoder. This behavior aligns with the characteristic steep performance curves of LDPC codes, where a small change in SNR can lead to a substantial difference in error rates. Conversely, as the SNR is increased, we anticipate a sharp decline in the Frame Error Rate (FER) and BER. This rapid improvement in performance with increasing SNR is particularly relevant to the high-SNR environment of HFT data transmission, suggesting that appropriately designed LDPC codes can achieve the extremely low error rates required for financial applications with minimal overhead.

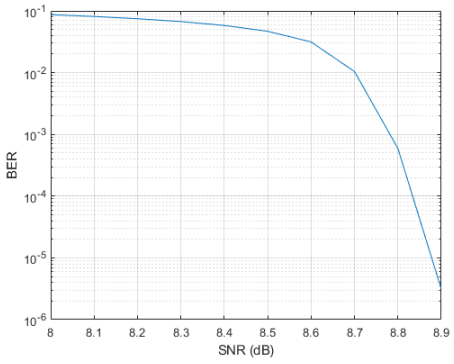

Fig. 10. BER vs SNR for LDPC Code

The graphical representation of the aforementioned charac-

teristic can be seen below where the number of errors increase as the channel has a lower E_s/N_o of 0.1, 0.01 and 0.001:

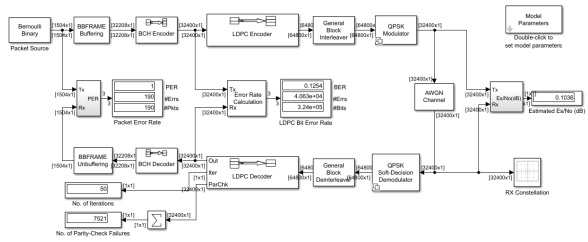

Fig. 11. Model Result in E_s/N_o of 0.1

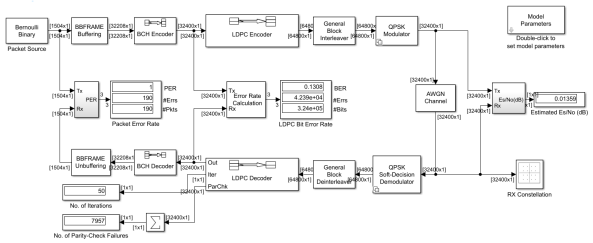

Fig. 12. Model Result in E_s/N_o of 0.01

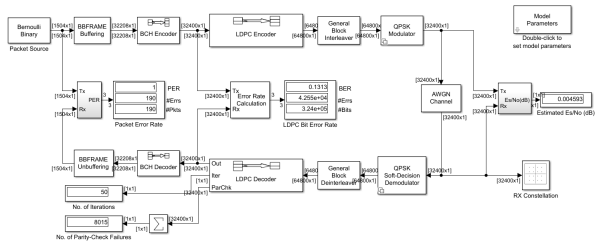

Fig. 13. Model Result in E_s/N_o of 0.001

V. Conclusion

Ensuring reliable data transmission in High-Frequency Trading (HFT)'s ultra-low latency environment is critical. This paper investigated optimizing Low-Density Parity-Check (LDPC) codes, leveraging their strong error correction in the relatively high SNR of HFT to achieve extremely low Bit Error Rates (BER) without prohibitive latency. We focused on Quasi-Cyclic (QC) LDPC codes and parity-check matrix splitting (Q/R-RAM) for efficient FPGA implementation. QC LDPC's structured matrices simplify hardware, while matrix splitting enhances parallelism for lower latency.

Experiments using a DVB-S.2 simulation demonstrated LDPC's strong error correction, showing a rapid BER/FER decrease with increasing SNR, relevant to HFT's high-SNR conditions. This supports the potential of optimized LDPC codes to meet HFT's stringent reliability needs.

This research provides a foundation for enhancing HFT data reliability through FPGA-optimized LDPC codes. Future work will concentrate on detailed FPGA design and performance evaluation within a realistic HFT context.

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