Exploration of the Potential of Quantum Annealing for Hard Scheduling Problems in Air Traffic Management: Report, July 2016

Introduction

Given encouraging of early results in the planning domain[1,2] and the expertise of our team in such sector, aim of the project is to use Quantum Annealing (QA), and in particular the state-of-art D-Wave 2X™ quantum annealer hosted at NASA Ames, as a metaheuristic for solving computational challenging problems in the context of Air Traffic Management (ATM). More precisely, the project has been focused on the problem to find distinct minimum-cost configuration scheduling advisories (CSAs). CSAs consist in the identification of optimal deviations from wind-optimal trajectories to avoid/resolve potential conflicts and minimize delays of flights. In this project, we limit our attention to the North Atlantic oceanic airspace (NAT) for which we have optimal-wind trajectories for two consecutive days (July 28th-29th 2012).

Since the D-Wave 2X™ quantum chip can only optimize binary optimization problems on a specific and fix-by-design architecture called Chimera, in the first part of the project we mainly focused on the formulation of CSAs in terms of discrete variables (Table 1 for tasks/milestones of the project). The discrete model is then expressed in terms of quadratic binary optimization (QUBO) problems that can be natively solved by the D-Wave 2X™ quantum chip. The next set of milestones will include the run of CSA instances on the D-Wave 2X™ quantum chip, as well as the comparison of the results with the best state-of-art classical QUBO optimizers.

Approach

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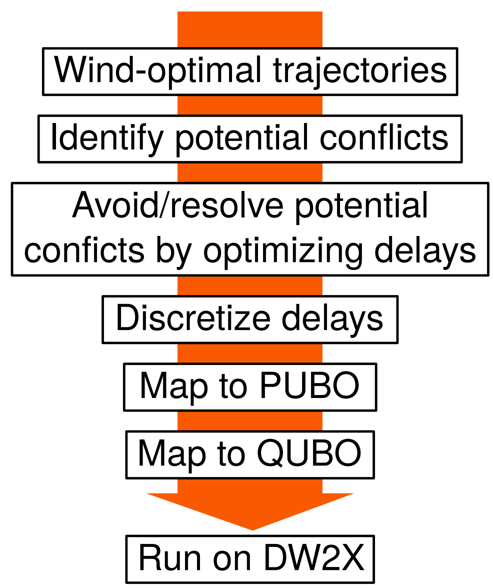

Figure 1: Flow diagram to map ATM problems into the D-Wave 2X™ quantum chip.

Technical details

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[1] Eleanor G Rieffel et al. "A case study in programming a quantum annealer for hard operational planning problems". In: *Quantum Information Processing* 14.1 (2015), pp. 1–36.

[2] Davide Venturelli, Dominic JJ Marchand, and Galo Rojo. "Quantum annealing implementation of job-shop scheduling". In: *arXiv preprint arXiv:1506.08479* (2015).

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Assessment

Task/Milestone	Performance Metric	Expected completion
Map the ATM problem to a suitable polynomial binary optimization problem (PUBO).	Number of required logical qubits. Largest degree of the polynomial. Connectivity of the underlying coupling graph.	✓
Map the ATM problem to a suitable quadratic binary optimization problem (QUBO).	Number of required logical qubits. Connectiviry of the underlying coupling graph.	✓
Identify a set of benchmark ATM problems.	Hardness as a function of size.	1 month
Analyze the results/performance of classical QUBO solvers on ATM problems.	Assess the quality/variety of the solutions after discretization. Find the bottom line for classical computation.	1.5 month
Find an embedding to map the ATM problem onto the Chimera architecture.	Number of physical qubits for each logical qubit. Largest ATM problem embeddable on the current D-Wave 2X™ chip.	2 month
Compile the ATM benchmark ensemble for the D-Wave 2X™ chip.	Scaling of expected time to solution vs. size compared to classical code. Variety of different acceptable solutions.	3 month
Outlook on different architectures and annealing strategies, hardware changes	Potential quantum enhancement.	4 month

Table 1: Breakdown of the project effort into milestones, including suggested performance metric and completion dates (check marks indicate completed tasks).

Conclusion