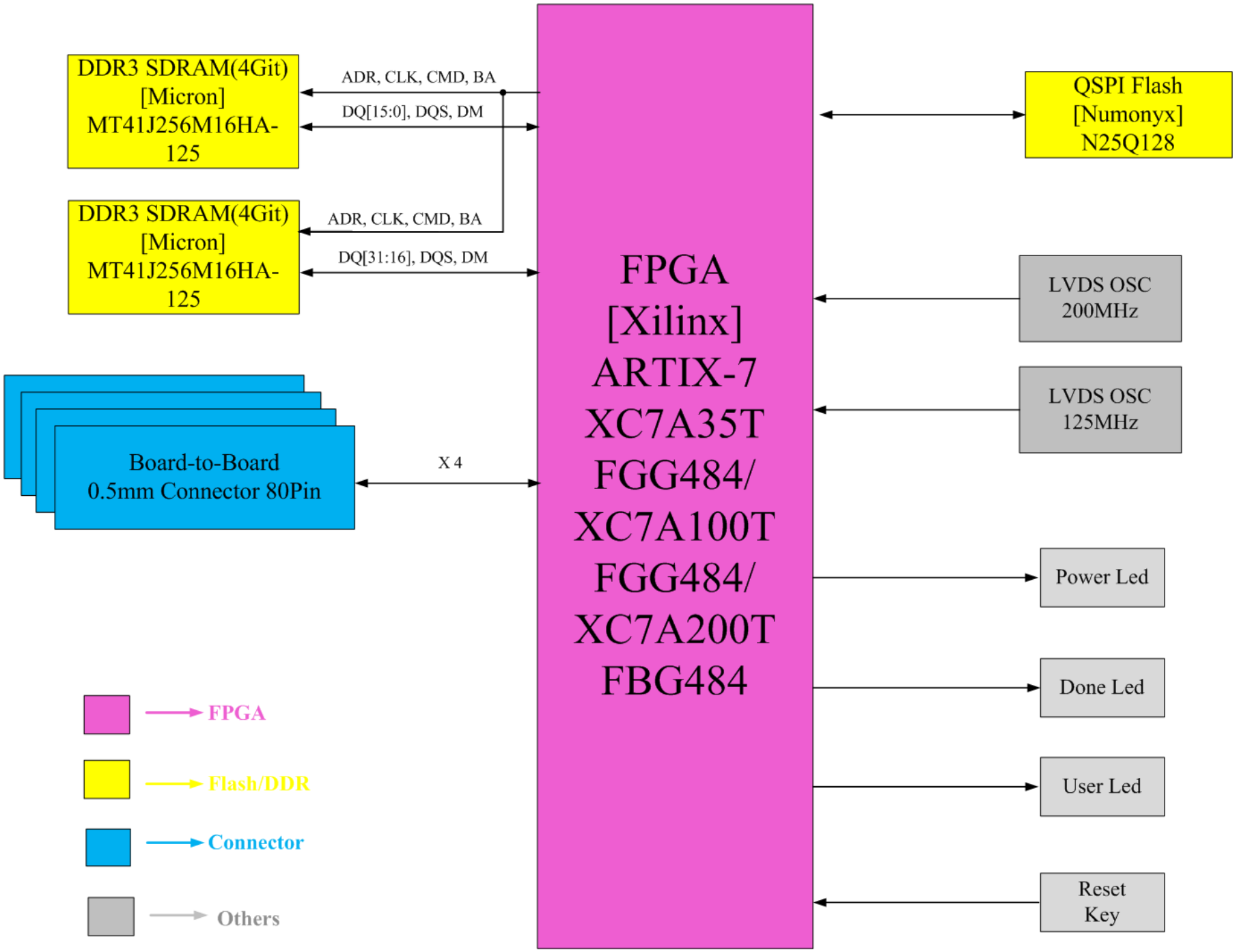

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Title: PAGE01 BLOCK DIAGRAM

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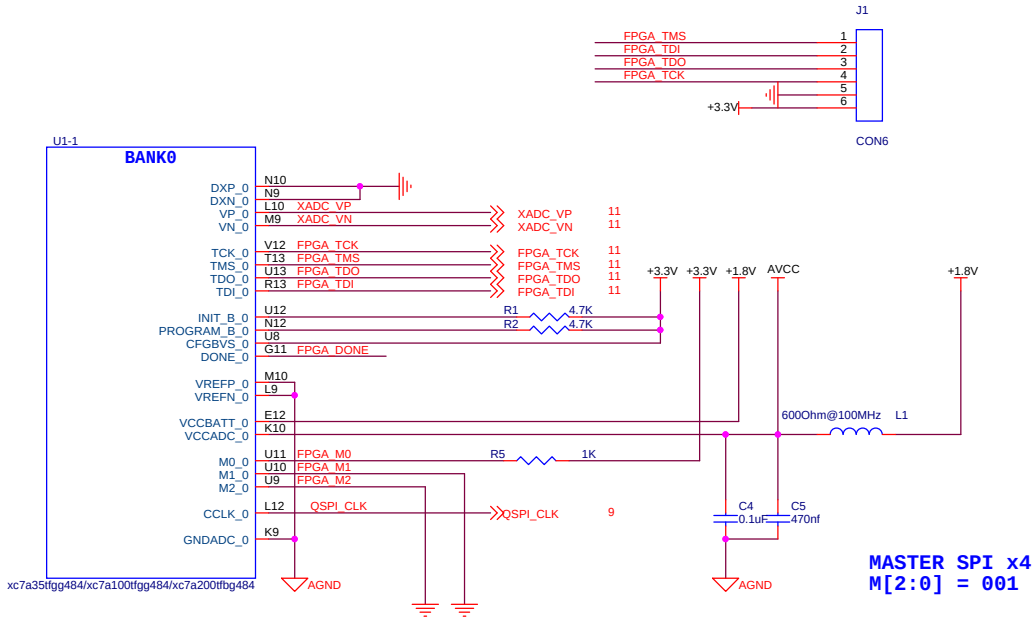

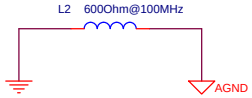

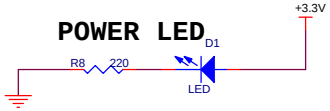

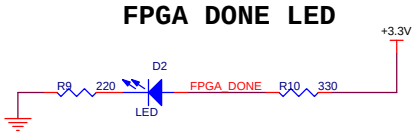

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Title: PAGE02 FPGA BANK0

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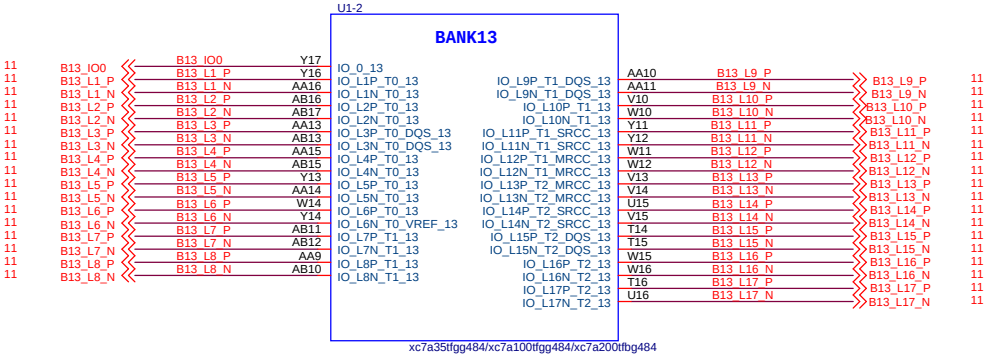
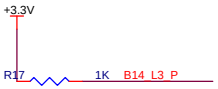
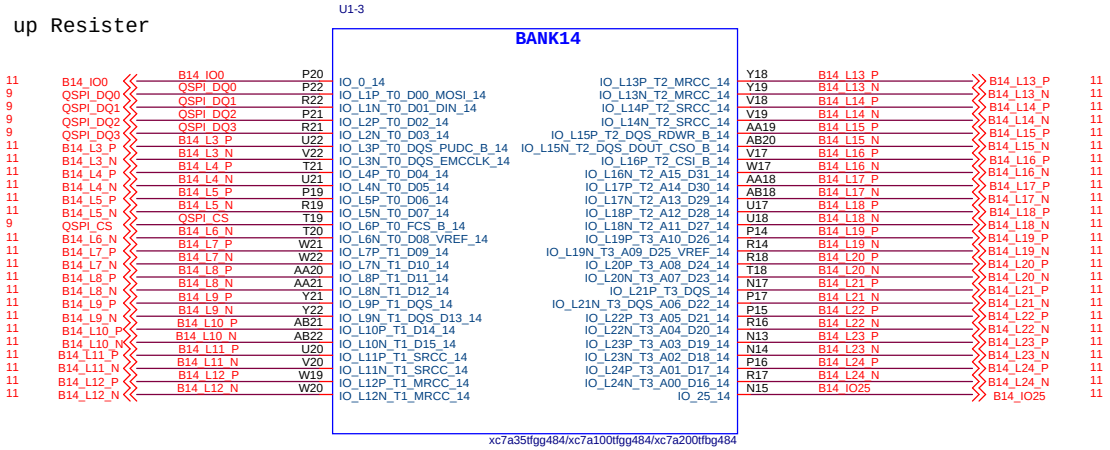
BANK13 is not exist in xc7a35T



PUDC_B=1: Deactive internal Pull up Resister





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Title: PAGE03 FPGA BANK13/14

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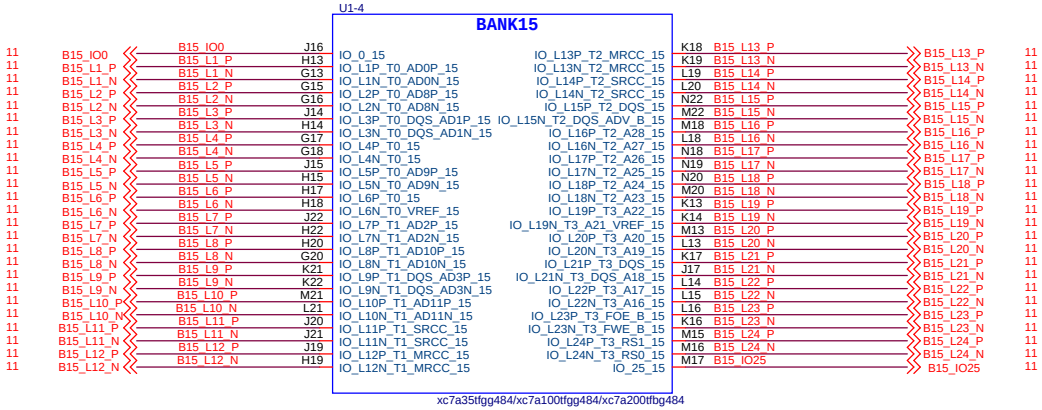

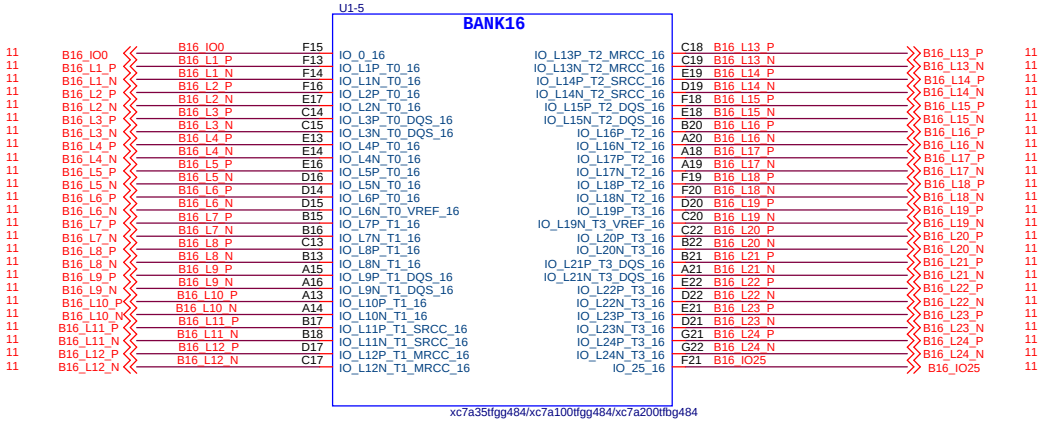

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Title: PAGE04 FPGA BANK15/16

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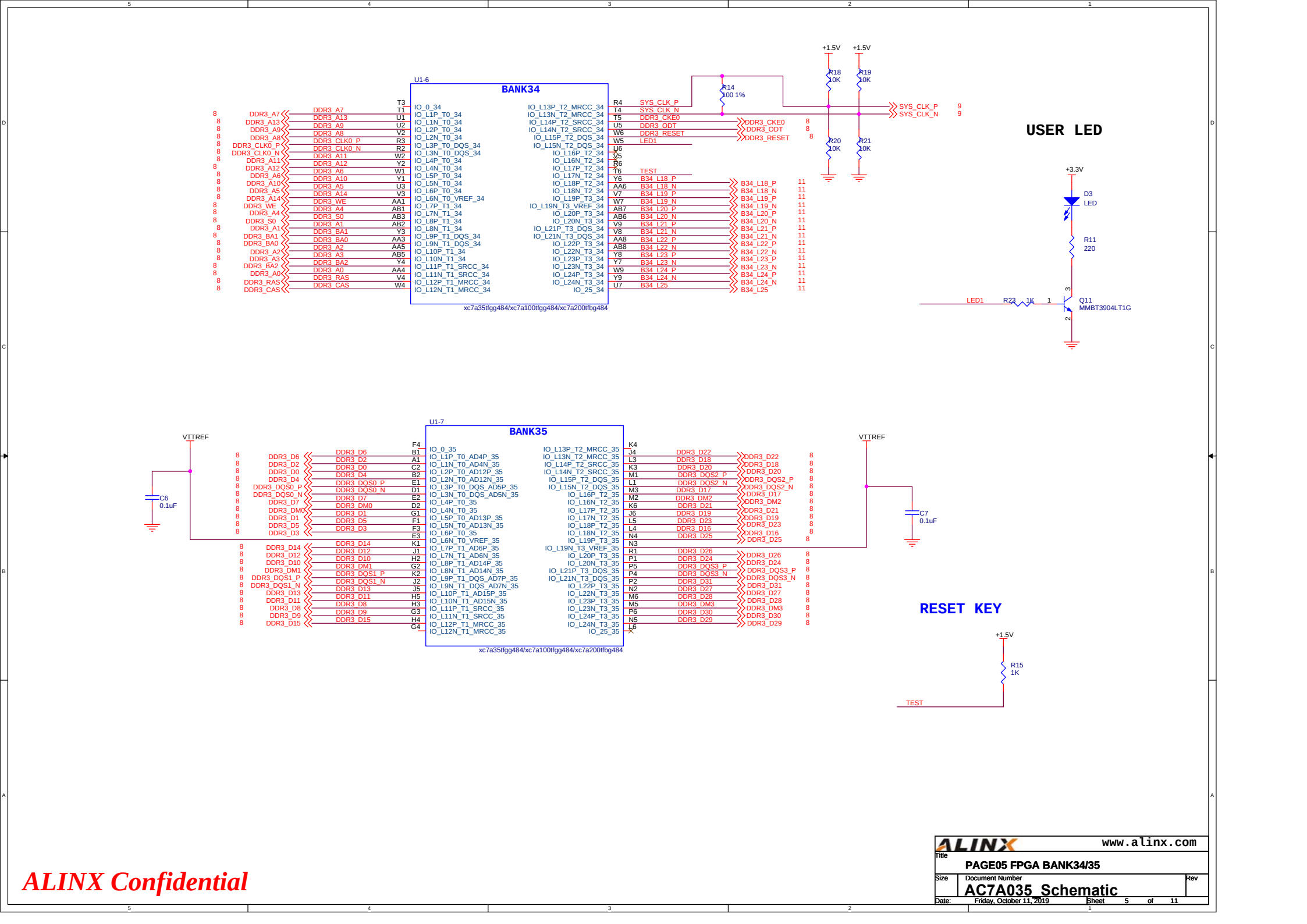

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Title: PAGE05 FPGA BANK34/35		
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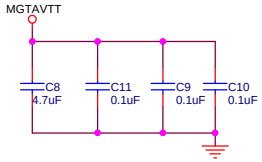
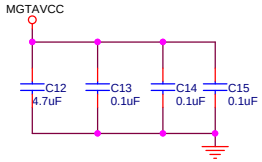
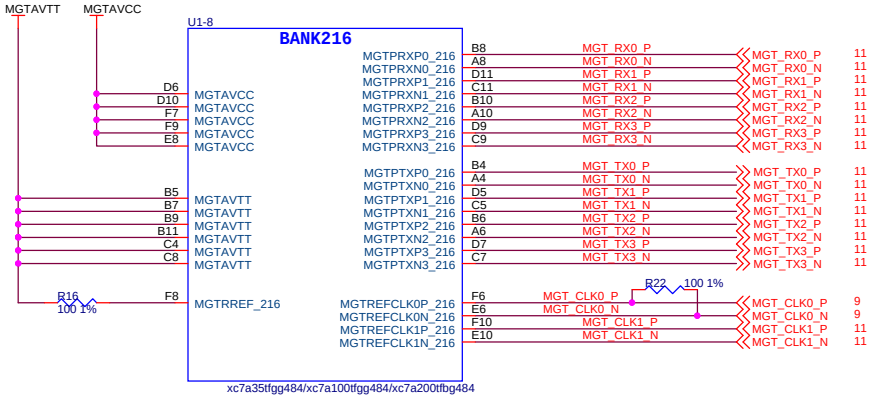
MGTAVTT 4.7uF(1) 0.1uF(2)



MGTAVCC 4.7uF(1) 0.1uF(2)





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Title: PAGE06 FPGA BAN216

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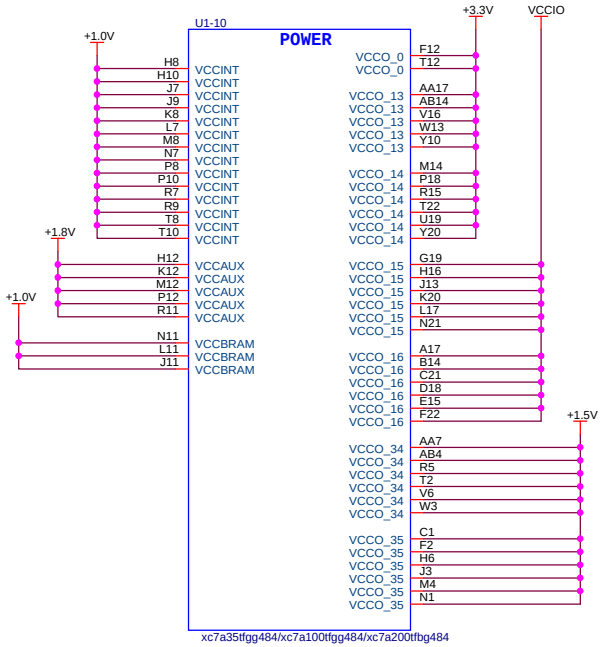

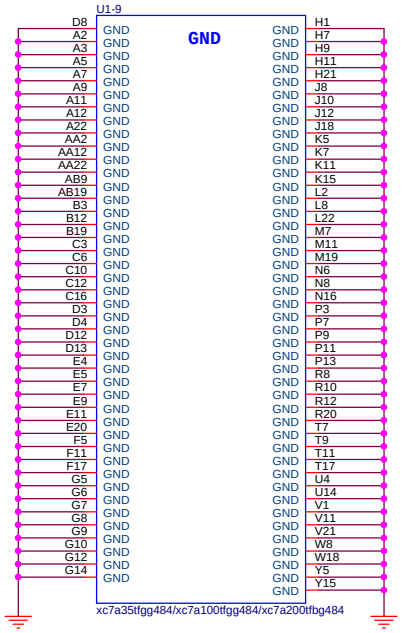

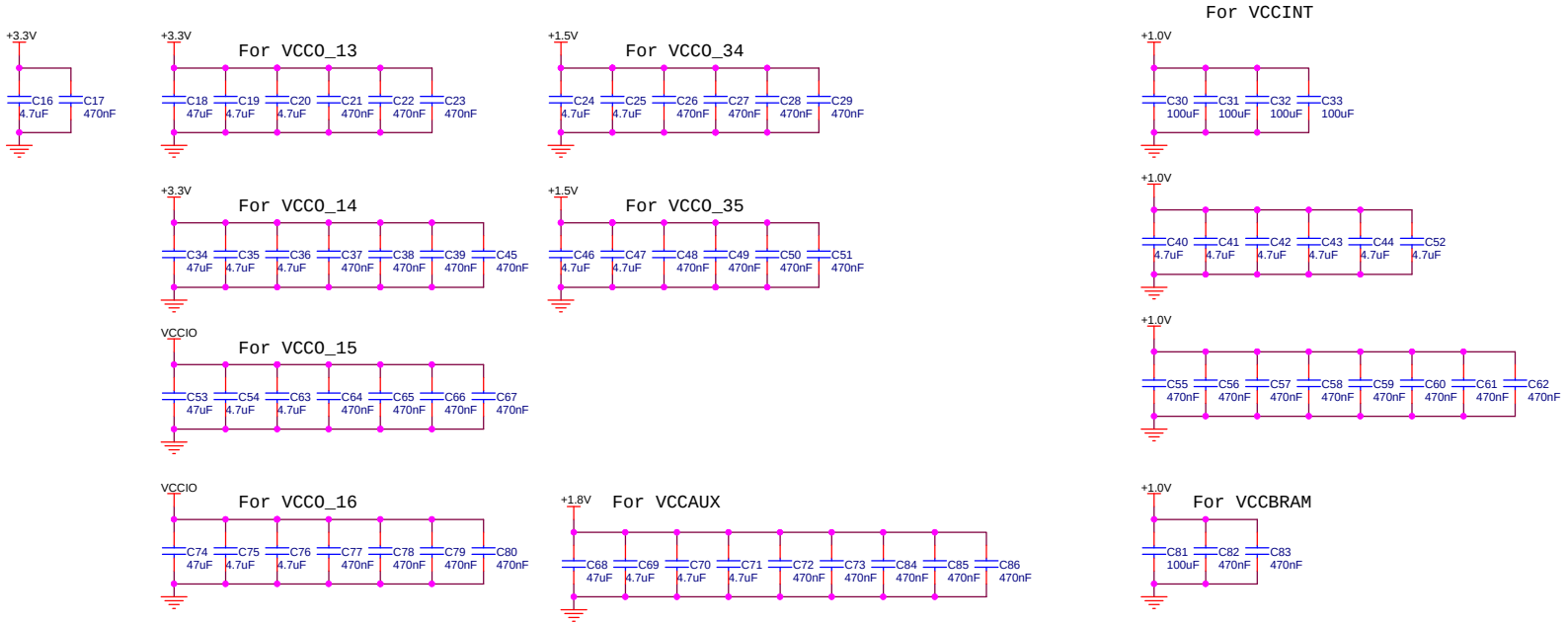

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Title	PAGE07 FPGA Power	
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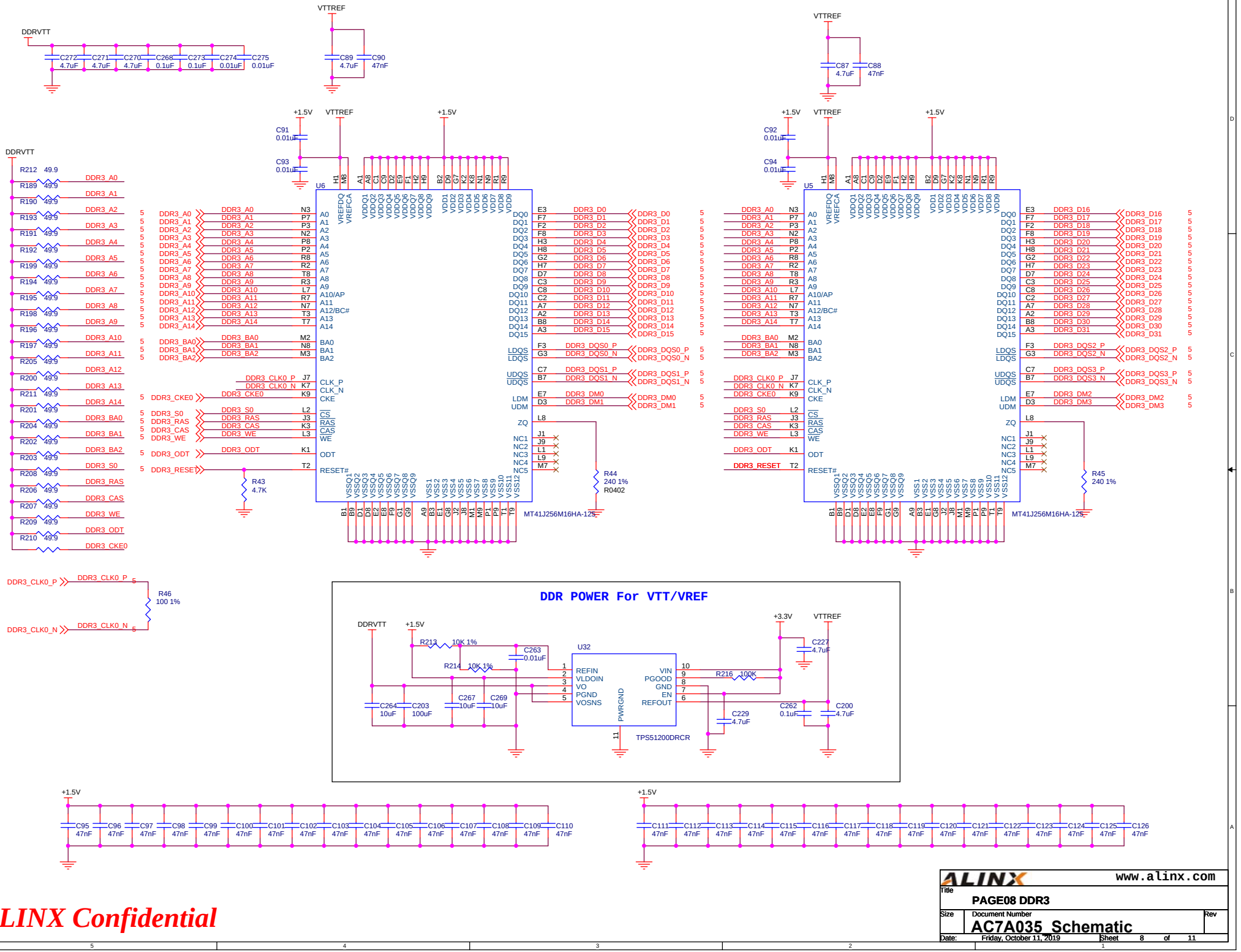
DDRVTT
VTTREF
+1.5V
+3.3V
U6
U5
U32
MT41J256M16HA-125
TPS51200DRCR
DDR POWER For VTT/VREF
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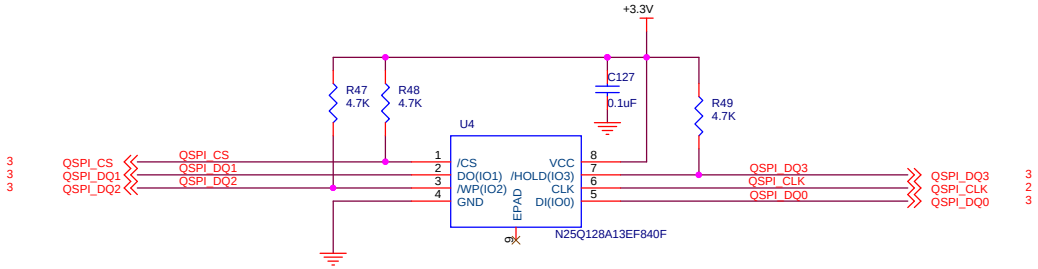
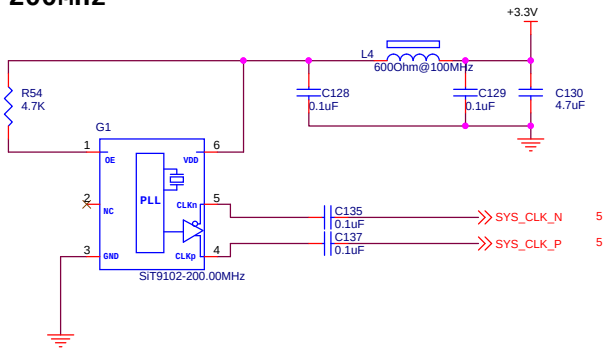
FPGA CONFIG SPI



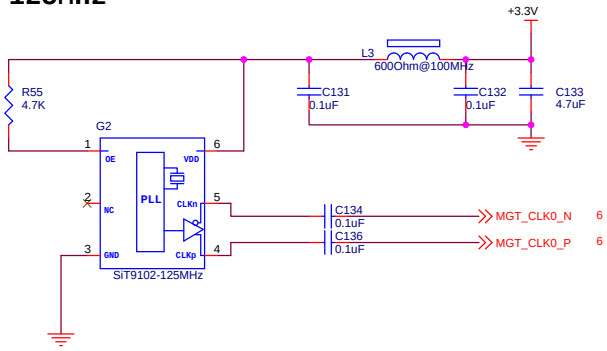
SYSTEM CLOCK

200MHz



GTP CLOCK

125MHz



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Title	PAGE09 CLOCK&FLASH
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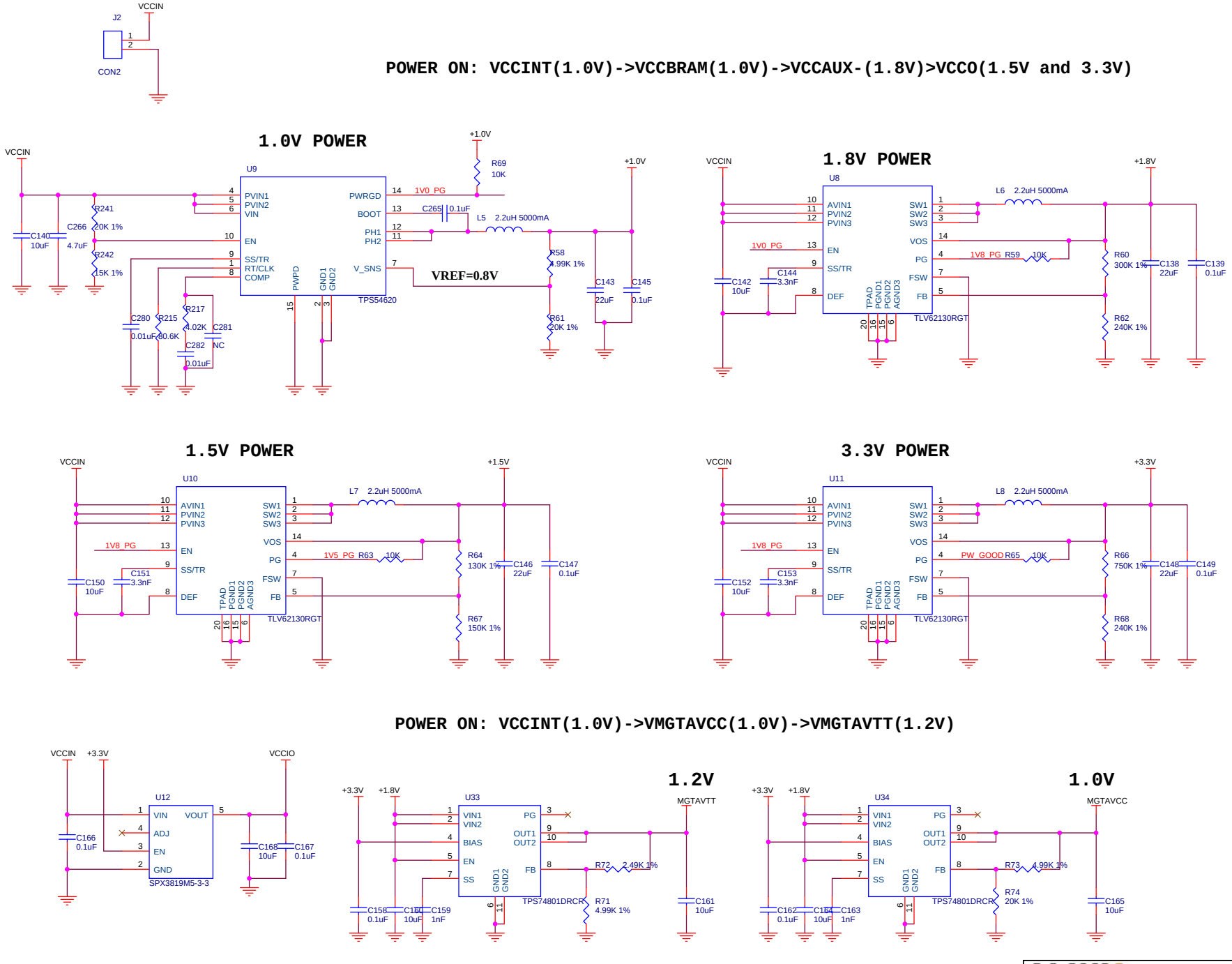
POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)
1.0V POWER
1.8V POWER
1.5V POWER
3.3V POWER
POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)
1.2V
1.0V
VCCIN
VCCIO
+1.0V
+1.8V
+1.5V
+3.3V
VREF=0.8V
TPS54620
TLV62130RGT
TPS74801DRCR
SPX3819M5-3-3
MGTAVTT
MGTAVCC
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PAGE10 POWER
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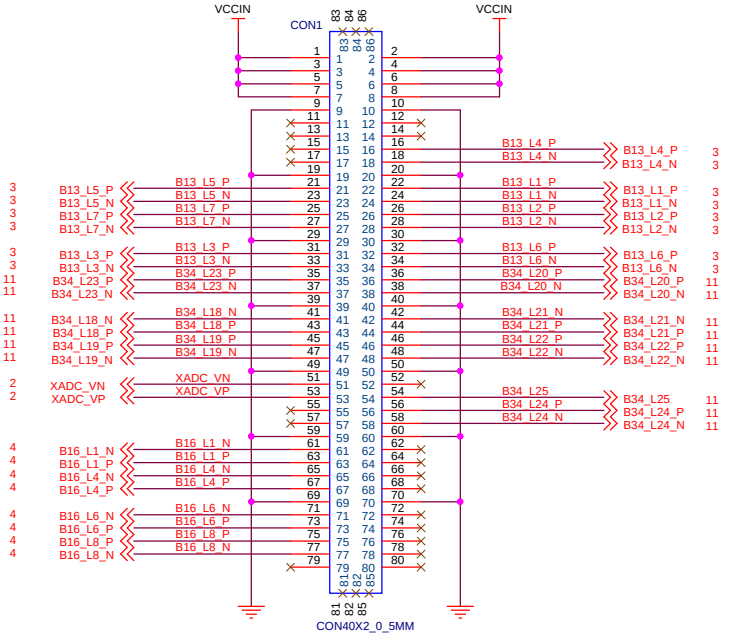
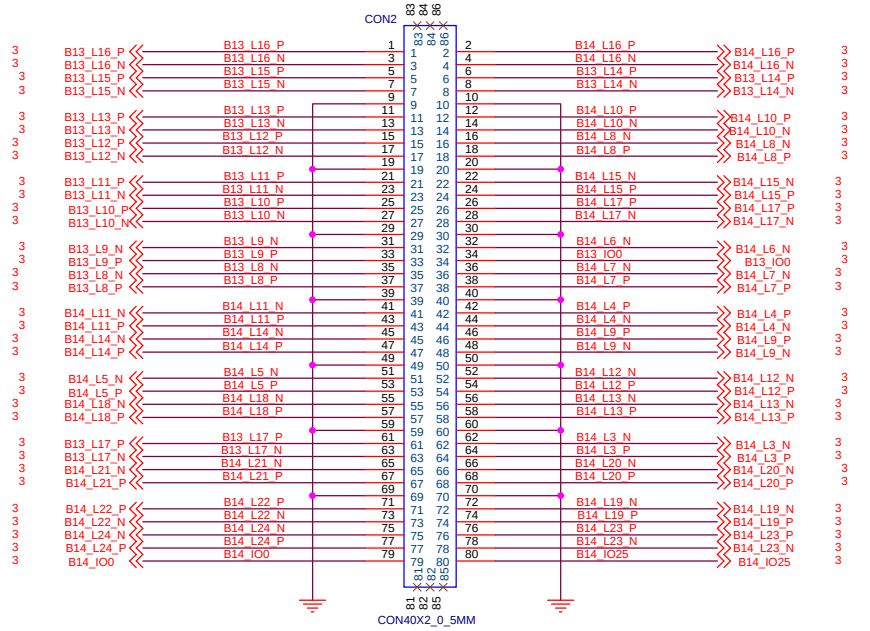
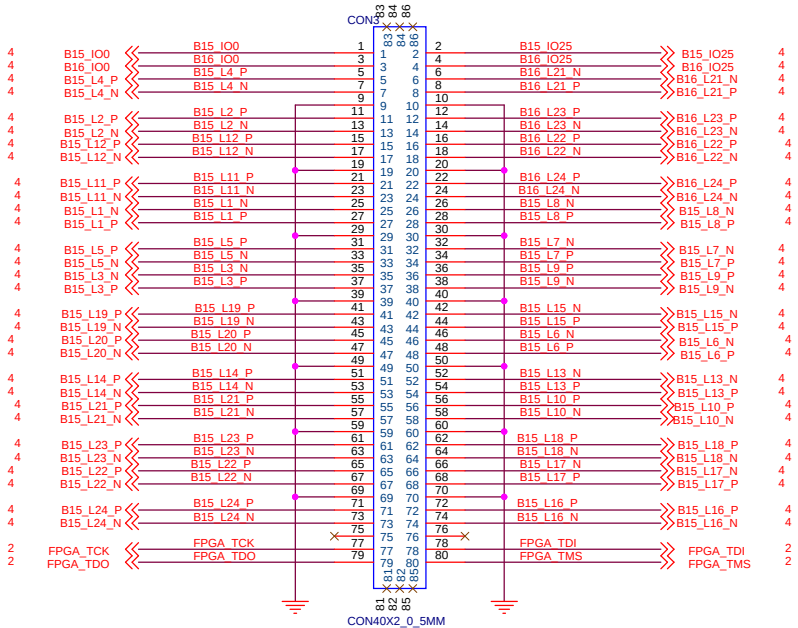
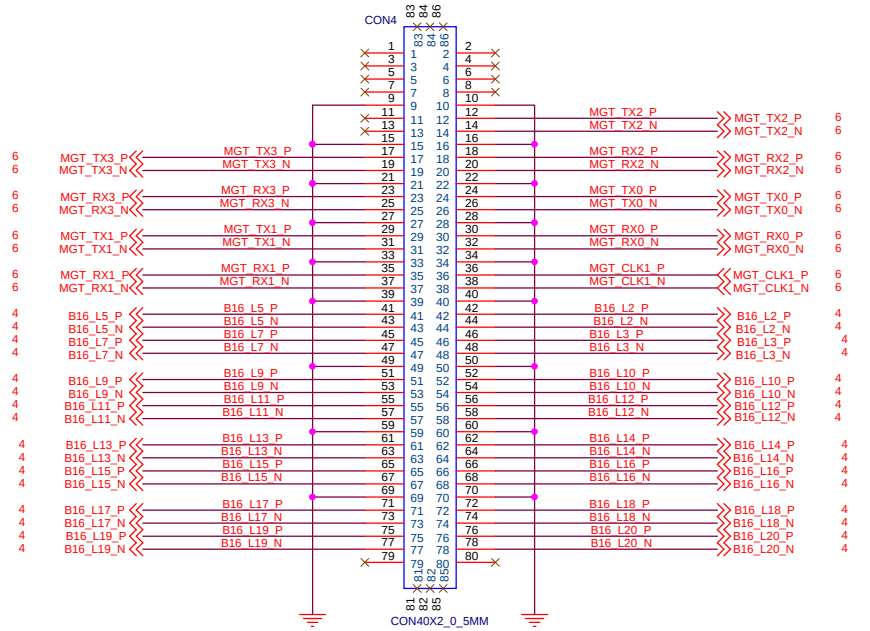
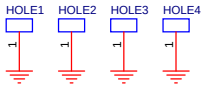
These IOs are on BANK34, Voltage is 1.5V!!!
BANK13 IO is not avaliable for XC7A35T











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Title: PAGE11 Connector

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