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The NA60 silicon tracking telescope for proton running

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Abstract

This note presents the silicon tracking telescope planned to be used in the NA60 experiment during the runs with the proton beam. After very briefly recalling the background context specific of the proton runs, we describe the overall concept of the tracking telescope, in terms of geometry and simulated performance (occupancies, momentum resolution of the charged tracks, dimuon mass resolution, etc). We then describe the microstrip sensor, the readout chip, the hybrid, and all the other components of the readout electronics chain (the service card, the ADC card, etc), including some information from previous experience in lab and beam tests. Finally, we address the issues related to mechanical supports and cooling.

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1 Introduction

The NA60 experiment has been approved to study prompt dimuon and charm production in proton and heavy-ion collisions, at the SPS. The first (commissioning) run will take place from October 20 to November 4 of 2001. In the years 2002 and 2003 it is expected that there will be around 30 days of proton running (at the beginning of the SPS operation) and around 30 days of ion running, with Pb ions in 2002 and with an 'intermediate mass ion' (probably In or Sn) in 2003.

This note is devoted to the silicon tracking telescope to be used in the proton runs. At the time when the NA60 proposal was written, early 2000, it was planned that the proton runs would use the same silicon telescope as the ion runs, completely composed of silicon pixel detectors. However, several factors contributed to a considerable delay in the availability of the corresponding readout chips. By the end of year 2000 it became clear that we would not be able to complete a reasonable number of pixel tracking planes in time for the proton runs of 2001 and 2002. On the other hand, it was clear that the much smaller multiplicities of produced charged particles in a proton induced collision allow for a good tracking telescope made of microstrip detectors, instead of the high granularity pixel detectors necessary to cope with heavy ion collisions. Section 2 explains in more detail the expected performance of a telescope made mostly of strip planes in the environment of proton-nucleus collisions.

After several discussions, it was found that the existing silicon microstrips detectors were not suitable for our application. In particular, the $r-\phi$ detectors developed for the LHC-B vertex detector are not appropriate for use in the dipole magnetic field of the target region of NA60, and would not fit in the small gap of the PT7 magnet. In March 2001, a new microstrip detector, optimized for the NA60 conditions, was designed by some of the authors of this note. The Section 3 describes the sensor design and its main characteristics.

Given the very short time scale for the building of the strip telescope, six months from its first conception to its commissioning on the beam, this project could only work if we were able to find (almost) all the components already available. Fortunately, the SCTA128 chip, described in Section 4, can be used without any change in the NA60 application. Also the hybrid developed for that chip in the framework of the ATLAS experiment, described in Section 5, can be used for NA60, with only two minor changes. The presently existing 'service card' requires some modifications, to minimize its thickness and length, and to place some components away from the (strong) magnetic field. This is explained in Section 6. Previous experience with these chips, hybrids and service cards, obtained in a test setup in the lab and in the ATLAS test beam, is summarized in Section 7.

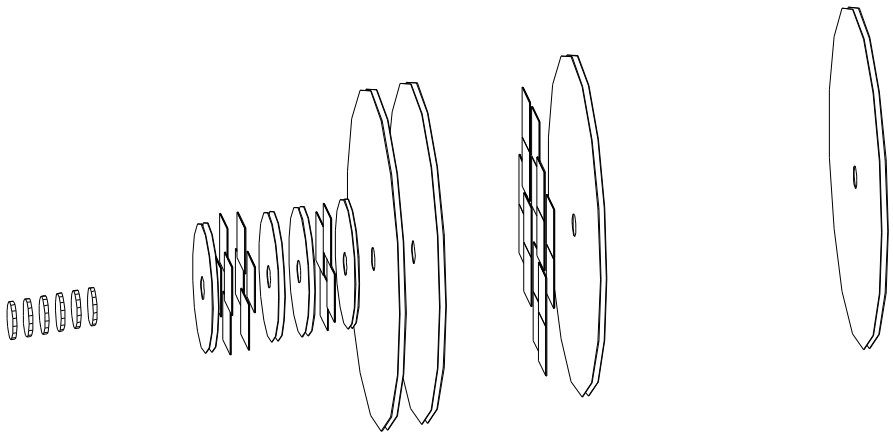
The next step in the readout electronics chain is a card with 8 ADC channels, described in Section 8, that reads the data stream from the service card, at 40 MHz, and sends it to the PCI-FLIC card, placed in the data acquisition PCs. The same PCI-FLIC 'flexible I/O' cards will be used for the readout of all the other detectors of NA60. A detailed description of the FLIC card can be found in Ref. [1].

Once we have the microstrip sensors, the hybrids (with the readout chips) and the service cards, we must assemble them in 'modules', with an appropriate mechanical frame that fits inside the magnet. This is discussed in Section 9, where the cooling issues are also briefly addressed.

We end this note with a rough estimation of the time schedule for the availability of the different components, for the tests of the chips prior to bonding on the hybrids, tests of the complete system, including sensors and the full readout electronics chain, and the assembly of the modules, including mechanical supports and cooling.

2 Performance of the silicon tracking telescope

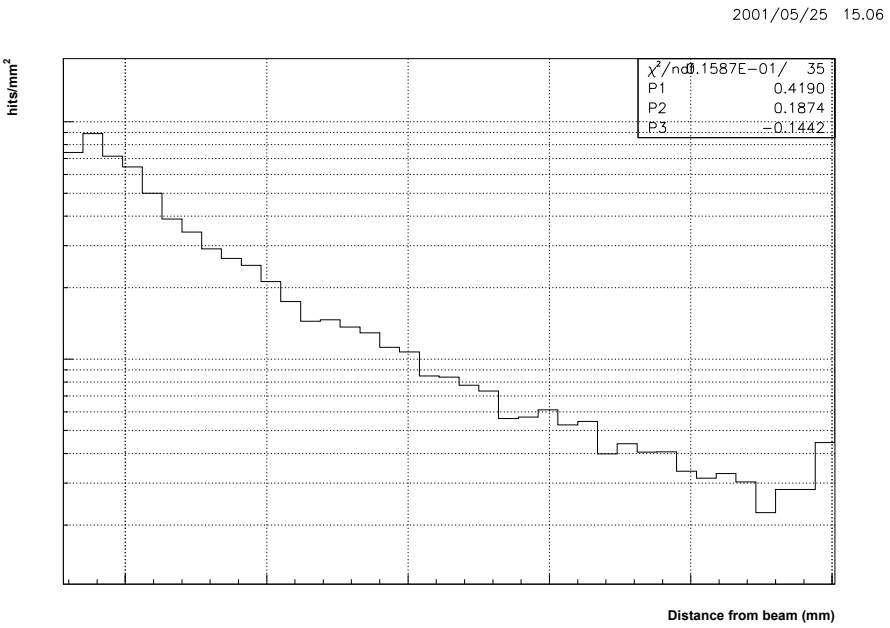
The general layout of the vertex telescope for the p-A runs is shown on Fig. 1. It consists of eight double planes of microstrip detectors, plus a few pixel planes.



	Pitch(μm)	Number
A	80.00	62
B	60.00	60
C	80.00	48
D	134.91	53
E	151.06	226
F	226.96	79

fits inside the inner region of the sensors, for those positioned at less than 14 cm from the target. These planes will be assembled with only four readout chips on each hybrid.

Figure 3 shows the hit density, per mm^2, in the first microstrip plane, as obtained by a full Monte-Carlo simulation (using Venus and Geant) of p-Pb collisions with 450 GeV/c protons. The corresponding densities for the most downstream planes are less than half, mainly because the low momentum secondaries are swept away by the 2.5 T magnetic field of the PT7 magnet.



The strips of each sensor have an inclination angle of $\pm 25^{\circ}$ with respect to the vertical axis, y. This value was found to be optimal according to the following criteria:

- to have similar resolutions in the x and y directions for the offsets ($\sigma(x, y)$) and slopes $\sigma(\phi_x, \phi_y)$;
- to have the best possible curvature (inverse momentum) resolution, $\sigma(C)$.

In fact, the ideal curvature resolution, $\sigma_{\rm ideal}(C)$, is obtained when the strips are oriented in the vertical direction since the dipole field is directed along the vertical axis, y, deflecting the particles in the $x - z$ plane.

The optimization criterion was, therefore, defined as:

$$\chi^2 = \left(\frac{\sigma(x)}{\sigma(y)}\right)^2 + \left(\frac{\sigma(y)}{\sigma(x)}\right)^2 \quad (1)$$

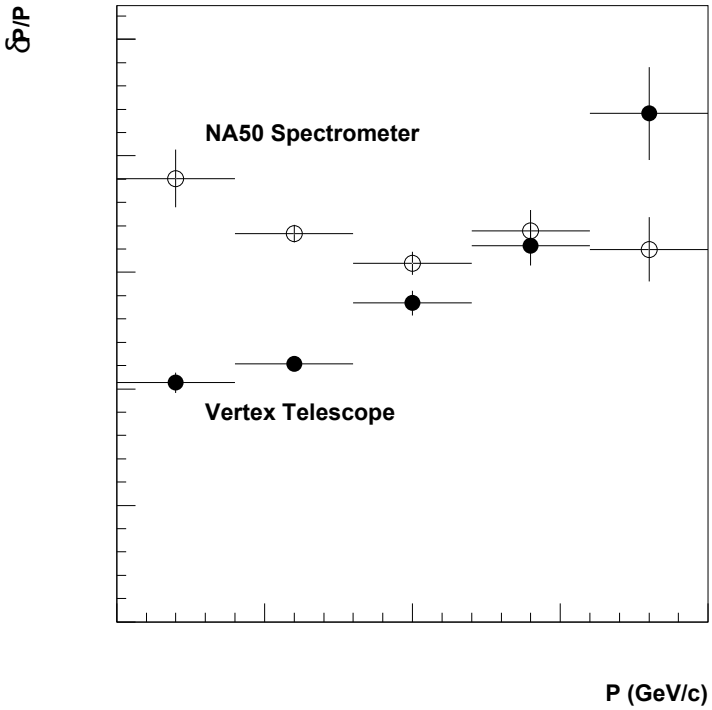
$$+\left(\frac{\sigma(\phi_x)}{\sigma(\phi_y)}\right)^2 + \left(\frac{\sigma(\phi_y)}{\sigma(\phi_x)}\right)^2 \quad (2)$$

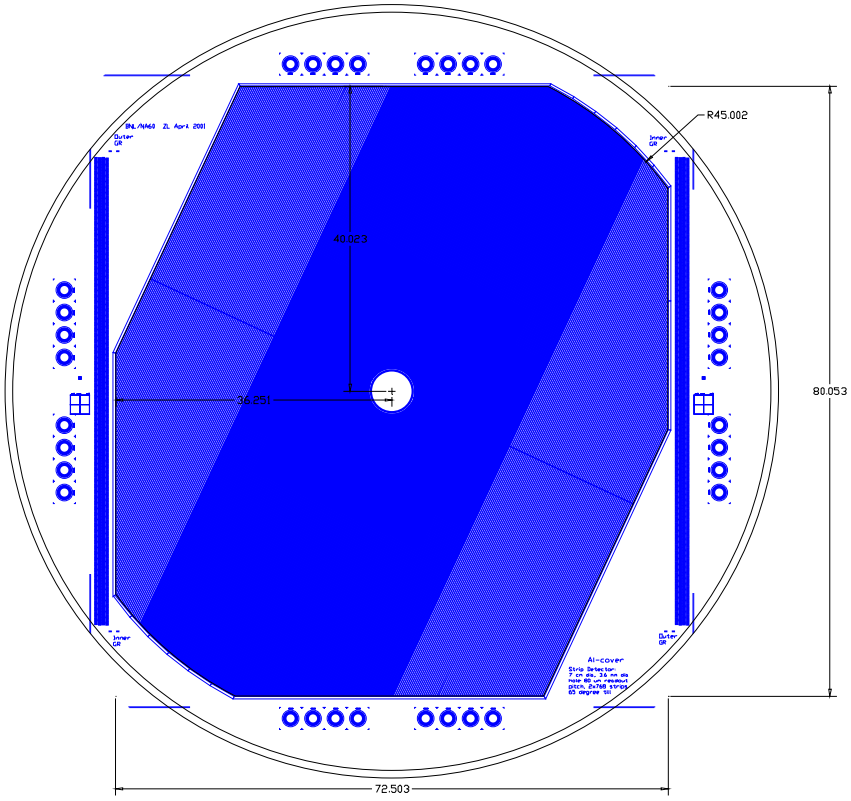
$$+\frac{\sigma(C)}{\sigma_{\rm ideal}(C)} \quad (3)$$

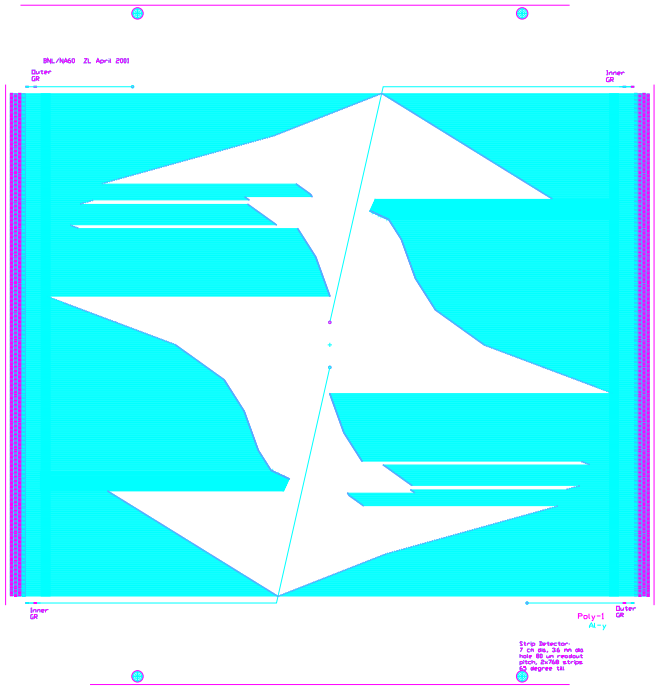
The selected value of the inclination angle provides a $\sigma(C)$ only 5 % higher than $\sigma_{\rm ideal}(C)$ and similar (within 20 %) offset and slope resolutions in x and y directions.

Unfortunately, the existing reconstruction software is not able to work with a mixed telescope, made of pixel and microstrip tracking planes. This makes it difficult to have a detailed study of the physics performance of the setup presented here. Nevertheless, by declaring the microstrips as a kind of very elongated pixels, we have been able to generate, by Monte-Carlo, a (small statistics) sample of reconstructed dimuons from ω decays. Figure 4 shows the momentum resolution of the simulated vertex telescope as a function of the muon momentum, compared to the resolution of the muon spectrometer. In the region of momenta relevant for the low-mass vector mesons (up to 15 GeV/c) the momentum resolution of the vertex spectrometer is now even better than that of the muon spectrometer.

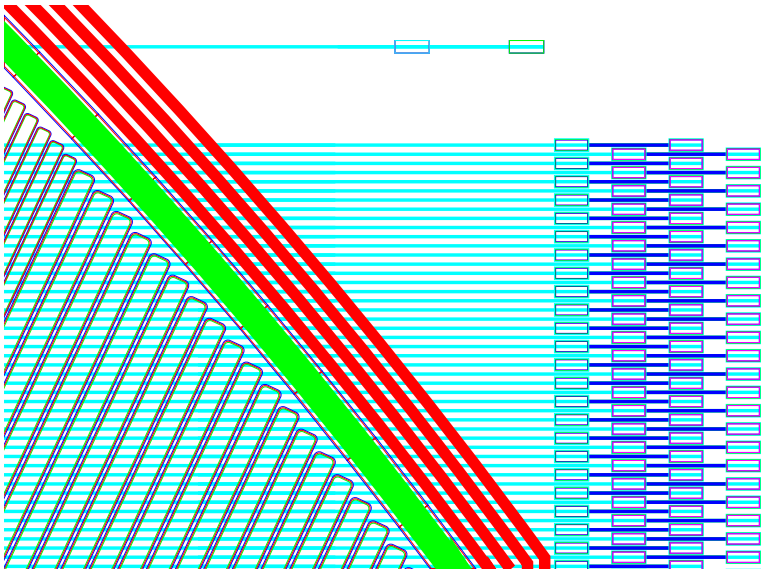
This new situation is considerably improved with respect to the values given in the NA60 proposal. The improved momentum resolution is due to the stronger magnetic field (2.5 T for the new PT7 magnet against the value 1.6 T of the previous TC8 magnet) and to the longer vertex telescope base (40 cm from the target to the last tracking plane, instead of the value 26 cm mentioned in the proposal). For the layout described in the proposal of NA60, the momentum resolution of the vertex telescope was ~ 3 times worse than the resolution of the muon spectrometer. The new calculated value for the mass resolution is 15-16 MeV/c^2, including the multiple scattering in the 2 mm thick Pb subtarget, to be compared with 20 MeV/c^2 for the setup described in the proposal. The offset resolution remains on the level of 35-40 μm, similar to the values given in the proposal.

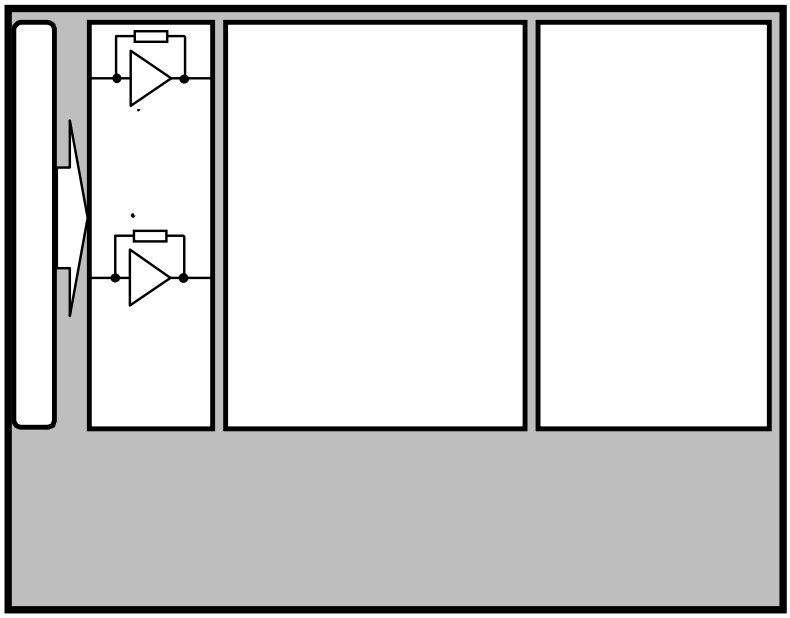

δP/P
NA50 Spectrometer
Vertex Telescope
P (GeV/c)


R45.002
40.023
36.251
80.053
72.503
Al-cover


BNL/MASD 21 April 2011
Outer GR
Inner GR
Inner GR
Outer GR
Poly-1
Al-y
Strip Detector
7 cm by 3.6 cm dia
n-in-p, 300 micron
pitch, 2x768 strips
90 degree tilt

that the effective pitch for the wire bonding is 160 μm. From the edge of the external bonding pads to the end of the silicon there is a distance of 577 μm.





4.2 The SCTA128VG version of the analogue chip

Although the SCTA128HC chip has been used successfully over the last two years to build detector modules one should not forget that this prototype has some limitations and should not be considered as a final version of the analogue chip. Development of the binary chip ABCD in the same DMILL technology has had a big impact on the planned improvements in the new version of the analogue chip. Apart from the changes implied by modified technology such as the introduction of new rad-hard resistors (RBXB type) and new structures for the input pads with a screening layer preventing parasitic coupling through the substrate, several improvements have been done in the front-end part.

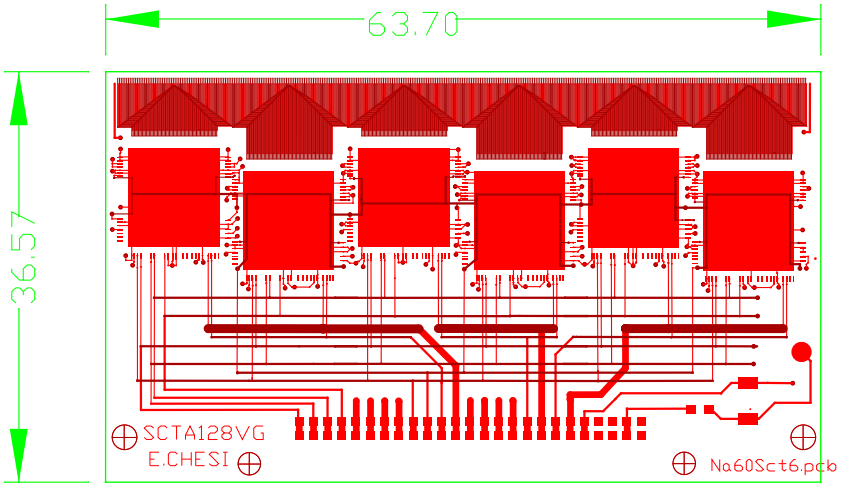
In April 2000 a new version of the analogue chip, the SCTA128VG, was submitted to the TEMIC foundry. The first stage of the preamplifier is identical to the ABCD3T design (the noise performance and radiation hardness is already proved). In the new design of the shaper stage we focused on the improvements of PSRR, immunity to spread of the process parameters, temperature and drifts during irradiation. The overall gain of the front-end stage was tuned to 50 mV/fC to be completely safe against the ADB pedestal spread and possible excess noise at the level of data transmission outside the chip. The stability of the front-end parameters with respect to temperature is improved by using a new band-gap reference for the bias DACs. Several changes in structure of the biasing and grounding of the front-end stage both on schematic and at the layout level have been applied to improve the stability of the chip working in detector system with millions of channels. During the optimisation of the circuit, special emphasis was placed on the reduction of possible variations in the circuit parameters with operating conditions (temperature and power supply) and the variations of process parameters from run to run.

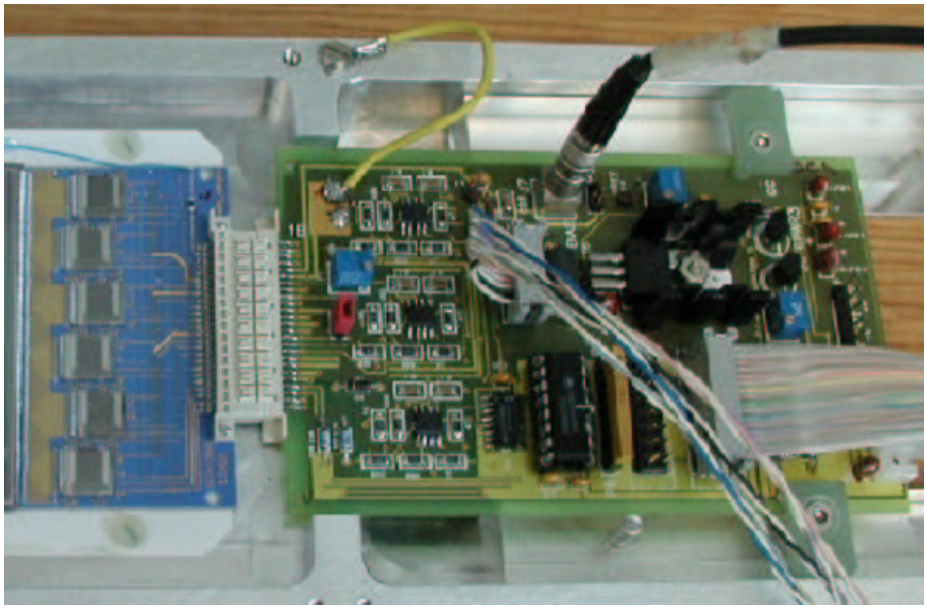
5 Description of the hybrid

The hybrid will hold either 4 or 6 readout chips, that read the signals from the sensor, via the wire bonds, and provide them to the service card, via a connector. Figure 10 shows the design of the hybrid.

This design is only very slightly different from the one used in the tests for ATLAS. In the NA60 application, the sensor will not be glued on top of the hybrid. Therefore, the long bias line in the ATLAS version was removed and replaced by a big pad where a wire can be connected, bringing the bias voltage to the back side of the sensor. The removal of the bias line was necessary to keep the wire bonds from the sensor to the hybrid within less than 3 mm long.

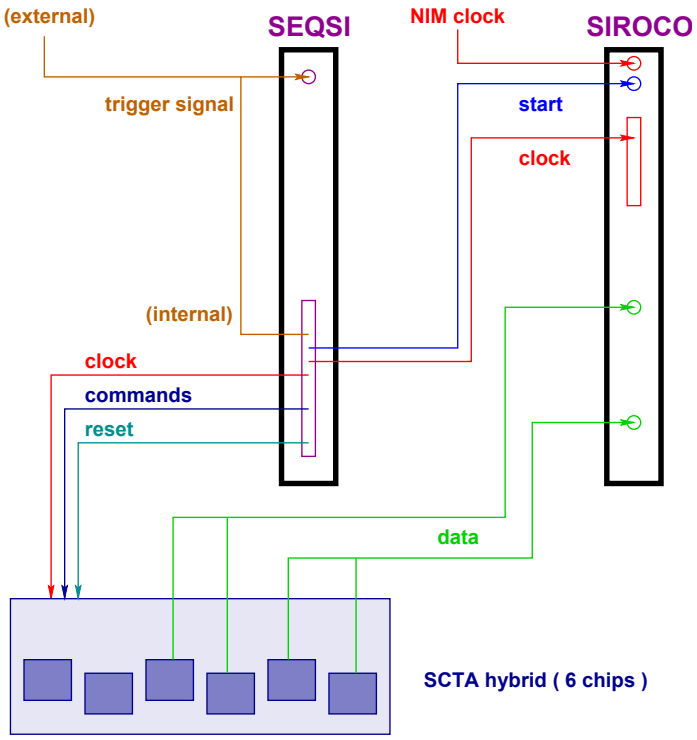
The other change concerns the order in which the chips are read out. When there are six chips in the hybrid, they are read in two steps, starting with the chips 1, 3 and 5 (counting from the right side in Fig. 10), followed by the chips 2, 4 and 6. In the case of the small strip planes, where the hybrids will be equiped with only the 4 most central chips, the chip number 1 is missing and, in the previous verion of the


63.70
36.57
SCTA128VG
E.CHESI
Na60Sct6.pcb



7 Experience from lab and beam tests

The SCT128A chip has been extensively studied in the lab where it has proved a good response uniformity and remarkable gain and noise characteristics. Several modules have been built using these chips on hybrids designed for operation with ATLAS type sensors and data has been taken on beam tests.



channels. It requires a clock signal with a fixed frequency and a start signal in order to set the beginning of the data sampling. The clock signal can be sent as NIM or ECL signal and can be adjusted to the frequency of the chip's multiplexer.

- *TDC*: provides useful timing information when signals generated by particles from radioactive sources are treated. The peaking time of that signal and the sampling time can be displaced by as much as the width of a clock cycle.

- *CORBO*: readout controller card used to generate VME interrupts in order to prevent the acceptance of external triggers when an event is being processed.

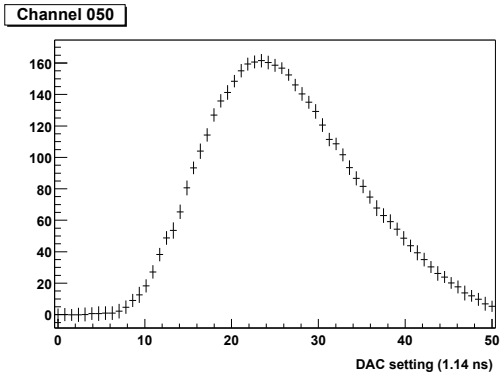
- *Fast-Carry Scaler*: gets the SEQSI clock and produces a clock signal with a lower frequency that can be used in the SIROCO when the multiplexer is running at a lower frequency.

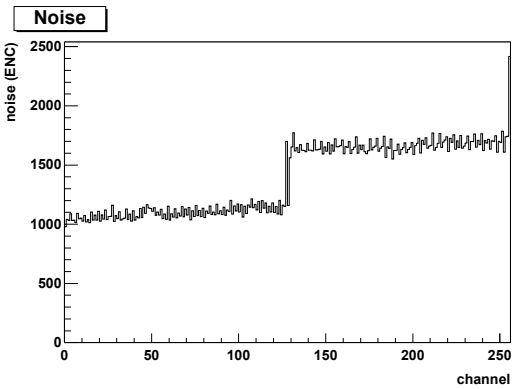
The software has been recently ported to the Linux operating system, making use of the new Linux driver for the National Instruments PCI-VXI card. It has a graphical user interface which allows to change all the settings of the chip and gives the user the possibility to select the trigger type and mode of operation. Thus, it is possible to use externally generated triggers (radioactive source, beam test) and internally generated triggers which can be optionally accompanied by calibration strobes (calibration with well known pulse amplitudes). Scans to find the correct timing and do a full characterization of the chips are easily accomplished via helpful menus.

The characterization of a chip is usually done through a procedure involving three steps. First of all, the correct timing is found for the sampling time of the calibration pulses generated internally on the chip. It is obtained through a scan of the strobe delay that gives us, basically, the shape of the pulse. Figure 13 shows the result of such a scan. Afterwards, we perform a scan over the calibration pulse height which yields a measurement of the gain and the electronic input noise of the channels of the chip. In Figs. 14 and 15 we see typical gain and noise plots for the channels of two chips on a hybrid. Finally, we make a scan over the cells of the analogue data buffer to check that the noise contribution due to variations in the cell pedestals is negligible (see Fig. 16).

Special attention must be paid to the synchronization between the clock sent to the chips and the command signals as well as to the synchronization between the clock sent to the SIROCO and the data coming back from the chips. Both clock signals can be delayed appropriately.

As commented previously, several modules composed by ATLAS sensors (two 6×6 cm^2 detectors bonded partially together to form 6 cm and 12 cm strips) and hybrids equipped with SCT128A chips were tested in beam tests showing an overall good performance. A telescope system formed by several planes of silicon detectors was used to build tracks and obtain the predicted hit positions on our SCT128A module.


Channel 050
160
140
120
100
80
60
40
20
0
0
10
20
30
40
50
DAC setting (1.14 ns)


Noise
noise (ENC)
2500
2000
1500
1000
500
0
0
50
100
150
200
250
channel

8 The data readout chain

A 6 channel ADC card (in EURO size A format) receives 6 analog signals from the 2 service cards of each sensor. After a digital compression and formatting, the data is sent over high speed LVDS to a PCI-FLIC card. A total of 4 PCI-FLIC cards in one PC are needed for reading the complete strip detector (16 sensors). A central module is needed to fanout various control signals.

The ADC card

These cards will be located a few meters from the detector. Each channel has a high bandwidth input buffer (AD8138) feeding a 10 bit, 40 Msample/s ADC (AD9203). The total gain (buffer+ADC) can be set such that the ADC resolution matches the r.m.s. noise of the signal.

Digital compression and formatting

The ADC is continuously sampling. Logic will detect the start of an event by its fixed header. Samples not belonging to an event are disregarded. Thereafter, a fixed number of samples per event are stored: $128 \times 4 \times 2$ in case of 4 consecutive time-samples for a pair of SCTAVG128 chips. A compression algorithm is applied to reduce the data volume by approximately a factor 2.

Transmission

The data of the 6 ADC channels is concatenated and serially transmitted over 'channel link' (DS90CR215 from National semiconductor) at a speed of 420 Mbit/s, which is the minimal (sic) speed achievable on channel link and resulting in the longest reliable transmission distance (around 20 meters).

FLIC mezzanine

The mezzanine has 4 channel link inputs and can acquire data from 4 ADC cards in parallel. Data on each input is buffered in a FIFO and sequentially forwarded through the S-link connection to the 32 Mbyte spill buffer on the PCI main card.

Central module

This module has the following functions:

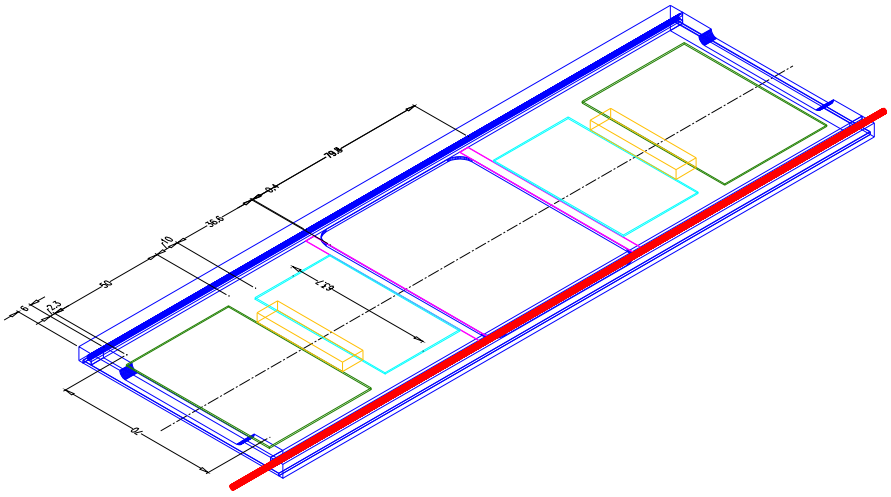
- configure the frontend IC's;
- operate all parts of the system synchronously at 40 MHz;
- fanout the trigger, burst and reset signals;

- produce a detector busy signal.

All signals are LVDS in shielded cables, to minimize emi in the system. It is placed adjacent to the ADC cards.

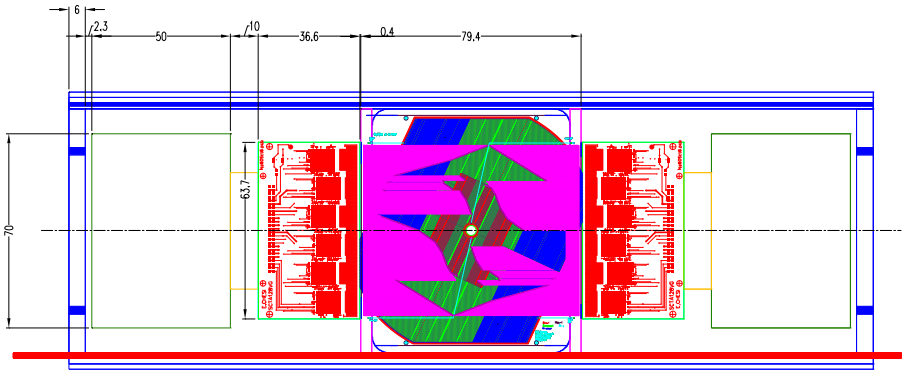
9 The microstrip tracking planes

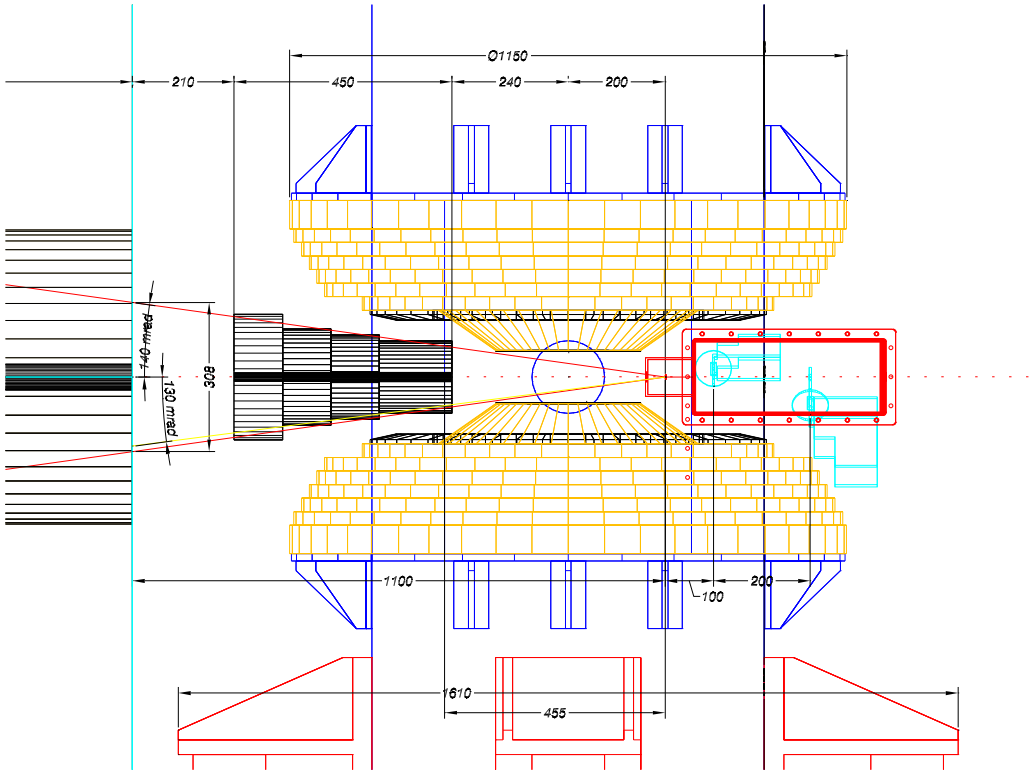
The telescope is composed of 16 tracking planes grouped in 8 modules of two 'back to back' planes. Each plane is made of an aluminium plate that holds one silicon microstrip detector, two hybrids and two service cards. Each aluminium plate is 1 mm thick and has a central hole, where the sensor is positioned, glued on its left and right edges. The sensor is separated from the aluminium plate by two strips of kapton for thermal isolation. The two hybrids are mounted to the left and right of the sensor, containing either 4 or 6 readout chips each, respectively for the 'small' and 'large' planes. The service cards are connected directly to the hybrids (no cables in between). During the tests in the laboratory, each aluminium plate is an independent unit. Only when positioned in the final telescope, each two planes will be assembled back to back in the eight modules. Figure 20 shows a 3-D view of one plane.



planes is 12 mm. The alignment between the two aluminium plates of a given module is guaranteed by bolts, positioned on the top and on the bottom of the frame, that traverse the aluminium from side to side. Two precisely drilled holes on the plates, only slightly larger than the diameter of the bolts, should impose an accurate relative alignment of the two planes of each module.

The height of the module is determined by the external (vertical) dimension of the sensor and should be 100 mm. This external height of the aluminium frame must be smaller than the gap of the PT7 magnet, 106 mm. The length of the aluminium frame (i.e. the dimension in the horizontal axis) is determined by the horizontal dimension of the sensor, the length of the hybrids, connectors and service cards. See Fig. 21 for a view of the sensor and hybrids placed in the frame.




Ø1150
210
450
240
200
740 max
130 max
308
1100
200
100
1610
455

good chips can be wire bonded on the hybrids in early August.

The first aluminium frame is being produced in the TA1 workshop, in a single piece. The cooling pipes, made of stainless steel, 2 mm diameter and 100 μm wall thickness, are also provided by TA1. The first tests of cooling will start as soon as we have the frame, using the ATLAS components to produce the heat on a 6-chip hybrid. Calculations of heat flow are being done by the ST-CV group and we should know soon if we can use dry nitrogen to keep the sensor at room temperature or if we will need to use water as coolant.

The final assembly and tests of all the components will take place in August and September so that, if there are no surprises, we have the telescope ready for the run in October.

Acknowledgements

It is a pleasure to thank Valeria Granata, Alan Honma, Rui de Oliveira, Antti Onnela, Alfredo Placci and Stefania Saladino for very helpful discussions concerning module assembly, mechanics and cooling issues. The exceptional help of Hannes Brugger with all the autocad drawings is gratefully acknowledged. Several other members of the NA60 collaboration have contributed and continue to contribute to a fast development of this recent project. Special thanks are due to Emmanuel Gangler, Bjorn Lenkeit, Hans Müller and Peter Rosinsky. We would like to acknowledge the important contribution of Carlos Lacasta to the DAQ system and software used in the lab and beam tests described in this note.

References

[1] H. Muller *et al.*, the FLIC card.

[2] J. Kaplon *et al.*, *DMILL Implementation of the Analogue Readout Architecture for Position Sensitive Detectors at LHC Experiments.*, Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998, CERN/LHCC/98-36

[3] W. Dabrowski *et al.*, *Performance of a 128 Channel Analogue Front-End Chip for Read-Out of Si Strip Detector Modules for LHC Experiments*, Proc. of the IEEE Nucl. Science Symposium, Seattle, IEEE Trans. on Nucl. Sci., in print.