





ISOLATED CAN TRANSCEIVER

Check for Samples: ISO1050

#### **FEATURES**

- 5000-V<sub>RMS</sub> Isolation (DW Package)
- 2500-V<sub>RMS</sub> Isolation (DUB Package)
- **Failsafe Outputs**
- Low Loop Delay: 150 ns Typical
- 50 kV/μs Typical Transient Immunity
- Meets or Exceeds ISO 11898 requirements
- Bus-Fault Protection of -27 V to 40 V
- **Dominant Time-Out Function**
- IEC 60747-5-2 (VDE 0884, Rev. 2) & IEC 61010-1 Approved
- **UL 1577, IEC 60950-1 and CSA Approvals Pending**
- 3.3-V Inputs are 5-V Tolerant

Typical 25-Year Life at Rated Working Voltage (see Application Report SLLA197 and Figure 15)

#### **APPLICATIONS**

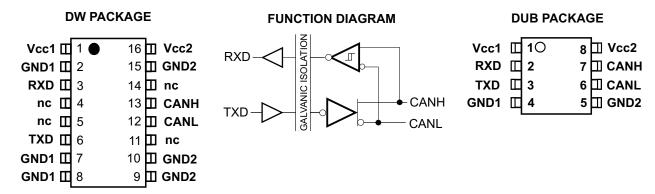
- CAN Data Buses
- **Industrial Automation** 
  - **DeviceNet Data Buses**
  - CANopen Data Buses
  - CANKingdom Data Buses
- Medical Scanning and Imaging
- **Security Systems**
- **Telecom Base Station Status and Control**
- **Building Automation**

#### DESCRIPTION

The ISO1050 is a galvanically isolated CAN transceiver that meets or exceeds the specifications of the ISO 11898 standard. The device has the logic input and output buffers separated by a silicon oxide (SiO<sub>2</sub>) insulation barrier that provides galvanic isolation of up to 5000 V<sub>RMS</sub> for DW Package and 2500 V<sub>RMS</sub> for DUB package. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection from -27 V to 40 V and over-temperature shut-down, as well as −12 V to 12 V common-mode range.

The ISO1050 is characterized for operation over the ambient temperature range of -55°C to 105°C.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1) (2)

|  |  |                                     |                                  | VALUE / UNIT   |  |
|--|--|-------------------------------------|----------------------------------|----------------|--|
| V <sub>CC1</sub> , V <sub>CC2</sub>    | Supply voltage (3)   |                                     |                                  | –0.5 V to 6 V  |  |
| V <sub>I</sub>                         | Voltage input (TXD)  |                                     |                                  | –0.5 V to 6 V  |  |
| V <sub>CANH</sub> or V <sub>CANH</sub> | r V <sub>CANH</sub> Voltage range at any bus terminal (CANH, CANL) |                                     |                                  |                |  |
| Io                                     | Receiver output current  | ±15 mA                              |                                  |                |  |
|  | Human Body Model   | JEDEC Standard 22, Method A114-C.01 | Bus pins and GND2 <sup>(4)</sup> | ±4 kV          |  |
| ESD                                    |  |                                     | All pins                         | ±4 kV          |  |
|  | Charged Device Model   | JEDEC Standard 22, Test Method C101 | All pins                         | ±1.5 kV        |  |
|  | Machine Model  | ANSI/ESDS5.2-1996                   | All pins                         | ±200 V         |  |
| T <sub>stg</sub>                       | Storage temperature  |                                     |                                  | –65°C to 150°C |  |
| TJ                                     | Junction temperature   |                                     |                                  | -55°C to 150°C |  |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This isolator is suitable for basic isolation within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.
- (3) All input and output logic voltage values are measured with respect to the GND1 logic side ground. Differential bus-side voltages are measured to the respective bus-side GND2 ground terminal.
- (4) Tested while connected between Vcc2 and GND2.

#### RECOMMENDED OPERATING CONDITIONS

|                                   |                                    |                         | MIN                | NOM | MAX                                | UNIT |
|-----------------------------------|------------------------------------|-------------------------|--------------------|-----|------------------------------------|------|
| V <sub>CC1</sub>                  | Supply voltage, controller si      | de                      | 3                  |     | 5.5                                | V    |
| V <sub>CC2</sub>                  | Supply voltage, bus side           |                         | 4.75               | 5   | 5.25                               | V    |
| V <sub>I</sub> or V <sub>IC</sub> | Voltage at bus pins (separate      | tely or common mode)    | -12 <sup>(1)</sup> |     | 12                                 | V    |
| V <sub>IH</sub>                   | High-level input voltage           | TXD                     | 2                  |     | 5.25                               | V    |
| V <sub>IL</sub>                   | Low-level input voltage            | TXD                     | 0                  |     | 0.8                                | V    |
| V <sub>ID</sub>                   | Differential input voltage         |                         | -7                 |     | 7                                  | V    |
|                                   | IPab lavel systems are             | Driver                  | -70                | -   | ^                                  |      |
| I <sub>OH</sub>                   | High-level output current          | Receiver                | -4                 |     | 5.5<br>5 5.25<br>12<br>5.25<br>0.8 | mA   |
|                                   | Law law law at a standard assessed | Driver                  |                    |     | 70                                 | 1    |
| I <sub>OL</sub>                   | Low-level output current           | Receiver                |                    |     | 4                                  | mA   |
| T <sub>A</sub>                    | Ambient Temperature                |                         | -55                |     | 105                                | °C   |
| TJ                                | Junction temperature (see T        | HERMAL CHARACTERISTICS) | -55                |     | 125                                | °C   |

<sup>(1)</sup> The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

#### **SUPPLY CURRENT**

over recommended operating conditions (unless otherwise noted)

|      | PARAMETE                        | ₹         | TEST CONDITIONS  | MIN TYP <sup>(1)</sup> | MAX | UNIT |
|------|---------------------------------|-----------|--|------------------------|-----|------|
|      | V Commissioners                 |           | $V_I = 0 \text{ V or } V_{CC1}$ , $V_{CC1} = 3.3 \text{V}$ | 1                      | 2   | A    |
| ICC1 | V <sub>CC1</sub> Supply current |           | $V_I = 0 \text{ V or } V_{CC1}$ , $V_{CC1} = 5V$           | 2                      | 3   | mA   |
|      | Dor                             |           | $V_I = 0 V$ , $60-\Omega$ Load                             | 52                     | 73  | A    |
| ICC2 | V <sub>CC2</sub> Supply current | Recessive | $V_I = V_{CC1}$  | 8                      | 12  | mA   |

(1) All typical values are at 25°C with  $V_{CC1} = V_{CC2} = 5V$ .



#### **DEVICE SWITCHING CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

| ı S  | ` ,                           |                 |     |     |     |      |
|--|-------------------------------|-----------------|-----|-----|-----|------|
| PARAME   | ΓER                           | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| t <sub>loop1</sub> Total loop delay, driver input to Dominant  | receiver output, Recessive to | See Figure 9    | 112 | 150 | 210 | ns   |
| t <sub>loop2</sub> Total loop delay, driver input to Recessive | receiver output, Dominant to  | See Figure 9    | 112 | 150 | 210 | ns   |

## **DRIVER ELECTRICAL CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

|                     | PARAMETER                              |                | TEST CONDITIONS   | MIN   | TYP  | MAX   | UNIT  |  |
|---------------------|--|----------------|---|-------|------|-------|-------|--|
|                     | Description (Description)              | CANH           | 0 - Francis de la Francis 0 1/2 0 1/2 D 2000  | 2.9   | 3.5  | 4.5   |       |  |
| $V_{O(D)}$          | Bus output voltage (Dominant)          | CANL           | See Figure 1 and Figure 2, $V_I = 0 \text{ V}$ , $R_L = 60\Omega$                           | 0.8   | 1.2  | 1.5   | V     |  |
| V <sub>O(R)</sub>   | Bus output voltage (Recessive)         |                | See Figure 1 and Figure 2, $V_I = 2 V$ , $R_L = 60 \Omega$                                  | 2     | 2.3  | 3     | V     |  |
| M                   | Differential output voltage (Deminent  | Δ.             | See Figure 1, Figure 2 and Figure 3, $V_I$ = 0 $V$ , $R_L$ = $60\Omega$                     | 1.5   |      | 3     | _     |  |
| $V_{OD(D)}$         | Differential output voltage (Dominant  | )              | See Figure 1, Figure 2, and Figure 3 $V_I$ = 0 $V$ , $R_L$ = 45 $\Omega$ , $V$ cc > 4.8 $V$ | 1.4   |      |       | V     |  |
| \/                  | Differential autout valtage (Deceasion | See Figure 1 a |   | -0.12 |      | 0.012 | V     |  |
| $V_{OD(R)}$         | Differential output voltage (Recessive | <del>)</del> ) | V <sub>I</sub> = 3 V, No Load –   |       |      | 0.05  | V     |  |
| V <sub>OC(D)</sub>  | Common-mode output voltage (Dom        | inant)         | See Figure 0  | 2     | 2.3  | 3     | V     |  |
| V <sub>OC(pp)</sub> | Peak-to-peak common-mode output        | voltage        | See Figure 8  |       | 0.3  |       | V     |  |
| I <sub>IH</sub>     | High-level input current, TXD input    |                | V <sub>I</sub> at 2 V   |       |      | 5     | μА    |  |
| I <sub>IL</sub>     | Low-level input current, TXD input     |                | V <sub>I</sub> at 0.8 V   | -5    |      |       | μА    |  |
| I <sub>O(off)</sub> | Power-off TXD leakage current          |                | V <sub>CC1</sub> , V <sub>CC2</sub> at 0 V, TXD at 5 V                                      |       |      | 10    | μА    |  |
|                     |  |                | See Figure 11, V <sub>CANH</sub> = -12 V, CANL Open   | -105  | -72  |       |       |  |
|                     | Chart aireuit ataadu atata autaut aurr | ont            | See Figure 11, V <sub>CANH</sub> = 12 V, CANL Open  |       | 0.36 | 1     | A     |  |
| I <sub>OS(ss)</sub> | Short-circuit steady-state output curr | ent            | See Figure 11, V <sub>CANL</sub> =–12 V, CANH Open  | -1    | -0.5 |       | mA    |  |
|                     |  |                | See Figure 11, V <sub>CANL</sub> = 12 V, CANH Open  |       | 71   | 105   |       |  |
| Co                  | Output capacitance                     |                | See receiver input capacitance  |       |      |       |       |  |
| CMTI                | Common-mode transient immunity         |                | See Figure 13, V <sub>I</sub> = V <sub>CC</sub> or 0 V                                      | 25    | 50   |       | kV/μs |  |

#### **DRIVER SWITCHING CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

|                  | PARAMETER  | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT |
|------------------|--|---|-----|-----|-----|------|
| t <sub>PLH</sub> | Propagation delay time, recessive-to-dominant output |   | 31  | 74  | 110 |      |
| t <sub>PHL</sub> | Propagation delay time, dominant-to-recessive output | 0.00 5 500000 4                         | 25  | 44  | 75  |      |
| t <sub>r</sub>   | Differential output signal rise time                 | See Figure 4                            | ,   | 20  | 50  | ns   |
| t <sub>f</sub>   | Differential output signal fall time                 |   | ,   | 20  | 50  |      |
| t <sub>dom</sub> | Dominant time-out                                    | ↓ C <sub>L</sub> =100 pF, See Figure 10 | 300 | 450 | 700 | μS   |

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#### RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

|                   | PARAMETER   | TEST CONDITIONS  | MIN                   | TYP <sup>(1)</sup> | MAX | UNIT  |
|-------------------|---|--|-----------------------|--------------------|-----|-------|
| V <sub>IT+</sub>  | Positive-going bus input threshold voltage  | Con Toble 1  |                       | 750                | 900 | mV    |
| V <sub>IT</sub> _ | Negative-going bus input threshold voltage  | See Table 1  | 500                   | 650                |     | mV    |
| V <sub>hys</sub>  | Hysteresis voltage (V <sub>IT+</sub> – V <sub>IT</sub> –)                                   |  |                       | 150                |     | mV    |
| \/                | Lligh level output voltage with \/cc E\/  | I <sub>OH</sub> = -4 mA, See Figure 6                  | $V_{CC} - 0.8$        | 4.6                |     | V     |
| V <sub>OH</sub>   | High-level output voltage with Vcc = 5V   | $I_{OH} = -20 \mu A$ , See Figure 6                    | V <sub>CC</sub> - 0.1 | 5                  |     | V     |
| \/                | High-level output voltage with Vcc1 = 3.3V  | I <sub>OL</sub> = 4 mA, See Figure 6                   | $V_{CC} - 0.8$        | 3.1                |     | V     |
| V <sub>OH</sub>   | nigh-level output voltage with vcc1 = 3.3v  | I <sub>OL</sub> = 20 μA, See Figure 6                  | V <sub>CC</sub> - 0.1 | 3.3                |     | V     |
|                   | Law lavel entent valtage  | I <sub>OL</sub> = 4 mA, See Figure 6                   |                       | 0.2                | 0.4 | V     |
| $V_{OL}$          | Low-level output voltage  | I <sub>OL</sub> = 20 μA, See Figure 6                  |                       | 0                  | 0.1 | V     |
| Cı                | Input capacitance to ground, (CANH or CANL)   | TXD at 3 V, $V_I = 0.4 \sin (4E6\pi t) + 2.5V$         |                       | 6                  |     | pF    |
| C <sub>ID</sub>   | Differential input capacitance  | TXD at 3 V, $V_I = 0.4 \sin (4E6\pi t)$                |                       | 3                  |     | pF    |
| R <sub>ID</sub>   | Differential input resistance   | TXD at 3 V   | 30                    |                    | 80  | kΩ    |
| R <sub>IN</sub>   | Input resistance (CANH or CANL)   | TXD at 3 V   | 15                    | 30                 | 40  | kΩ    |
| R <sub>I(m)</sub> | Input resistance matching (1 – [R <sub>IN (CANL)</sub> ] / R <sub>IN (CANL)</sub> ]) × 100% | V <sub>CANH</sub> = V <sub>CANL</sub>                  | -3%                   | 0%                 | 3%  |       |
| CMTI              | Common-mode transient immunity  | V <sub>I</sub> = V <sub>CC</sub> or 0 V, See Figure 13 | 25                    | 50                 |     | kV/μs |

<sup>(1)</sup> All typical values are at 25°C with  $V_{CC1} = V_{CC2} = 5V$ .

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

|                  | PARAMETER   | TEST CONDITIONS            | MIN | TYP | MAX | UNIT |
|------------------|---|----------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> | Propagation delay time, low-to-high-level output    |                            | 66  | 90  | 130 |      |
| t <sub>PHL</sub> | Propagation delay time, high-to-low-level output    | TXD at 3 V, See Figure 6   | 51  | 80  | 105 |      |
| t <sub>r</sub>   | Output signal rise time                             | TAD at 3 V, See Figure 6   |     | 3   | 6   | ns   |
| t <sub>f</sub>   | Output signal fall time                             |                            |     | 3   | 6   |      |
| t <sub>fs</sub>  | Failsafe output delay time from bus-side power loss | VCC1 at 5 V, See Figure 12 |     | 6   |     | μS   |



#### PARAMETER MEASUREMENT INFORMATION

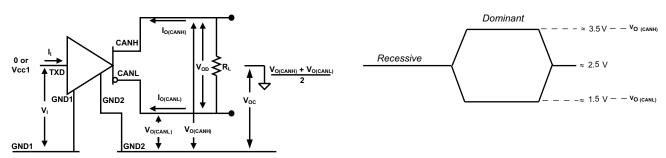


Figure 1. Driver Voltage, Current and Test Definitions

Figure 2. Bus Logic State Voltage Definitions

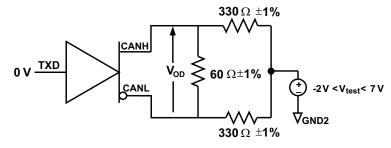
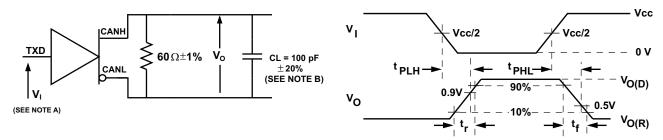


Figure 3. Driver V<sub>OD</sub> with Common-mode Loading Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_f \leq$  6 ns,  $t_f \leq$  6 ns,  $t_G \leq$  50 $\Omega$ .
- B. C<sub>L</sub> includes instrumentation and fixture capacitance within ±20%.

Figure 4. Driver Test Circuit and Voltage Waveforms

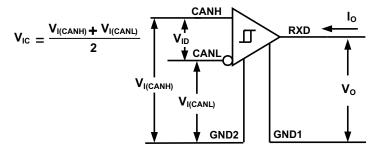
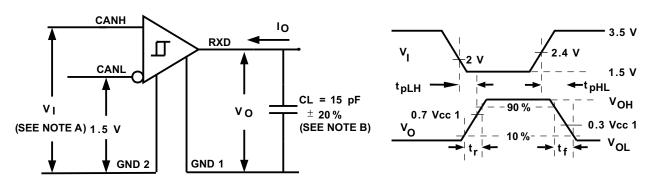


Figure 5. Receiver Voltage and Current Definitions



## PARAMETER MEASUREMENT INFORMATION (continued)

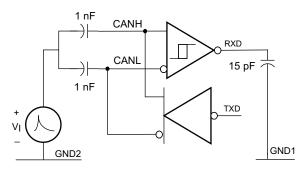


- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50\Omega$ .
- B. C<sub>1</sub> includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

**Table 1. Differential Input Voltage Threshold Test** 

|                   | INPUT             |                 |   | OUTPUT          |
|-------------------|-------------------|-----------------|---|-----------------|
| V <sub>CANH</sub> | V <sub>CANL</sub> | V <sub>ID</sub> |   | R               |
| –11.1 V           | -12 V             | 900 mV          | L |                 |
| 12 V              | 11.1 V            | 900 mV          | L | .,              |
| -6 V              | -12 V             | 6 V             | L | V <sub>OL</sub> |
| 12 V              | 6 V               | 6 V             | L |                 |
| –11.5 V           | -12 V             | 500 mV          | Н |                 |
| 12 V              | 11.5 V            | 500 mV          | Н |                 |
| -12 V             | -6 V              | -6 V            | Н | V <sub>OH</sub> |
| 6 V               | 12 V              | -6 V            | Н |                 |
| Open              | Open              | X               | Н |                 |



The waveforms of the applied transients are in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b.

Figure 7. Transient Over-Voltage Test Circuit



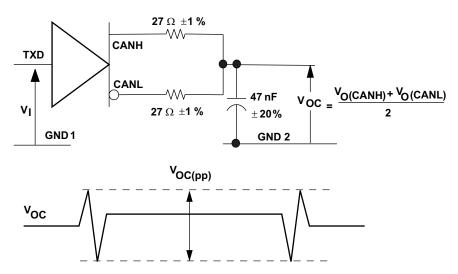


Figure 8. Peak-to-Peak Output Voltage Test Circuit and Waveform

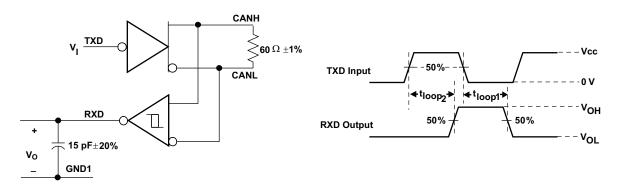
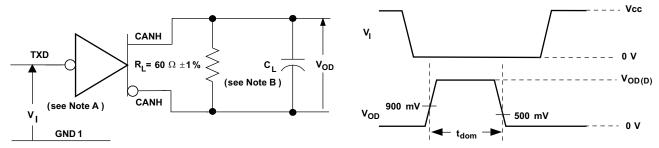


Figure 9. t<sub>LOOP</sub> Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50\Omega$ .
- B. C<sub>L</sub> includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Timeout Test Circuit and Voltage Waveforms



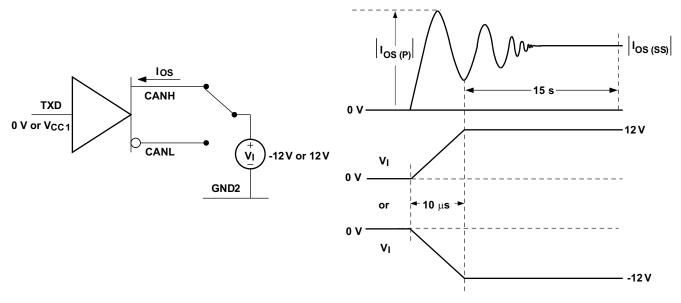


Figure 11. Driver Short-Circuit Current Test Circuit and Waveforms

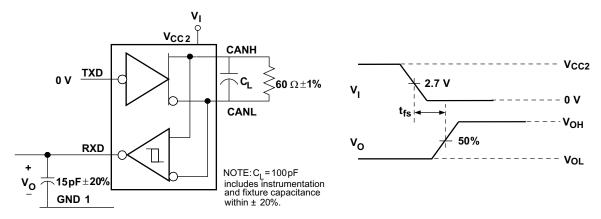


Figure 12. Failsafe Delay Time Test Circuit and Voltage Waveforms



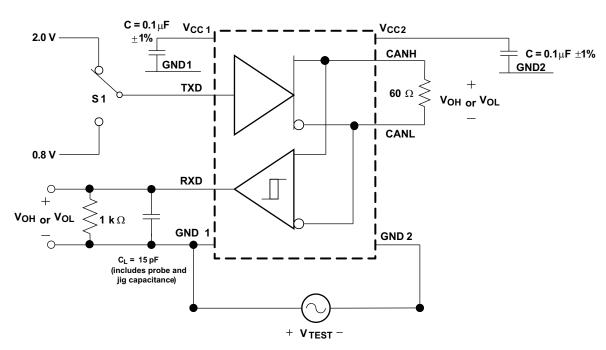


Figure 13. Common-Mode Transient Immunity Test Circuit

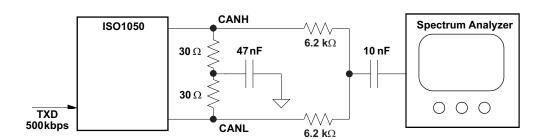


Figure 14. Electromagnetic Emissions Measurement Setup

#### **DEVICE INFORMATION**

## **FUNCTION TABLE**(1)

|                  |      | DRIVER |           | RECEIVER   |        |           |  |
|------------------|------|--------|-----------|--|--------|-----------|--|
| INPUTS           | OUTI | PUTS   | BUS STATE | DIFFERENTIAL INPUTS                                    | OUTPUT | BUS STATE |  |
| TXD              | CANH | CANL   | BUSSIAIE  | V <sub>ID</sub> = CANH-CANL                            | RXD    | BUS STATE |  |
| L <sup>(2)</sup> | Н    | L      | DOMINANT  | V <sub>ID</sub> ≥ 0.9 V                                | L      | DOMINANT  |  |
| Н                | Z    | Z      | RECESSIVE | $0.5 \text{ V} < \text{V}_{\text{ID}} < 0.9 \text{ V}$ | ?      | ?         |  |
| Open             | Z    | Z      | RECESSIVE | V <sub>ID</sub> ≤ 0.5 V                                | Н      | RECESSIVE |  |
| Х                | Z    | Z      | RECESSIVE | Open   | Н      | RECESSIVE |  |

<sup>(1)</sup> H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

<sup>(2)</sup> Logic low pulses to prevent dominant time-out.



## ISOLATOR CHARACTERISTICS (1) (2)

over recommended operating conditions (unless otherwise noted)

|                 | PARAMETER                                 | TEST CONDITIONS  |       | MIN   | TYP               | MAX | UNIT |
|-----------------|---|--|-------|-------|-------------------|-----|------|
| L(I01)          | Minimum air gap (Clearance)               | Shortest terminal to terminal distance through air   |       | 6.1   |                   |     | mm   |
| L(102)          | Minimum external tracking (Creepage)      | Shortest terminal to terminal distance across the package surface  | DUB-8 | 6.8   |                   |     | mm   |
| L(I01)          | Minimum air gap (Clearance)               | Shortest terminal to terminal distance through air   |       | 8.34  |                   |     | mm   |
| L(102)          | Minimum external tracking (Creepage)      | Shortest terminal to terminal distance across the package surface  | DW-16 | 8.10  |                   |     | mm   |
|                 | Minimum Internal Gap (Internal Clearance) | Distance through the insulation  |       | 0.014 |                   |     | mm   |
| R <sub>IO</sub> | Isolation resistance                      | Input to output, V <sub>IO</sub> = 500 V, all pins on each side of barrier tied together creating a two-terminal device, 100°C |       |       | >10 <sup>12</sup> |     | Ω    |
|                 |   | Input to output V <sub>IO</sub> = 500 V, 100°C ≤Tamb <≤Tamb  | max   |       | >10 <sup>11</sup> |     | Ω    |
| C <sub>IO</sub> | Barrier capacitance                       | $V_1 = 0.4 \sin(4E6\pi t)$   |       |       | 1.9               |     | pF   |
| C <sub>I</sub>  | Input capacitance to ground               | $V_1 = 0.4 \sin(4E6\pi t)$   |       |       | 1.3               |     | pF   |

<sup>(1)</sup> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

## **INSULATION CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

|                   | PARAMETI                             | ≣R            | TEST CONDITIONS                                     | SPECIFICATION     | UNIT  |  |
|-------------------|--------------------------------------|---------------|---|-------------------|-------|--|
|                   | Maximum working insulation           | 8-DUB Package |   | 560               | \     |  |
| $V_{IORM}$        | voltage per IEC                      | 16-DW Package |   | 1200              | Vpeak |  |
|                   |                                      | 8-DUB Package | V <sub>PR</sub> = 1.875 x V <sub>IORM</sub> , t = 1 | 1050              |       |  |
| $V_{PR}$          | Input to output test voltage per IEC | 16-DW Package | sec (100% production) Partial discharge < 5 pC      | 2250              | Vpeak |  |
| V <sub>IOTM</sub> | Transient overvoltage per IEC        |               | t = 60 sec (qualification)                          | 4000              | Vpeak |  |
|                   |                                      |               | t = 1 sec (100% production)                         | 4000              |       |  |
|                   |                                      | 0.0110.0      | t = 60 sec (qualification)                          | 2500              | \ /   |  |
| .,                | loolation valtage man I II           | 8-DUB Package | t = 1 sec (100% production)                         | 3000              | Vrms  |  |
| $V_{ISO}$         | Isolation voltage per UL             | 4C DW Dealers | t = 60 sec (qualification)                          | 5000              | .,    |  |
|                   |                                      | 16-DW Package | t = 1 sec (100% production)                         | 6000              | Vrms  |  |
| R <sub>S</sub>    | Isolation voltage per UL             |               | $V_{IO}$ = 500 V at $T_{S}$                         | > 10 <sup>9</sup> | Ω     |  |
|                   | Pollution Degree                     |               |   | 2                 |       |  |

#### **IEC 60664-1 RATINGS**

| PARAMETER                   | TEST CONDITIONS                | SPECIFICATION |
|-----------------------------|--------------------------------|---------------|
| Basic isolation group       | Material group                 | III-a         |
|                             | Rated mains voltage ≤ 150 Vrms | I–IV          |
| Installation classification | Rated mains voltage ≤ 300 Vrms | <b>III</b>    |
|                             | Rated mains voltage ≤ 400 Vrms | I–II          |

<sup>(2)</sup> Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.



#### **IEC SAFETY LIMITING VALUES**

safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

|  | PARAMETER        |   |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT | 1 |
|--|------------------|---|---|---|-----|-----|-----|------|---|
|  | I <sub>S</sub> S | Safety input, output, or supply current | DUB-8   | $\theta_{JA} = 73.3 \text{ °C/W}, V_I = 5.5 \text{ V}, T_J = 150 \text{°C}, T_A = 25 \text{°C}$   |     |     | 310 | A    | 1 |
|  |                  |   |   | $\theta_{JA} = 73.3 \text{ °C/W}, V_I = 3.6 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}$ | 474 |     |     | mA   |   |
|  |                  |   |   | $\theta_{JA} = 76 \text{ °C/W}, V_I = 5.5 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}$   |     |     | 299 |      |   |
|  |                  | DW-16                                   | $\theta_{JA} = 76 \text{ °C/W}, V_I = 3.6 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}$ |   |     | 457 | mA  |      |   |
|  | T <sub>S</sub>   | Maximum case temperature                |   |   |     |     | 150 | °C   | Ī |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assured junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

#### REGULATORY INFORMATION

| VDE                                  | CSA  | UL   |
|--------------------------------------|--|--|
| Certified according to IEC 60747-5-2 | Approved under CSA Component Acceptance Notice | Recognized under 1577 Component Recognition Program <sup>(1)</sup> |
| File Number: 40016131                | File Number: pending                           | File Number: pending   |

<sup>(1)</sup> Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

#### THERMAL INFORMATION (DUB-8 PACKAGE)

over recommended operating conditions (unless otherwise noted)

|                         | PARAMETER                            | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT |
|-------------------------|--------------------------------------|---|-----|------|-----|------|
| 0                       | lunction to air                      | Low-K Thermal Resistance <sup>(1)</sup>   |     | 120  |     | °C/W |
| $\theta_{JA}$           | Junction-to-air                      | High-K Thermal Resistance   |     | 73.3 |     | °C/W |
| $\theta_{JB}$           | Junction-to-board thermal resistance | Low-K Thermal Resistance  |     | 10.2 |     | °C/W |
| $\theta_{JC}$           | Junction-to-case thermal resistance  | Low-K Thermal Resistance  |     | 14.5 |     | °C/W |
| P <sub>D</sub>          | Device power dissipation             | $V_{\rm CC1}$ =5.5V, $V_{\rm CC2}$ =5.25V, $T_{\rm A}$ =105°C, $R_{\rm L}$ = 60 $\Omega$ , TXD input is a 500kHz 50% duty-cycle square wave |     |      | 200 | mW   |
| T <sub>j shutdown</sub> | Thermal shutdown temperature (2)     |   |     | 190  |     | °C   |

<sup>(1)</sup> Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

#### THERMAL INFORMATION (DW-16 PACKAGE)

|                  |  | ISO1050 |       |  |
|------------------|--|---------|-------|--|
|                  | THERMAL METRIC <sup>(1)</sup>                | DW      | UNITS |  |
|                  |  | 16      |       |  |
| $\theta_{JA}$    | Junction-to-ambient thermal resistance       | 76.0    |       |  |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance    | 41      |       |  |
| θ <sub>ЈВ</sub>  | Junction-to-board thermal resistance         | 47.7    | 00044 |  |
| ΨЈТ              | Junction-to-top characterization parameter   | 14.4    | °C/W  |  |
| √JВ              | Junction-to-board characterization parameter | 38.2    |       |  |
| 9<br>JCbot       | Junction-to-case (bottom) thermal resistance | n/a     |       |  |

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

<sup>(2)</sup> Extended operation in thermal shutdown may affect device reliability.



# LIFE EXPECTANCY vs WORKING VOLTAGE (8-DUB PACKAGE)

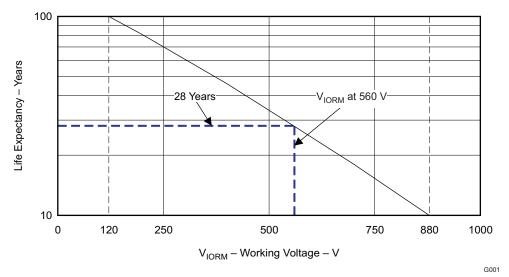
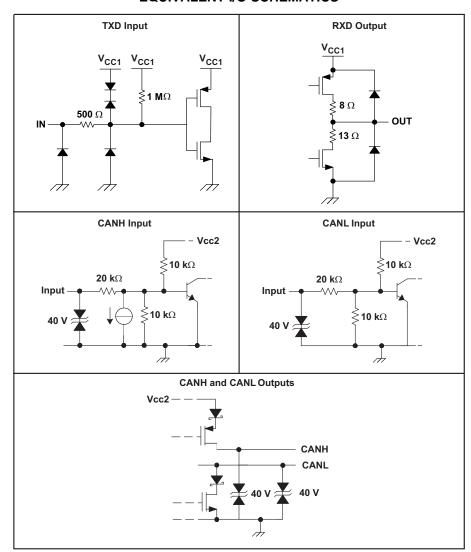


Figure 15. Life Expectancy vs Working Voltage



## **EQUIVALENT I/O SCHEMATICS**



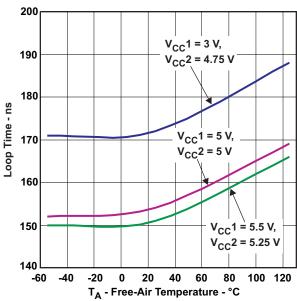


#### **TYPICAL CHARACTERISTICS**

#### RECESSIVE-TO-DOMINANT LOOP TIME

VS

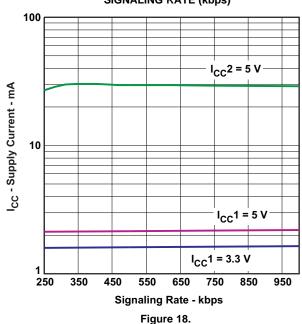
FREE-AIR TEMPERATURE (across Vcc)



#### Figure 16.

#### **SUPPLY CURRENT (RMS)**

SIGNALING RATE (kbps)



## DOMINANT-TO-RECESSIVE LOOP TIME

vs

FREE-AIR TEMPERATURE (across Vcc)

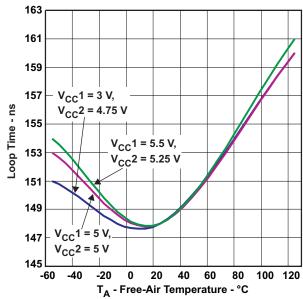


Figure 17.

#### DRIVER OUTPUT VOLTAGE

vs

FREE-AIR TEMPERATURE

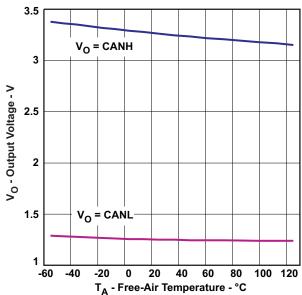
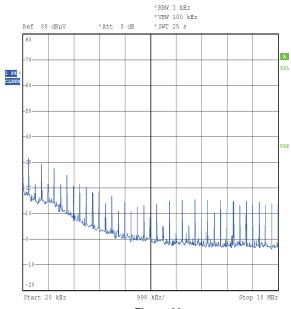


Figure 19.



# **TYPICAL CHARACTERISTICS (continued)**

#### **EMISSIONS SPECTRUM TO 10 MHz**



#### **EMISSIONS SPECTRUM TO 50 MHz**

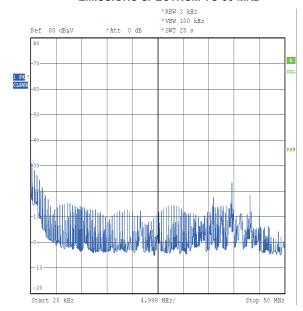


Figure 21.



#### APPLICATION INFORMATION

#### **DOMINANT TIME-OUT**

A dominant time-out circuit in the ISO1050 prevents the driver from blocking network communications if a local controller fault occurs. The time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs on TXD before the time-out of the circuits expires, the driver is disabled to prevent the local node from continuously transmitting a Dominant bit. If a rising edge occurs on TXD, commanding a Recessive bit, the timer will be reset and the driver will be re-enabled. The time-out value is set so that normal CAN communication will not cause the Dominant time-out circuit to expire.

#### **FAILSAFE**

If the bus-side power supply Vcc2 is lower than about 2.7V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent spurious transitions due to an unstable supply. If Vcc1 is still active when this occurs, the receiver output will go to a failsafe HIGH value in about 6 microseconds.

#### THERMAL SHUTDOWN

The ISO1050 has an internal thermal shutdown circuit that turns off the driver outputs when the internal temperature becomes too high for normal operation. This shutdown circuit prevents catastrophic failure due to short-circuit faults on the bus lines. If the device cools sufficiently after thermal shutdown, it will automatically re-enable, and may again rise in temperature if the bus fault is still present. Prolonged operation with thermal shutdown conditions may affect device reliability.

#### **BUS LOADING**

In the CAN standard ISO 11898-2 the driver differential output is specified with a  $60\Omega$  load (must be greater than 1.5V) and with a fully-loaded bus (must be greater than 1.2V). The ISO1050 is specified to meet the 1.5V requirement with a  $60\Omega$  load, and 1.4V with a  $45\Omega$  load. The differential input resistance of the ISO1050 is a minimum of  $30K\Omega$ . If the 167 transceivers are in parallel on a bus, this is equivalent to a  $180\Omega$  differential load. That transceiver load of  $180\Omega$  in parallel with the  $60\Omega$  (two  $120\Omega$  termination resistors) gives a total  $45\Omega$ . Therefore, the ISO1050 supports over 167 transceivers on a single bus segment, with margin to the 1.2V CAN requirement.



## **REVISION HISTORY**

| Changes from Original (June 2009) to Revision A  | Page |
|--|------|
| Added Typical 25-Year Life at Rated Working Voltage to Features  | 1    |
| Added LIFE EXPECTANCY vs WORKING VOLTAGE section   | 12   |
| Changes from Revision A (Sept 2009) to Revision B  | Page |
| Added information that IEC 60747-5-2 and IEC61010-1 have been approved                                       | 1    |
| Changed DW package from preview to production data   | 1    |
| Added Insulation Characteristics and IEC 60664-1 Ratings tables  | 10   |
| Added IEC file number  |      |
| Added DW-16 thermal information table  | 11   |
| Changes from Revision B (June 2009) to Revision C  | Page |
| Changed the IEC 60747-5-2 Features bullet From: DW package Approval Pending To: VDE approved and DW packages |      |
| • Changed the Minimum Interal Gap value from 0.008 to 0.014 in the Isolator Characteristics table            | 10   |
| Changed V <sub>IORM</sub> Specification From: 1300 To: 1200 per VDE certification                            | 10   |
| Changed V <sub>PR</sub> Specification From 2438 To: 2250   | 10   |
| Added the Bus Loading paragraph to the Application Information section                                       | 16   |





8-Jul-2010

#### **PACKAGING INFORMATION**

| Orderable Device | Status (1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| ISO1050DUB       | ACTIVE     | SOP          | DUB                | 8    | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-4-260C-72 HR           |                             |
| ISO1050DUBR      | ACTIVE     | SOP          | DUB                | 8    | 350         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-4-260C-72 HR           |                             |
| ISO1050DW        | PREVIEW    | SOIC         | DW                 | 16   | 40          | TBD                        | Call TI              | Call TI                      |                             |
| ISO1050DWR       | PREVIEW    | SOIC         | DW                 | 16   | 2000        | TBD                        | Call TI              | Call TI                      |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width     |
|----|---|
| B0 | Dimension designed to accommodate the component length    |
|    | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device      | Package<br>Type | Package<br>Drawing |   |     | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|-------------|-----------------|--------------------|---|-----|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| ISO1050DUBR | SOP             | DUB                | 8 | 350 | 330.0                    | 24.4                     | 10.9       | 10.01      | 5.85       | 16.0       | 24.0      | Q1               |

**PACKAGE MATERIALS INFORMATION** 

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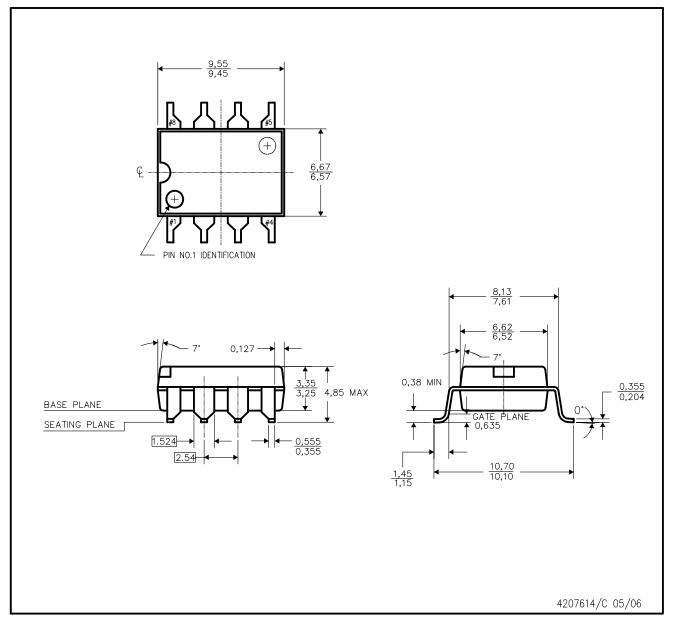


#### \*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| ISO1050DUBR | SOP          | DUB             | 8    | 350 | 358.0       | 335.0      | 35.0        |

# DUB (R-PDSO-G8)

# PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M-1982.

- B. This drawing is subject to change without notice.
- C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.



# DW (R-PDSO-G16)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



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