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Digitally Assisted Adaptive Equalizer in 90 nm With Wide Range Support From 2.5 Gbps to 6.5 Gbps

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Abstract

This paper describes a production-worthy adaptive equalizer used for integrating a transceiver on an FPGA. Since FPGAs are required to support a wide customer base, it is desirable to have a design flexible enough to adapt to different types of backplanes, drivers and data rates. This is extremely challenging since the data rate of the transceiver varies from 622 Mbps to 6.5 Gbps. The goal of the adaptive equalizer is to support a data rate of 2.5 Gbps to 6.5 Gbps with no backplane attenuation and up to 17 dB of attenuation. Meeting these requirements requires over 1600 equalization settings and four stages of equalizer. Choosing the optimal setting would be impractical since each link would have different characteristics. Once the optimal setting has been chosen it might need to be changed if the environment changes due to aging or drifts in voltage or temperature. An adaptive equalizer is a critical requirement for the application. This paper describes a digitally-assisted equalizer that meets these goals.

Authors Biographies

Wilson Wong is a principle design engineer at Altera Corporation. Wilson Wong has more than 17 years of experience in analog circuit design. His current interests include high-speed equalization, adaptive equalization and clock data recovery circuits. Prior to joining Altera, Mr. Wong worked at Nexgen Microsystems and Tredennick Inc. He holds a BSEE from the University of California, Berkeley.

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Tin Lai is a member of technical staff at Altera Corp. Tin has over 12 years of experience in digital and analog design and development. Tin has worked on 3.125 Gbps and 8.5 Gbps SERDES in Altera® Stratix® GX and Stratix II GX product lines. Tin spent a one year internship with Intel Corporation in Folsom, California. He holds a B.S. degree in Electrical Engineering from UC Berkeley.

Simar Maangat is a member of technical staff at Altera Corporation. Simar Maangat has seven years of experience at Altera Corp. mainly in analog design development. Mr. Maangat has worked on 3.125 Gbps and 6.375 Gbps SERDES in Altera's Stratix GX and Stratix II GX product lines. Prior to joining Altera Corp., Mr. Maangat interned at Digital Equipment Corporation (DEC) in Palo Alto. He holds a B.S. degree in Electrical Engineering from UC Berkeley.

Tim Hoang is a senior manager at Altera Corporation. Since joining Altera in 1993, he has been working on the design of various circuits. He is currently involved in the design of next-generation high-speed, low-power PLLs, and CDR. He received a BSEE from University of California at Berkeley in 1993.

Tina Tran is a senior design manager at Altera Corporation. Tina Tran is working in the design group responsible for the development of high-speed transceivers at Altera. She has been in the semiconductor industry for more than 15 years including almost 10 years with Altera. She holds a BSEE from the University of California, Berkeley.

Introduction

Recent work on adaptive equalization shows the feasibility of multigigabit adaptation. To support a wide customer base, it is desirable to have a design flexible enough to adapt to different types of backplanes, drivers and data rates. The design described in [1] is implemented on 0.18- μm CMOS technology and can boost up to 20 dBs at up to 3.5 Gbps. Since the amount of attenuation and low frequency swing is unknown for any given customer driver and backplane, paper [1] proposes the need for combining low frequency adaptation and high frequency boost. The design in [2] is implemented on 0.13 μm and equalizes up to 30" of backplane trace at 10 Gbps. Conventional adaptive equalizers utilize an analog approach to generate the control voltage for the equalizer. The amount of boost is stored on an integrating capacitor. Previous designs support only one control voltage to vary the equalization. These constraints make it difficult to support a wide range of data rates and backplanes, thus many existing designs target very specific backplanes and input amplitude levels.

Architecture

This paper discusses the choice of a digitally assisted implementation for adaptive equalization. Figure 1 shows the block diagram of the adaptive equalizer. The digital approach allows greater flexibility and enables adapting to unknown customer backplanes and drivers as well as a wide data range. The design targets a data rate of 2.5 Gbps to 6.5 Gbps.

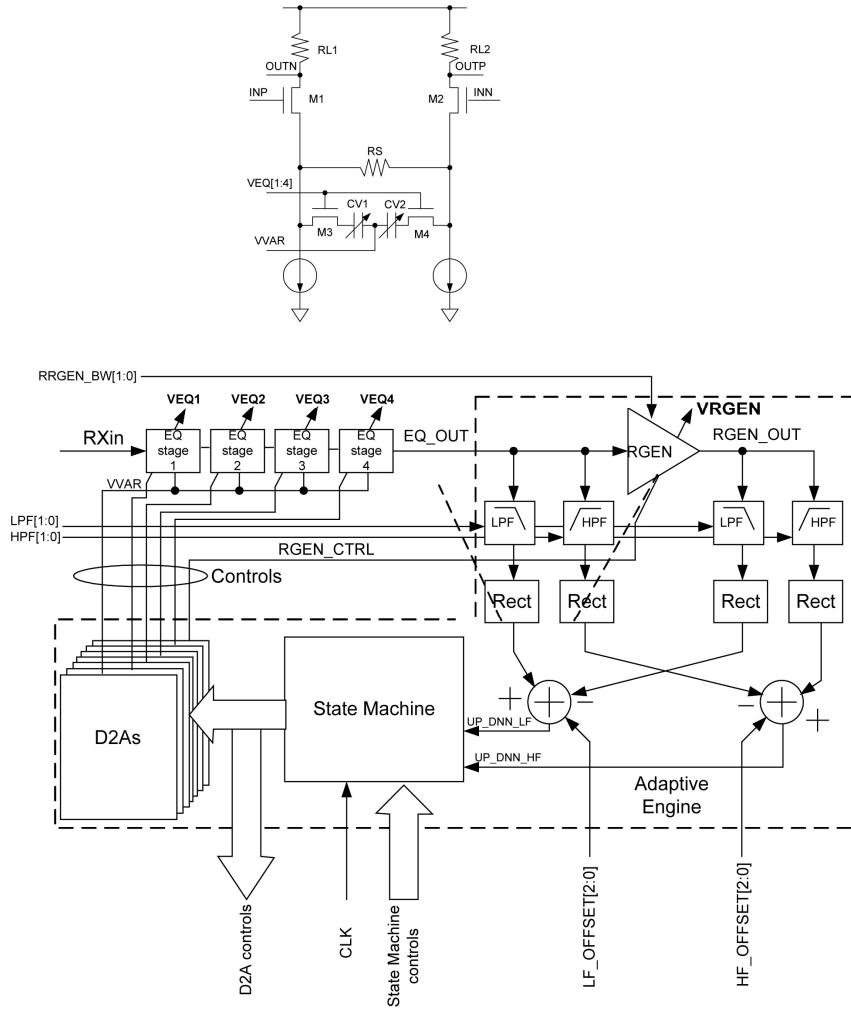


Figure 1. Adaptive Equalizer Block Diagram and Equalizer Details

A flexible state machine controls an 8-bit D2A and generates the control voltages for four equalizer stages and a reference edge generator (RGEN). The 256-level D2A output ranges from 0V to 1.2V with a voltage increment of roughly 4.7mV. A digital approach easily allows a “one-time adaptation” option by locking in the final adaptation values to reduce power and noise. The D2A values can easily be read out to allow link monitoring. The adaptation settings can be monitored to check if the system environment has changed and whether re-optimization is required.

The RGEN is a limiting amplifier and generates “ideal” edges for the equalizer output to compare against. As described in [1], a dual loop approach is required for optimal adaptation where the low frequency voltage amplitude (voltage level after a long run of ones or zeros) is unknown. The low pass filters and rectifiers extract the low frequency content of the RGEN and equalizer outputs. The low frequency loop compares the low frequency content and generates control voltage VRGEN to control the low frequency amplitude of the RGEN to match that of the equalizer. The RGEN is a limiting amplifier consisting of a simple multistage CML design. Varying the tail current changes the amplitude. Once the low frequency loop has set the low frequency amplitude of the

RGEN block to match the equalizer output, the high frequency loop adjusts the high frequency boost of the four equalizer stages by comparing its output against the “ideal” edges generated by the RGEN block.

Simulation Results and Methodology

The state machine has many features to enhance adaptation and flexibility. Programmable clock division for the low and high frequency loops allows controlling the adaptation rates of the two loops individually. The frequencies should be different to prevent the two loops from interacting. The state machine controls the sequence of boost, how many equalizer stages are boosted together and the maximum value each can be boosted. For example, stage 1 can be followed by stage 2 and so on. Alternatively, stage 1 and 2 can be boosted together, followed by stage 3. Figure 2 shows a sample adaptation sequence.

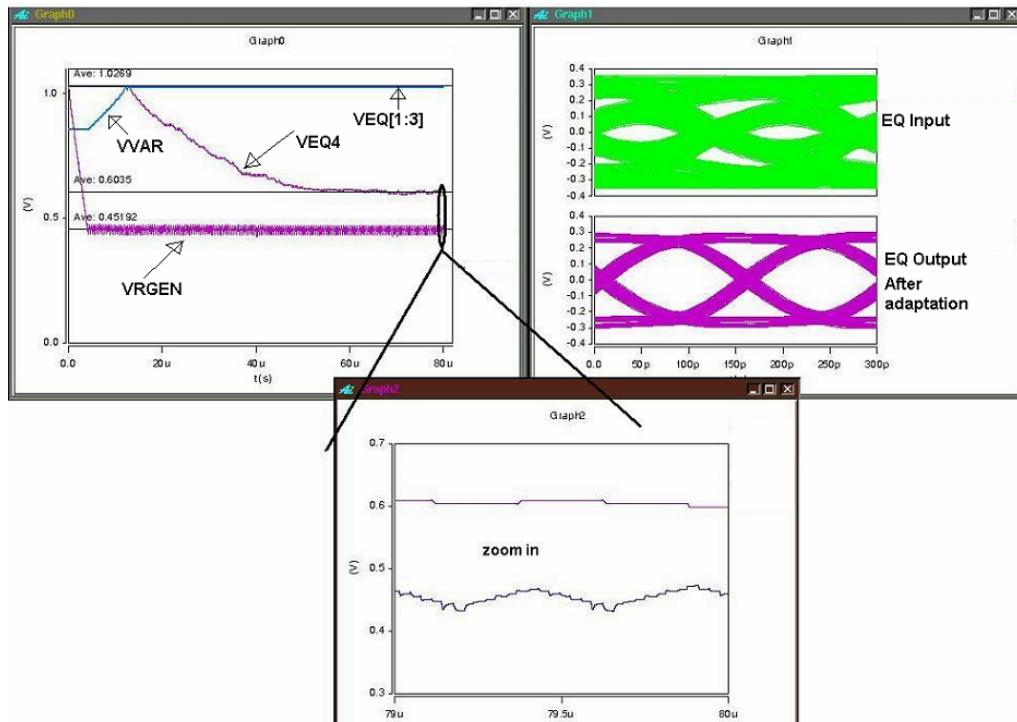


Figure 2. Sample Adaptation Sequence

The state machine allows initial values to be loaded and begin adaptation. In this case, adaptation starts with all stages of equalizer and the RGEN control at maximum boost, while the VVAR control voltage is near minimum. The sequencing of the control voltages, and the values stabilizing at about 60 μ s where a solution is reached, are observed. In this simulation, the low and high frequency loops are running at 32 MHz and 4 MHz, respectively. Alternative algorithms can easily be implemented and tested.

Figure 3 shows a sampling of customer backplanes and illustrates that different slopes need to be supported to allow flexibility.

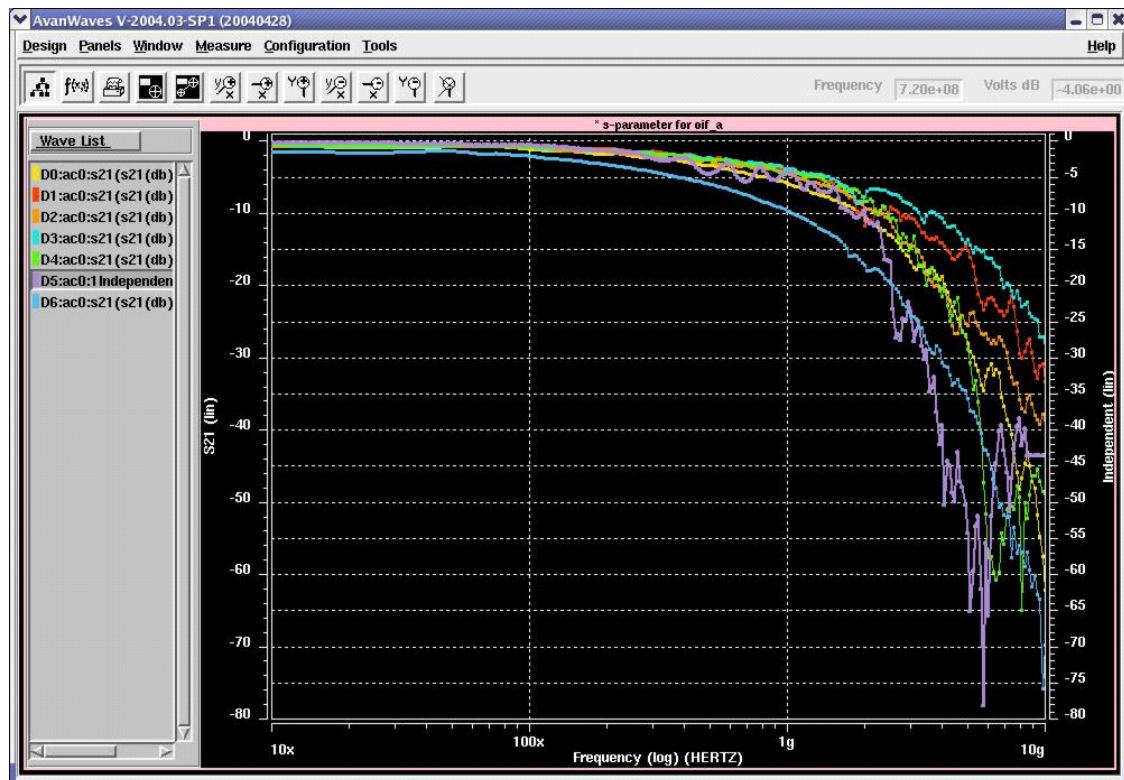


Figure 3. Attenuation Curves for Various Customer Backplanes

Figure 4 shows the attenuation characteristics of the OIF-A backplane. A simple curve fitting shows three poles can roughly fit this backplane at 6-Gbps operation. Operating at 10 Gbps requires four poles for a better fit.

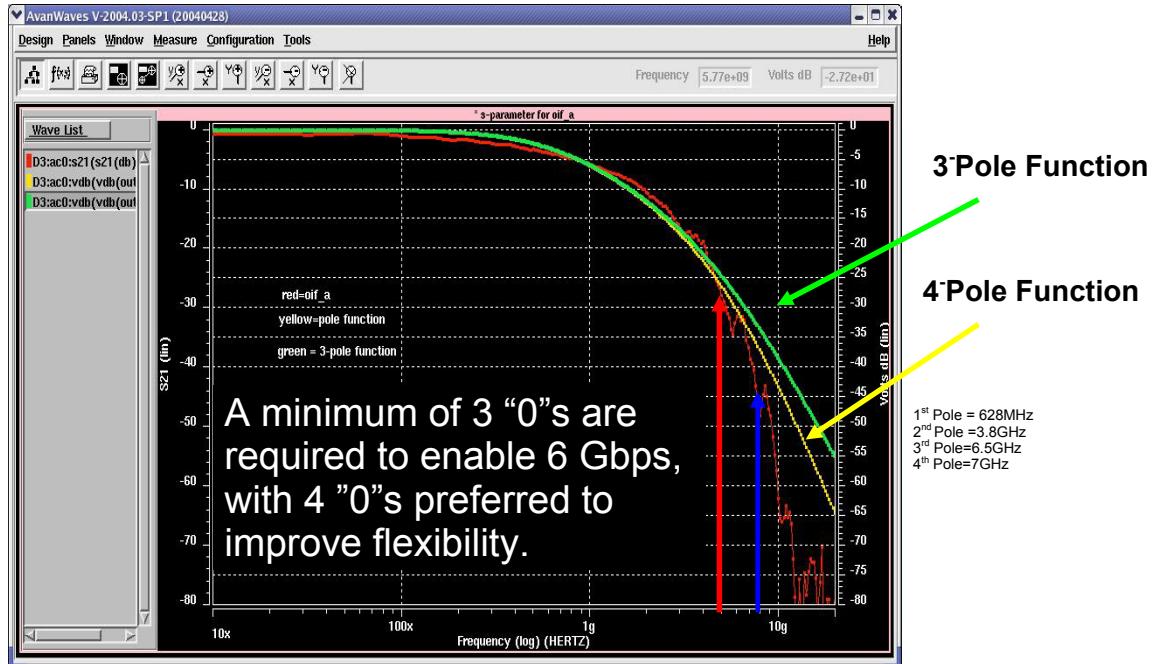


Figure 4. Required Number of Poles to Fit the OIF-A Backplane at 6 Gbps and 10 Gbps

Since each stage contributes one “0”, the ability to sequence the boost in an independent manner allows for better fitting of random backplanes. Figure 3 shows that boosting four stages together only allows a steep slope.

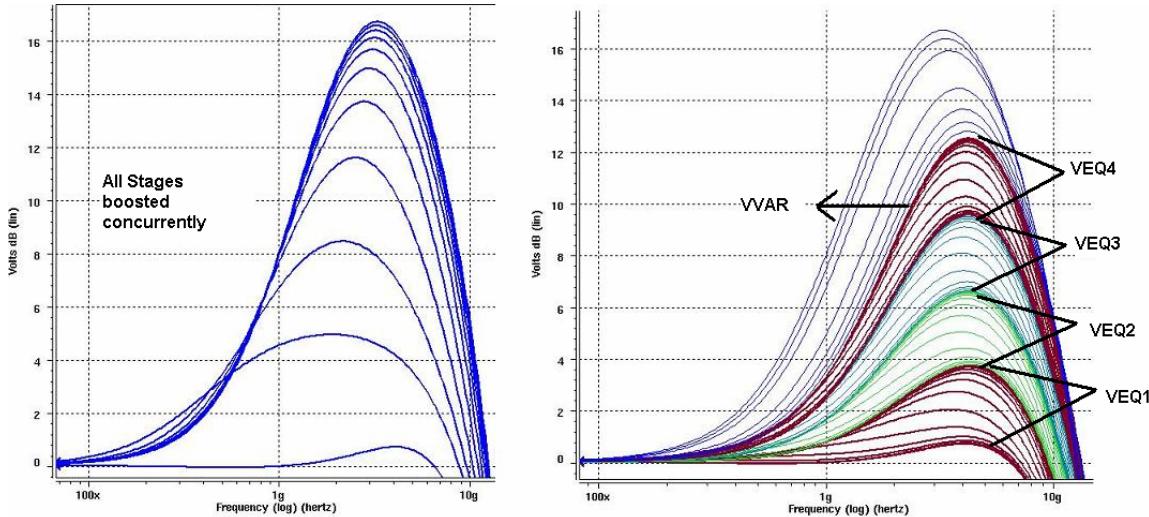


Figure 5. Equalization Curves Showing Difference Between Boosting Stages Individually vs. Sequentially

The right graph shows a different solution space if boosting the stages sequentially is allowed. Stages one through four are boosted sequentially, followed by VVAR. Note the range of available equalization slopes available. VVAR is the varactor boost feeding all four stages. The VVAR control shifts the boost curves to lower frequencies and can be inserted sequentially after boosting any equalizer stage(s).

The state machine allows different permutations of boost sequencing. MATLAB simulations were run on ten different customer backplanes and all possible equalization solution spaces with data rates from 2.5 Gbps to 6.5 Gbps. The results showed that the optimal solution required sequentially boosting each stage for this particular architecture. Most backplanes required more than one stage of boost, which traditional designs support. The digital approach allows support of four stages of equalization or a slope of up to 80 dB of boost per decade. The flexibility of the state machine allows changing the solution space if required.

Several other features are required for flexibility, high performance, and manufacturability. In order to support a wide data range, the corner frequencies of the low and high pass filters should be programmable. Offset cancellation should be provided for the comparators since offset would affect adaptation accuracy. The bandwidth of the RGEN block should also be programmable to avoid over equalization for lower data rates. This is easily accomplished by using programmable resistors in the CML stages.

Figure 6 shows the adaptation results for two different RGEN bandwidths. The over-equalized eye results if a bandwidth designed for 6.5 Gbps operation is used at 3.2 Gbps. Over-equalization may result in increased jitter.

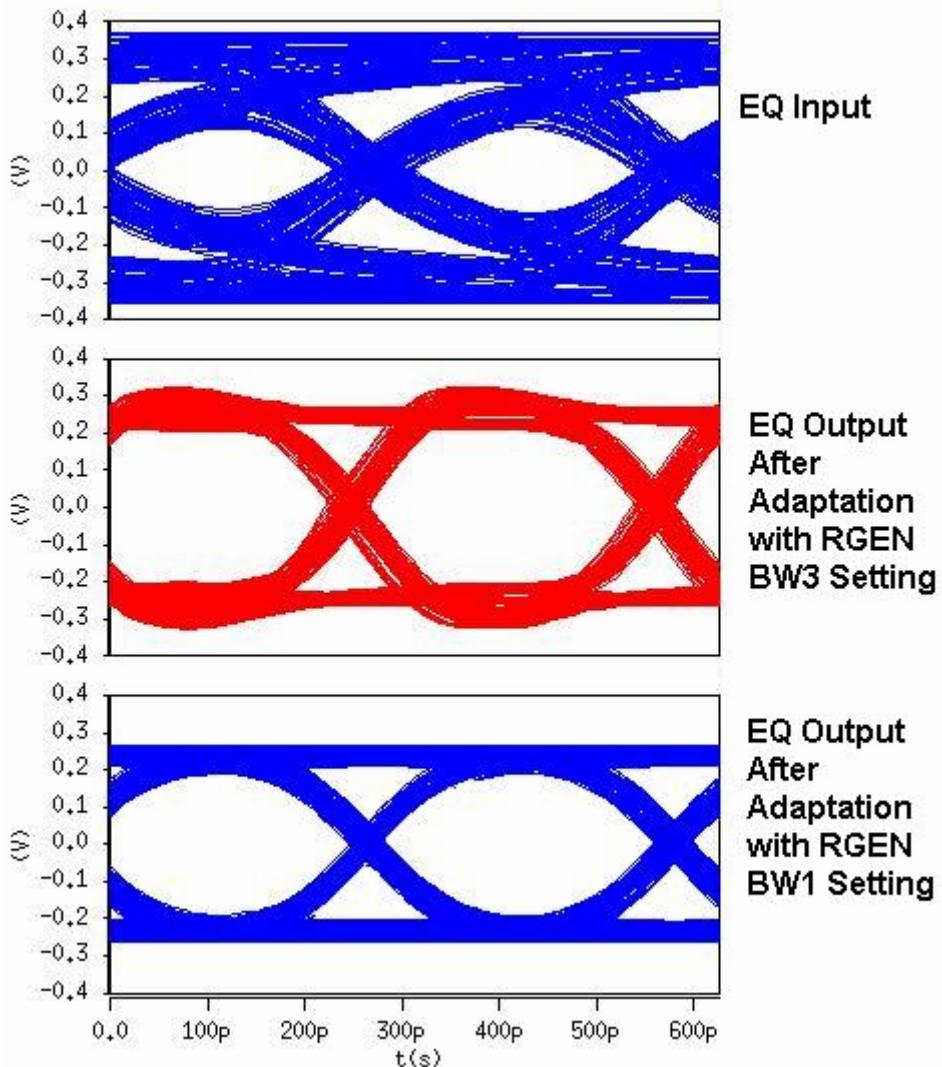


Figure 6. Adaptation at 3.2 Gbps Showing Results With Different RGEN Bandwidth Setting

Figure 7 shows eye diagrams after adaptation at 6.5 Gbps. Several legacy backplanes with completely closed eyes designed for lower data rates were successfully equalized.

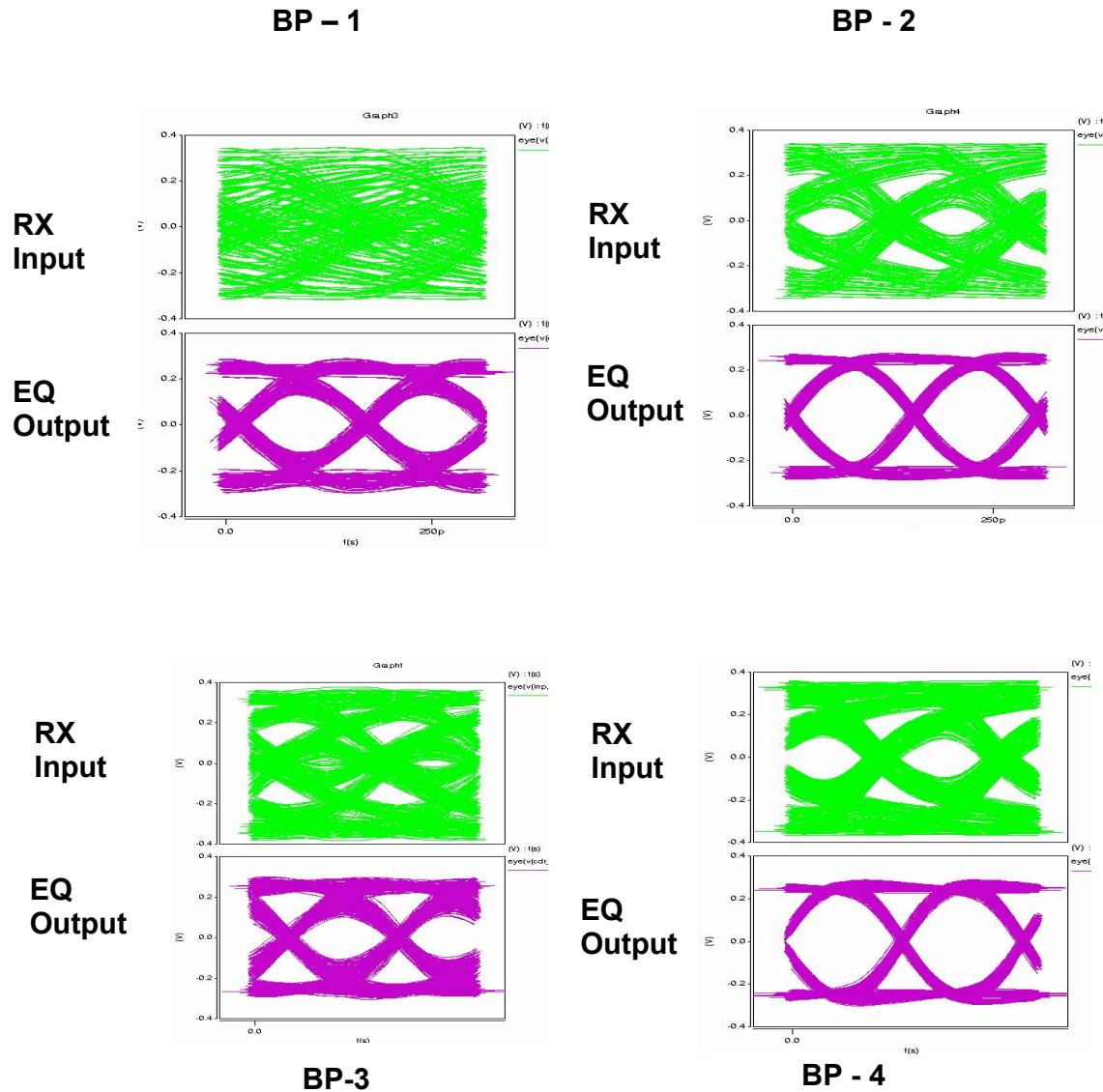


Figure 7. Adaptation Results at 6.5 Gbps for Various Backplanes

Measured Results

Figure 8 shows measured eye diagrams after adaptation at 6.5 Gbps for the FCI board. Two different lengths of trace were measured and the resulting eyes after adaptation are similar.

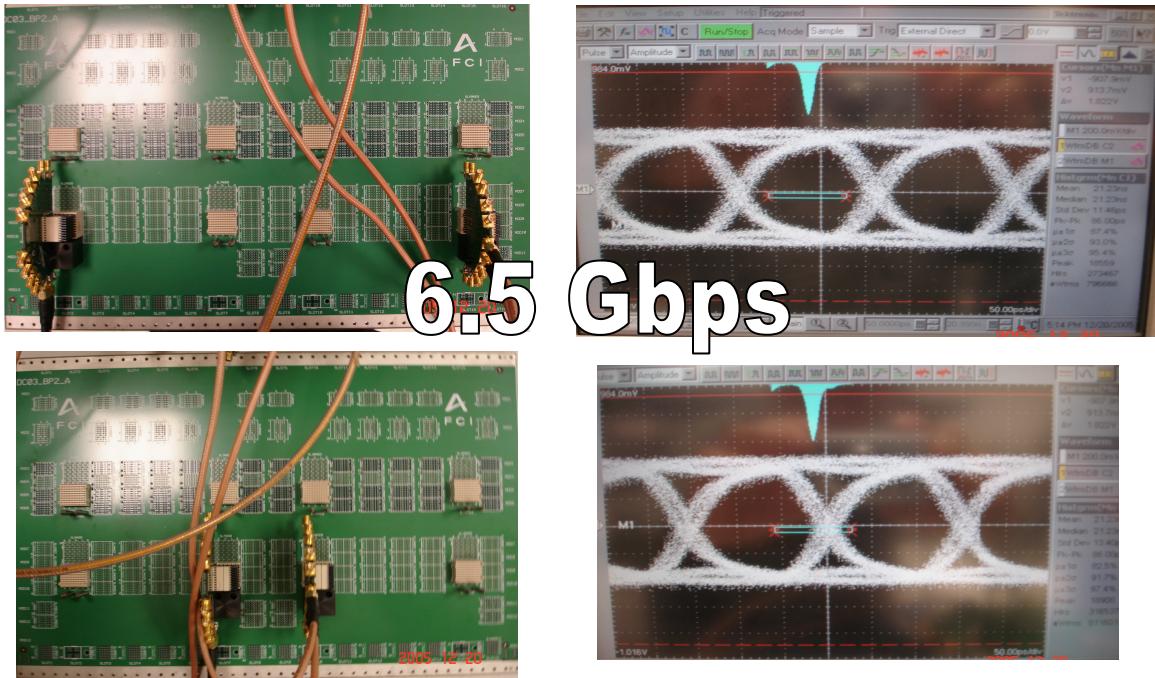


Figure 8. Adapted Eye Diagrams at 6.5 Gbps for FCI Board With Different Lengths of Backplane

Figure 9 shows eye diagrams before and after adaptation for the XAUI legacy backplane at 6.5 Gbps. The eye is almost completely closed before adaptation and open after adaptation.



Figure 9. Adapted Eye Diagrams at 6.5 Gbps for 32" XAUI Legacy Backplane With Two Connectors and Two Daughter Cards

The adaptive equalizer architecture is realized in a 90-nm TGO logic process. It is fully integrated with a wide-range full-duplex transceiver designed to run from 622 Mbps to 6.5 Gbps. Figure 10 shows a plot of the Stratix II GX device that has over 90K logic elements. This chip contains 16 full duplex transceivers supporting data rates from 622 Mbps to 6.5 Gbps. The adaptive equalizer has been verified with over a dozen customer backplanes designed to run from 2.5 Gbps to 6.5 Gbps.

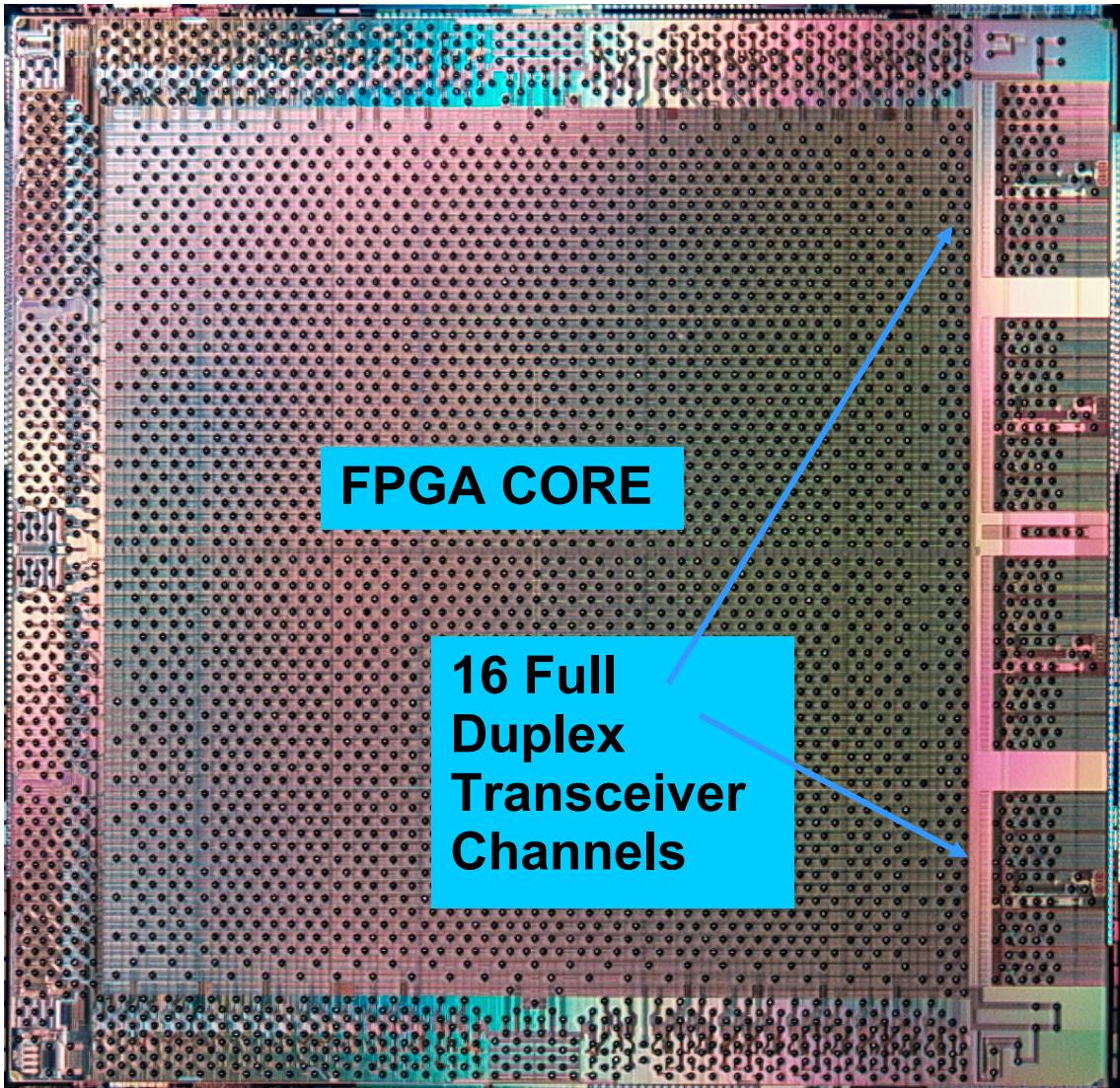


Figure 10. Stratix II GX Chip Plot

Conclusions

This paper has demonstrated a digitally assisted adaptive design integrated on an FPGA. Review of various customer backplanes showed that adaptive designs that only control one “0” are not sufficient. The digital implementation allows the ability to support a wider customer base by allowing the flexibility to change the equalization profile via four stages of equalization and reference corner frequency. The digital state machine allows changing the pole locations as well as the number of poles enabled concurrently. The comparator offset due to random mismatch is also canceled digitally to allow manufacturability. The adaptive block is able to successfully equalize over a dozen backplanes with data rates from 2.5 Gbps to 6.5 Gbps.

Acknowledgments

Authors thank Altera Corporation CAD and Layout Departments.

References

- [1] J.-S. Choi et al., “*A 0.18um CMOS 3.5Gb/s Continuous-Time Adaptive Cable Equalizer Using Enhanced Low-Frequency Gain Control Method*,” IEEE J. Solid-State Circuits, pp. 419-425, March, 2004.
- [2] S. Gondi et al., “*A 10Gb/s CMOS Adaptive Equalizer for Backplane Applications*,” ISSCC 2005, session 18.1.



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