Name: Pranjal Verma, B. Tech (EE), IC-ResQ Lab.

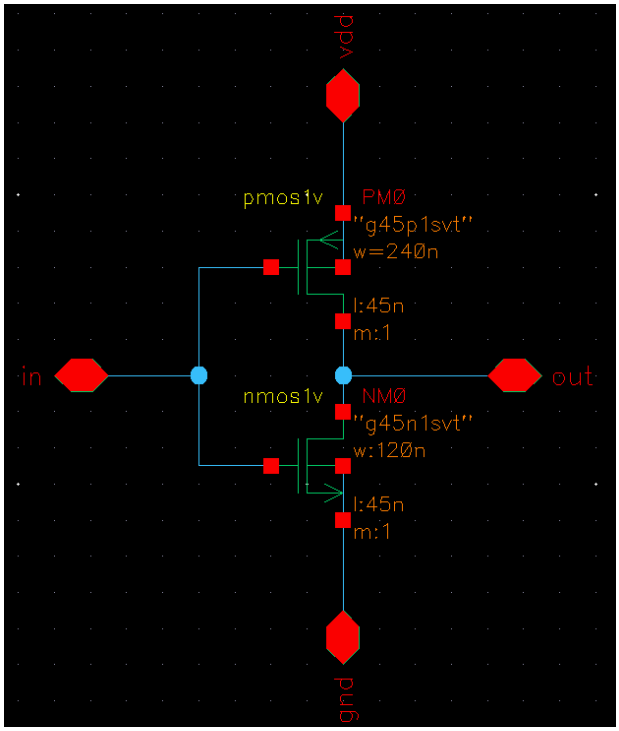
Work Completed –

1. Schematic to GDS-II: (complete flow)

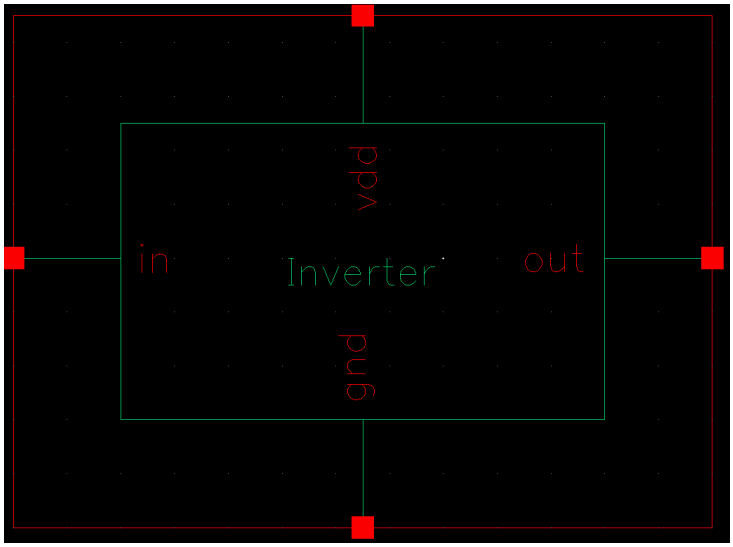
- Schematic of Inverter
- Symbol
- Testbench
- Pre-simulation – Dynamic power, Leakage power and Transient response.
- Layout
- DRC
- LVS
- QRC
- Post Layout Simulation
- Pad Frame (Schematic, Layout and DRC)
- Stream-out GDS -II

Inverter

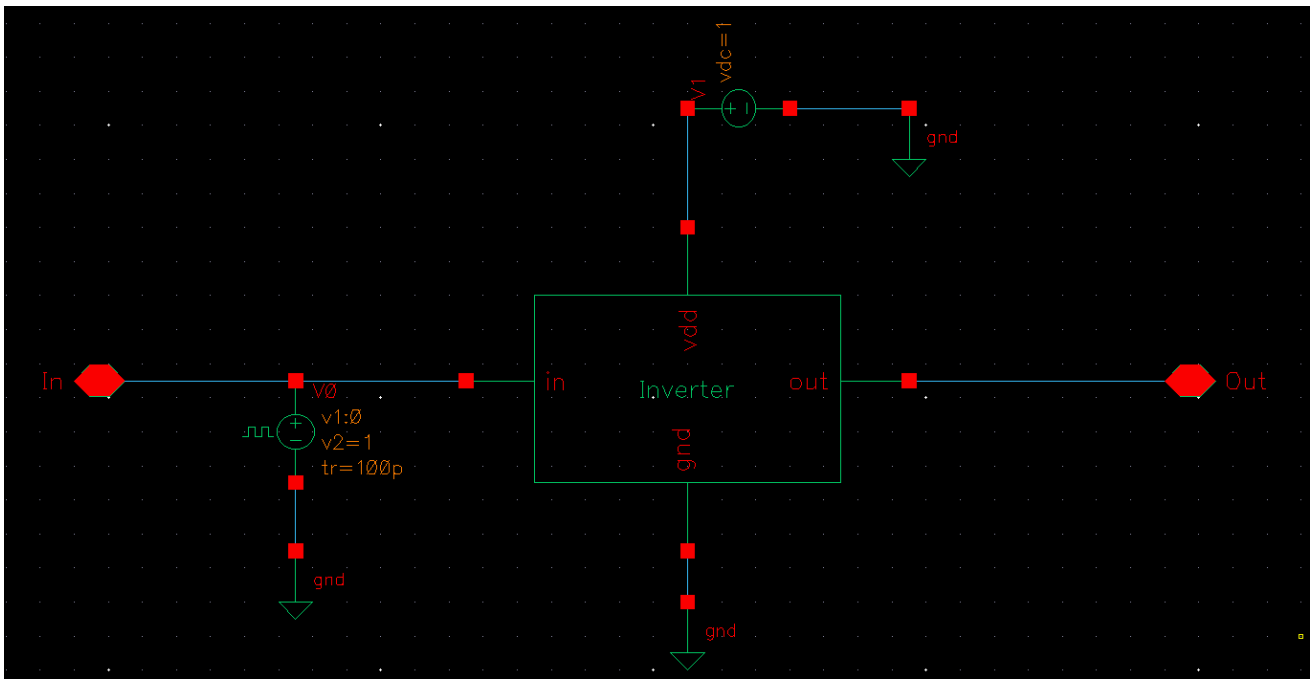
Schematic



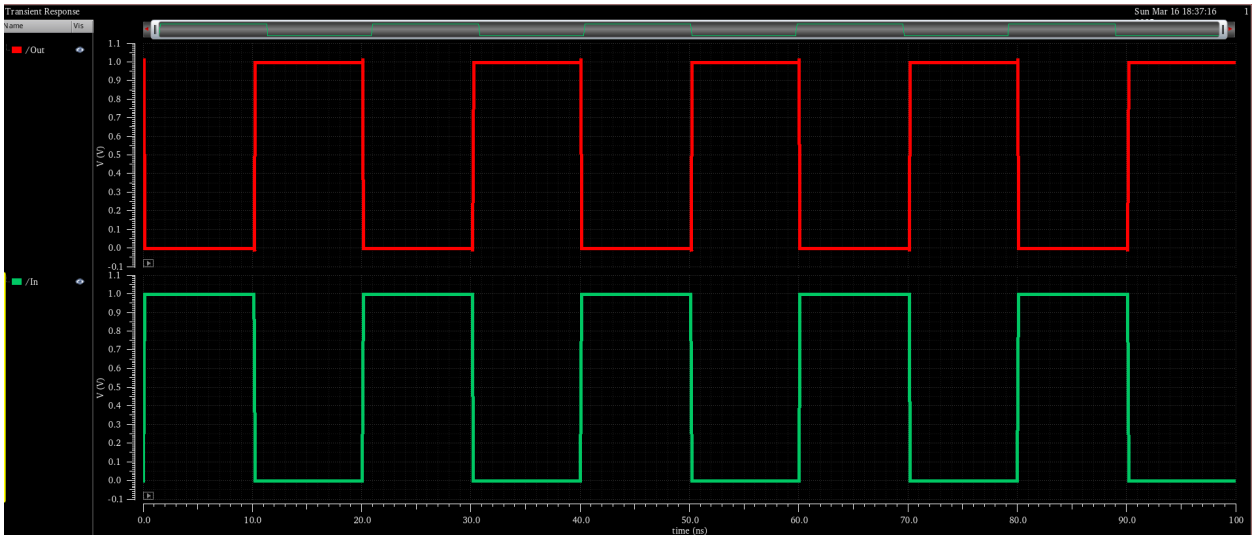
Symbol



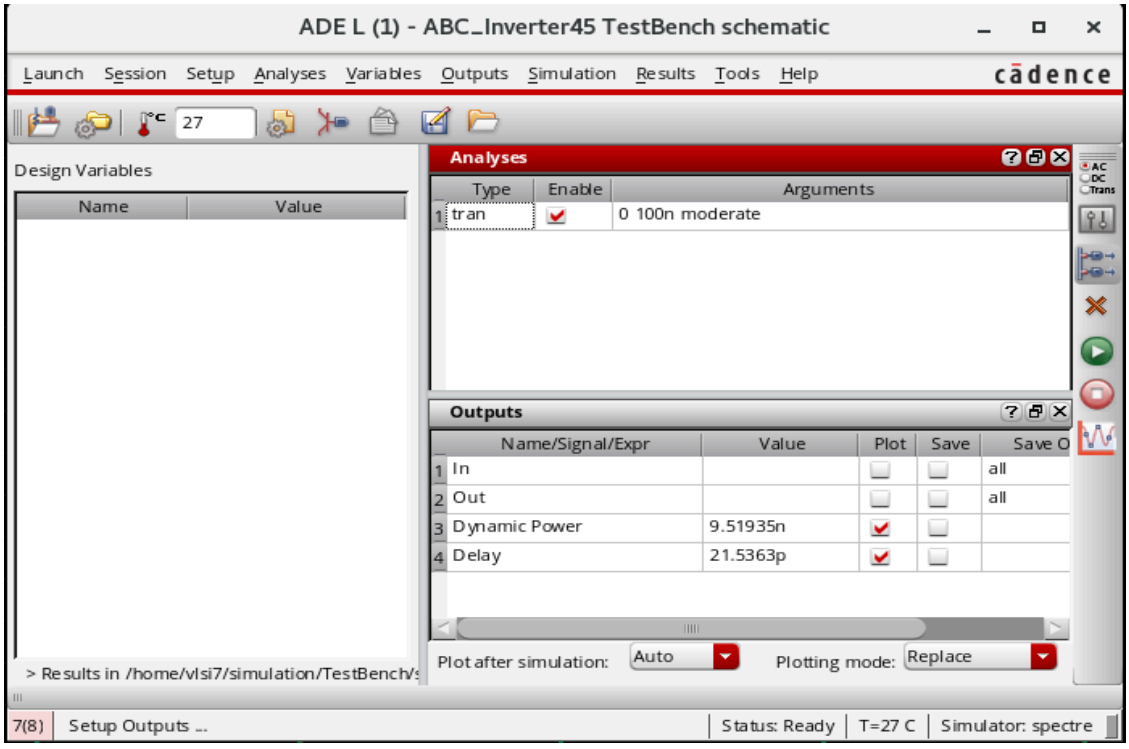
Testbench:



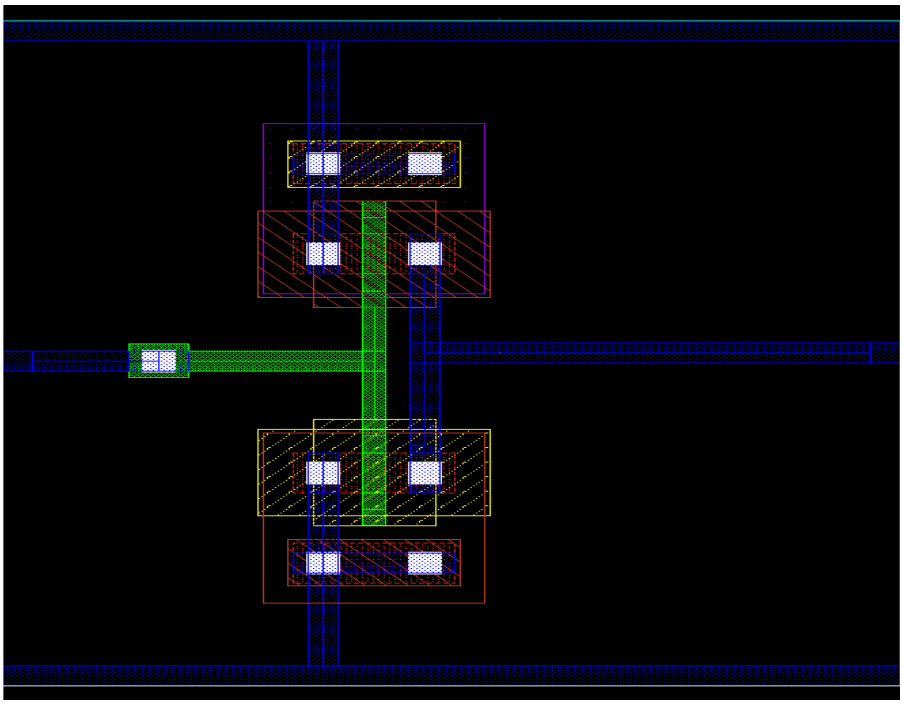
Transient Response:



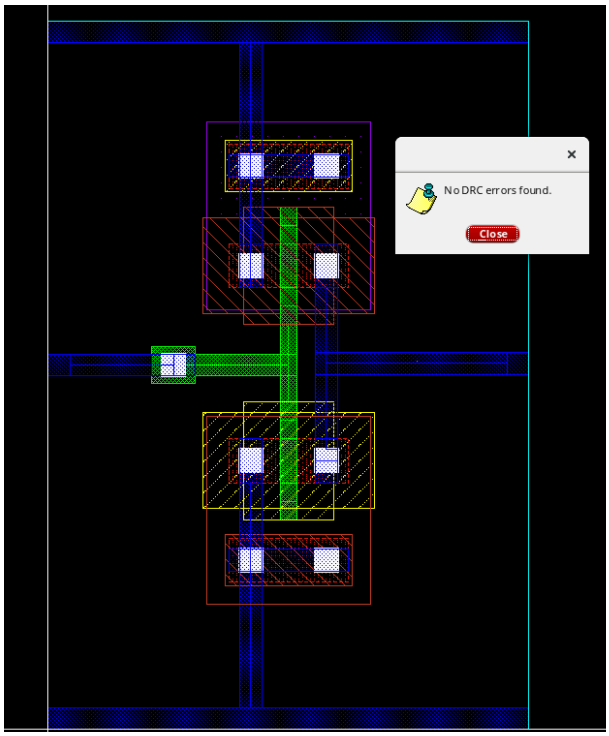
Dynamic power and propagation:



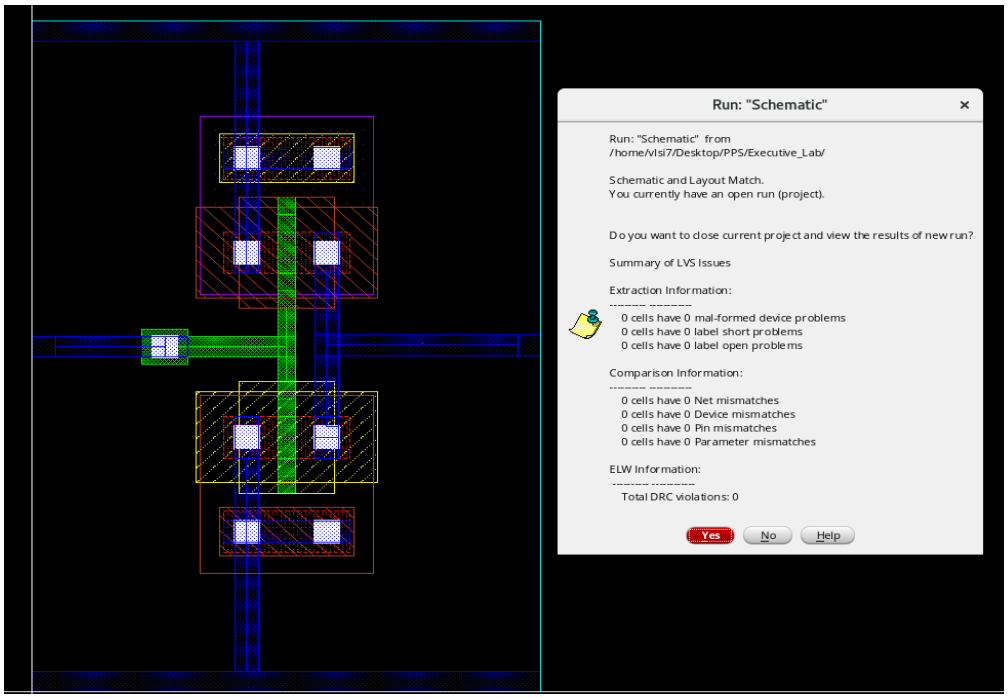
Layout :



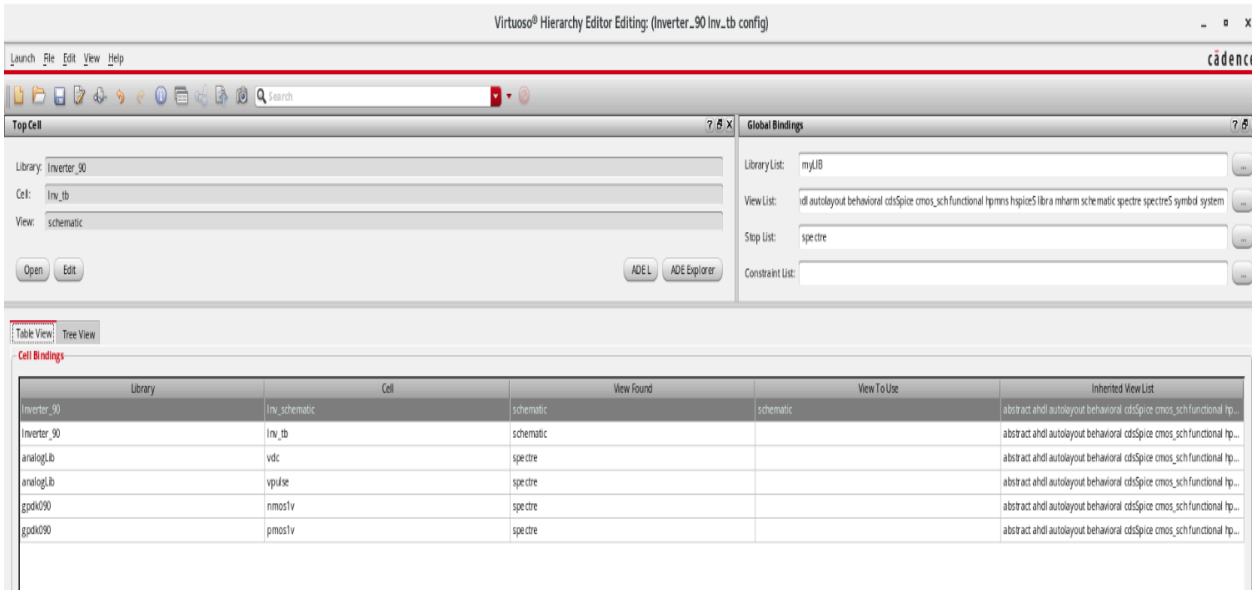
DRC :


No DRC errors found.
Close

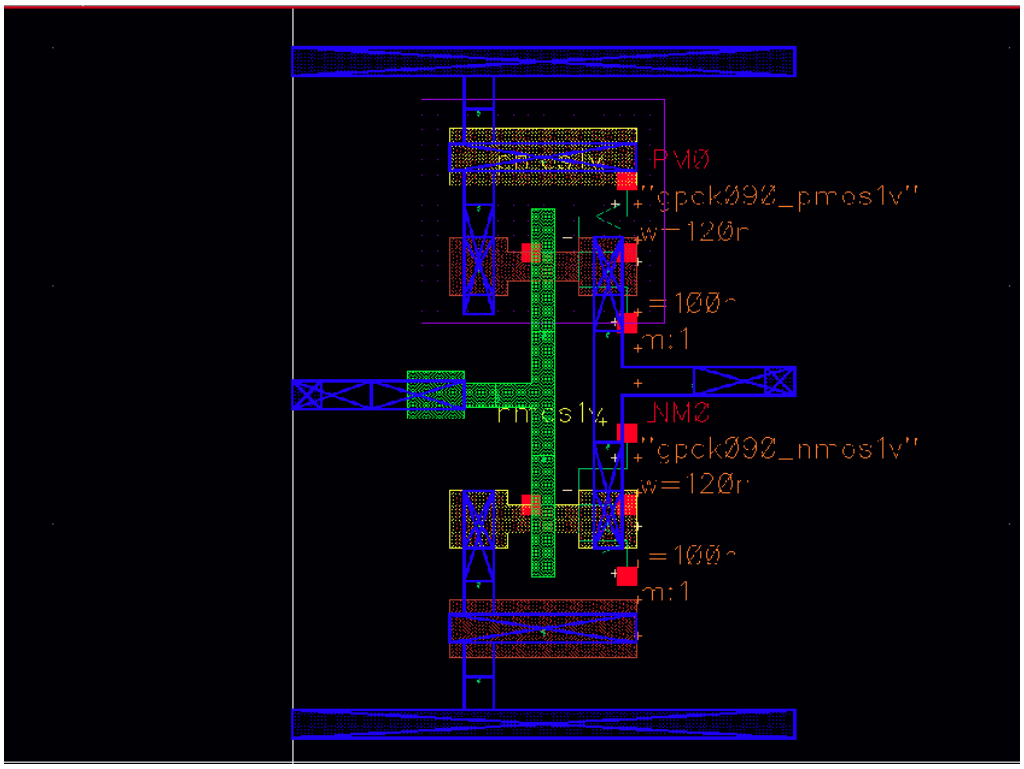
LVS:


Run: "Schematic"
Run: "Schematic" from
/home/vlsi7/Desktop/PPS/Executive_Lab/
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help

QRC:



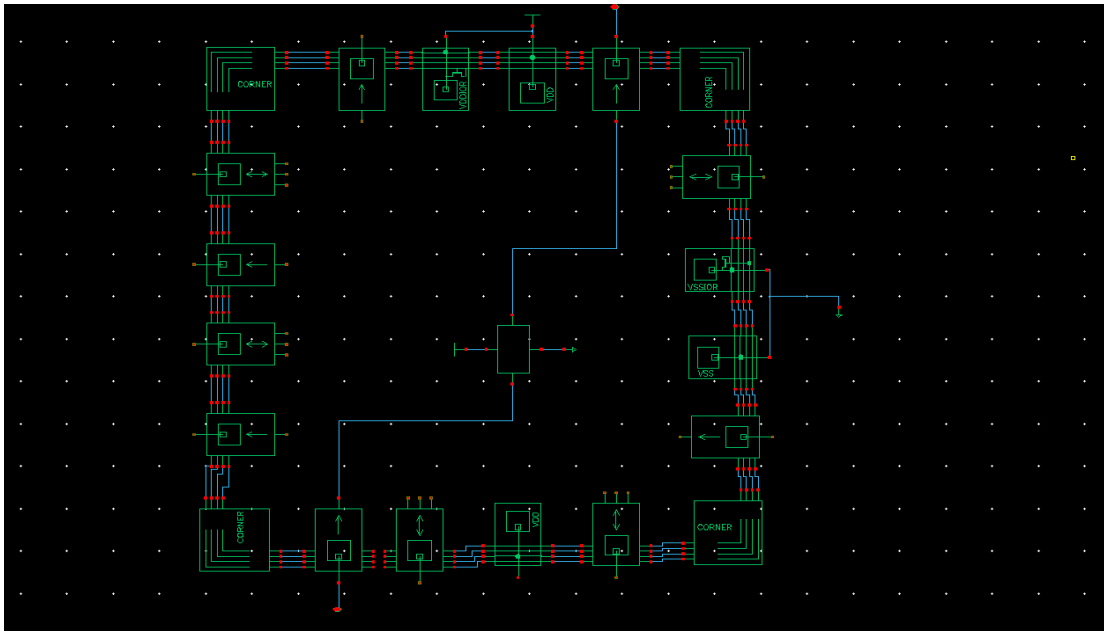
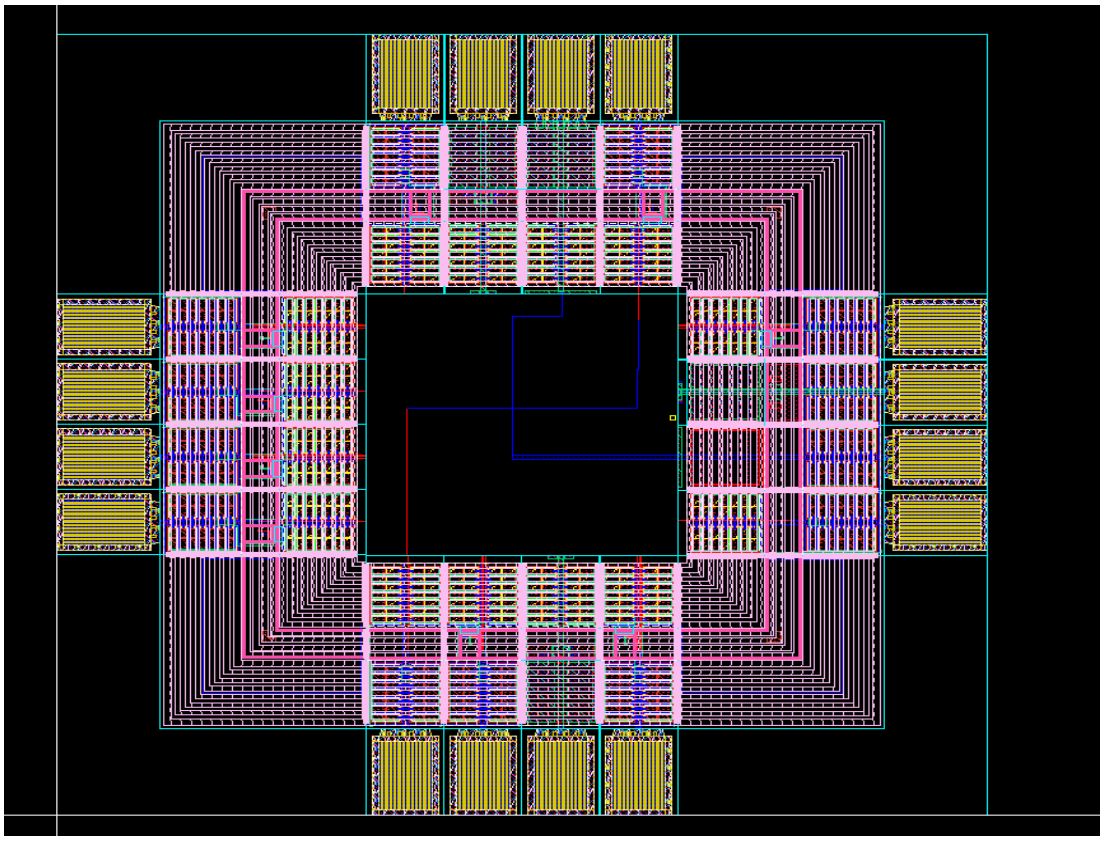
AV-extracted view -



Post Layout Simulation:

Pad Frame :

Schematic :



Layout: