IIIT BANGALORE

VLS 502

Analog CMOS VLSI Design

Project Report

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Submitted To:-

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VL502: Analog IC Design, 2024-2025 Final Project
Externally Compensated LDO Design

1. Specifications

Design: The specifications used in our design are as follows.

Table 1: Specifications Summary

Parameter	Value
Input voltage	1.4V
Output Voltage	1V
PSRR @ Heavy Load	60dB
Iload, min	2mA
Iload,Max	10mA
Cload	10uF
Iq	50uA

2. Purpose of an LDO

- **Voltage Regulation:** Provides a stable and precise output voltage despite variations in input voltage and varying load conditions..
- **Low Dropout Voltage:** Operates efficiently even when the supply is close to the output voltage.
- **Power Supply Rejection:** Filters out variations from the power supply, ensuring clean power delivery to the circuit.
- **Frequency Compensation:** Improves Stability of the design by making sure that the Phase Margin is greater than 45 degree.

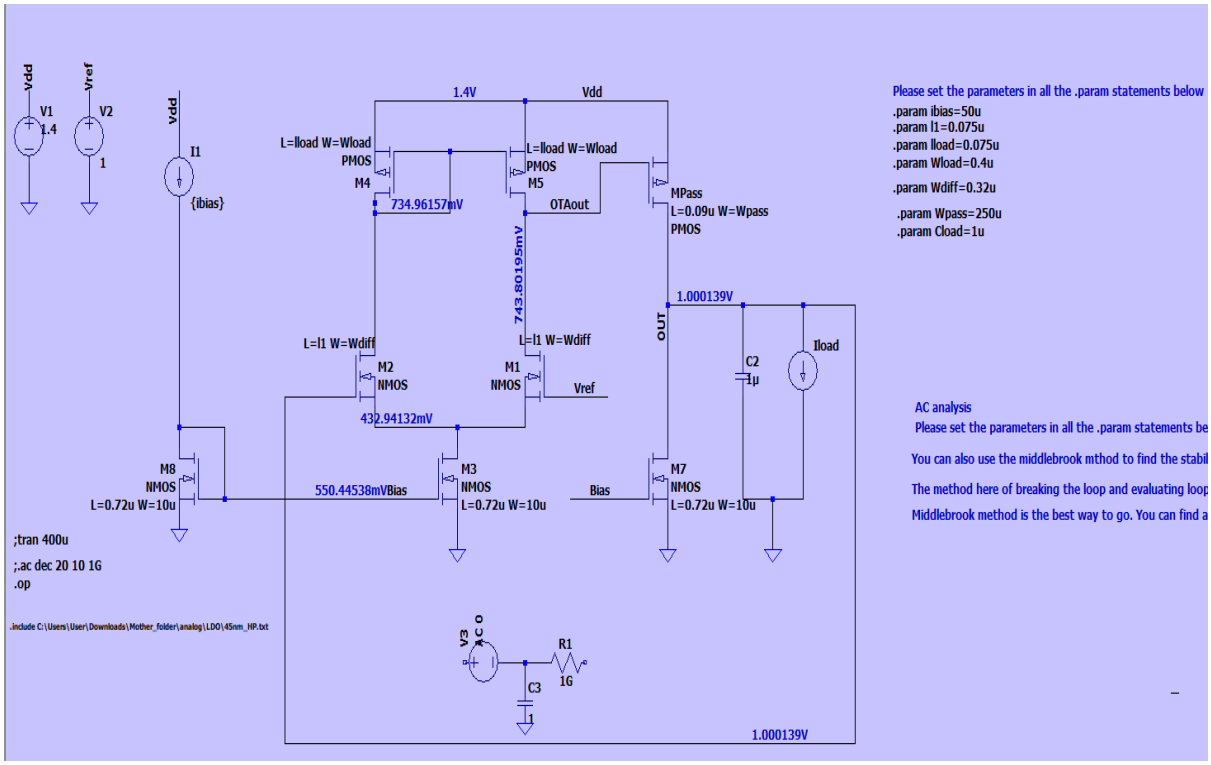

Figure 1: Our LDO schematic

Table 2: Sizing of the Transistors

Transistor Type	**Length**	**Width**
PMOS Pass FET	90nm	250µm
Diff-Amp PMOS Load	75nm	400nm
Diff-Amp Input Pair	75nm	320nm
NMOS for current mirror	720nm	10µm

3. Relevance of Techplots

- GitHub link to our tech plots for our chosen technology node of 45 nm - GitHub Repository.
- Takeaway1: f_T improves with shorter channel lengths, making circuits faster with scaling.
- Takeaway2: Compared to 180 nm, the FOMs here are $g_m r_o$ values are low for the same values of g_m/I_d , f_t values are higher, and I_d/w values are also higher.
- Takeaway3: We chose the Vds to be 400 mV, and we expect that to result in some error because all the transistors might not have Vds drop across them as 400 mV.It is very possible that the Vds across the MOSFETs can change under different values of load current.
- Takeaway4: The I_d/w values tend to saturate as we move towards Sub-Threshold region of operation .

- Takeaway5: Square-law models, though widely used in analog circuit design, are approximations that fail to capture short-channel effects, velocity saturation, and other high-field phenomena critical in deep-submicron processes like 45nm. This often leads to discrepancies between design intent and silicon performance.Techplots bridge this gap by deriving model-independent transistor parameters directly from simulation data.

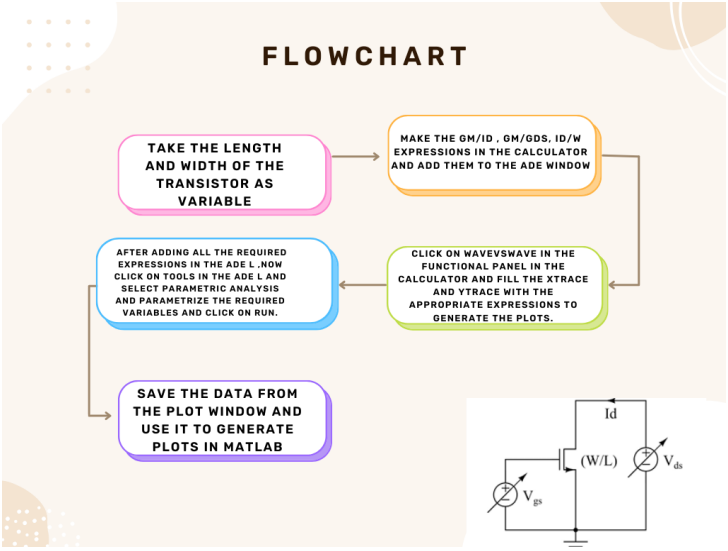

Figure 2: Schematic for generating techplots.

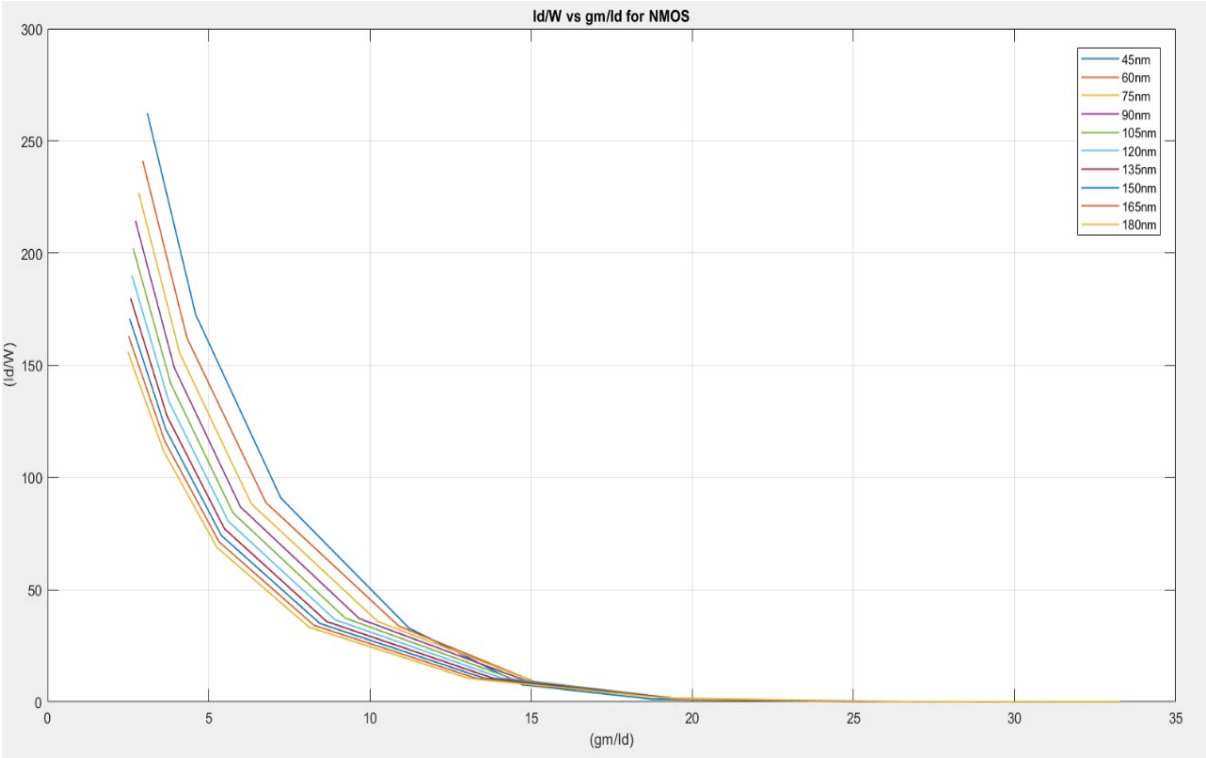

Figure 3: NMOS Techplots after Matlab postprocessing - Id/W

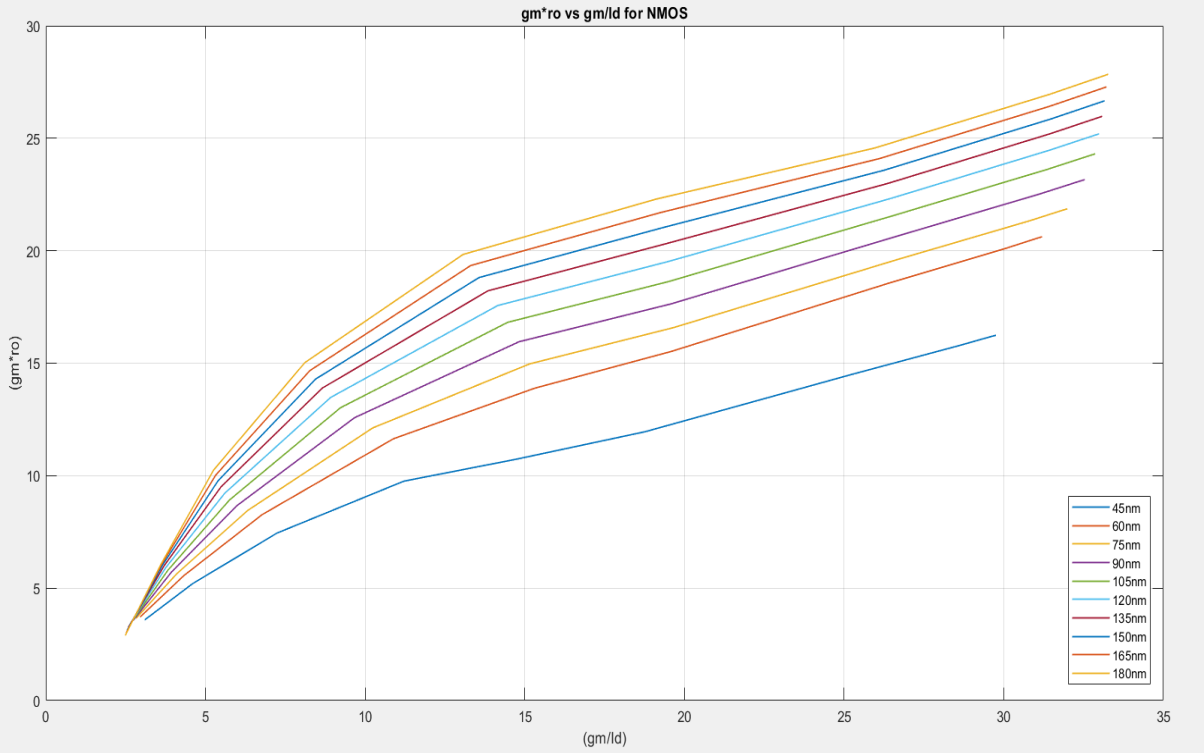

Figure 4: NMOS Techplots after Matlab postprocessing - gmro

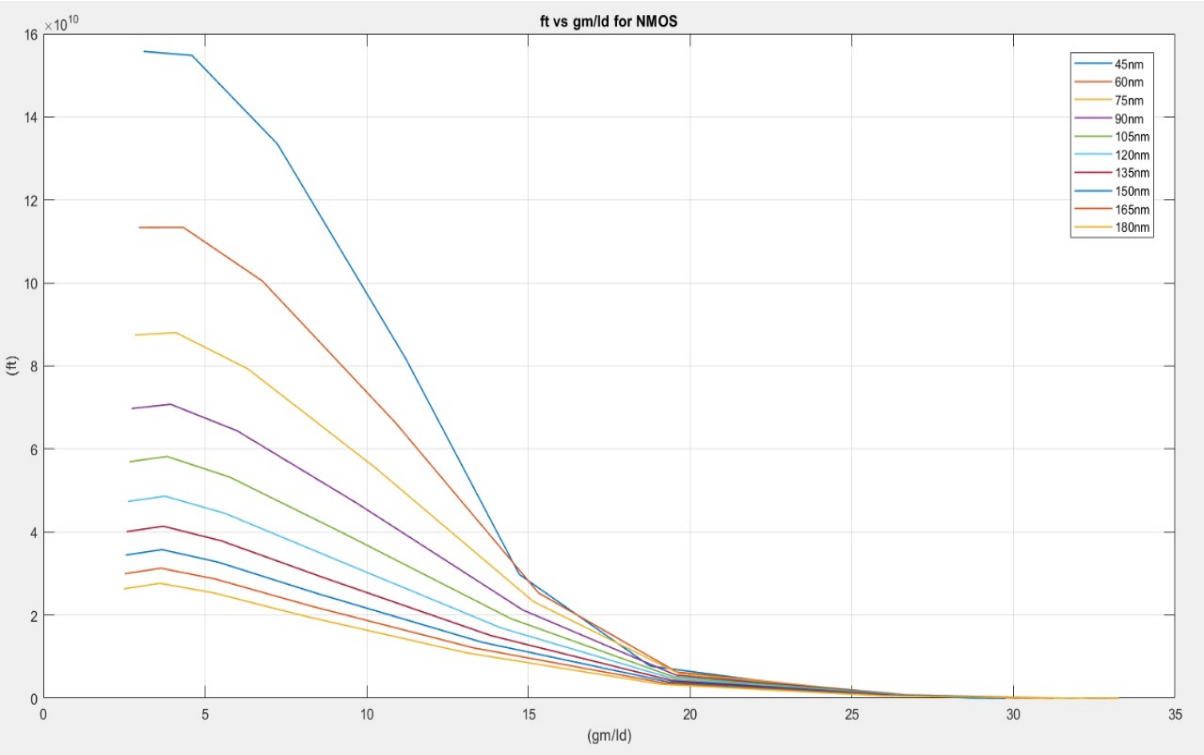

Figure 5: NMOS Techplots after Matlab postprocessing - fT

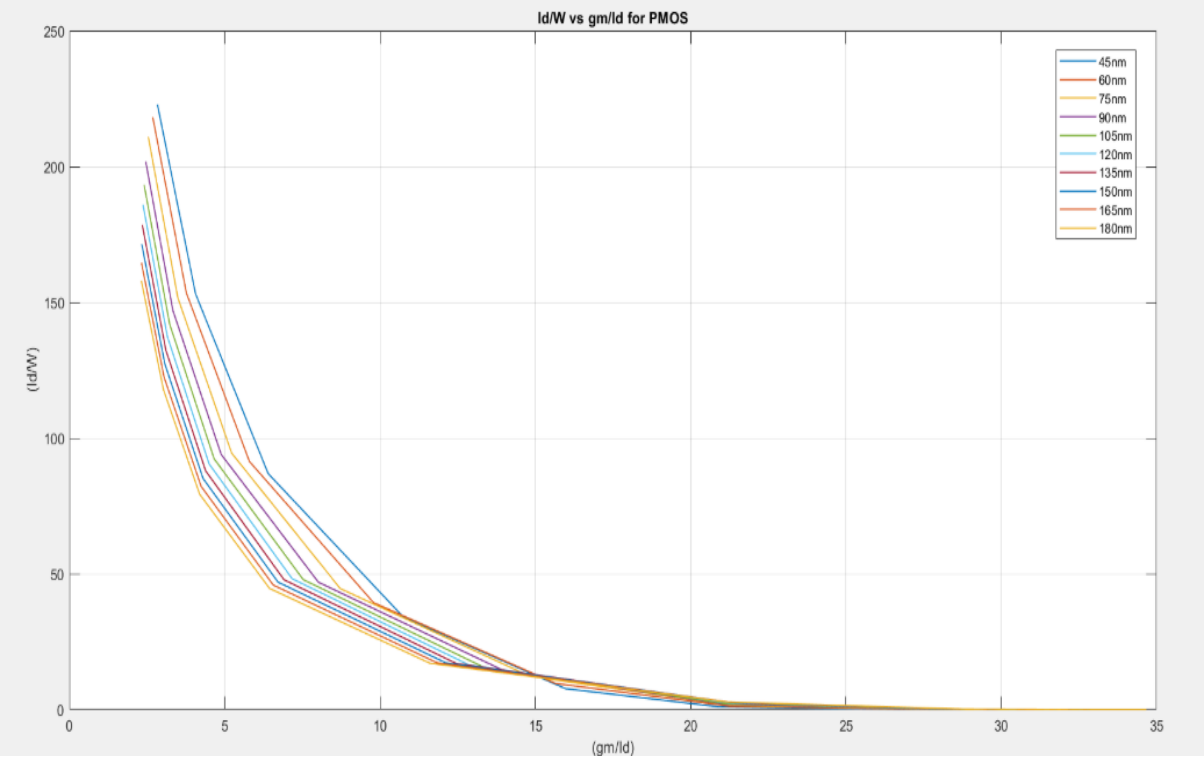

Figure 6: PMOS Techplots after Matlab postprocessing - Id/W

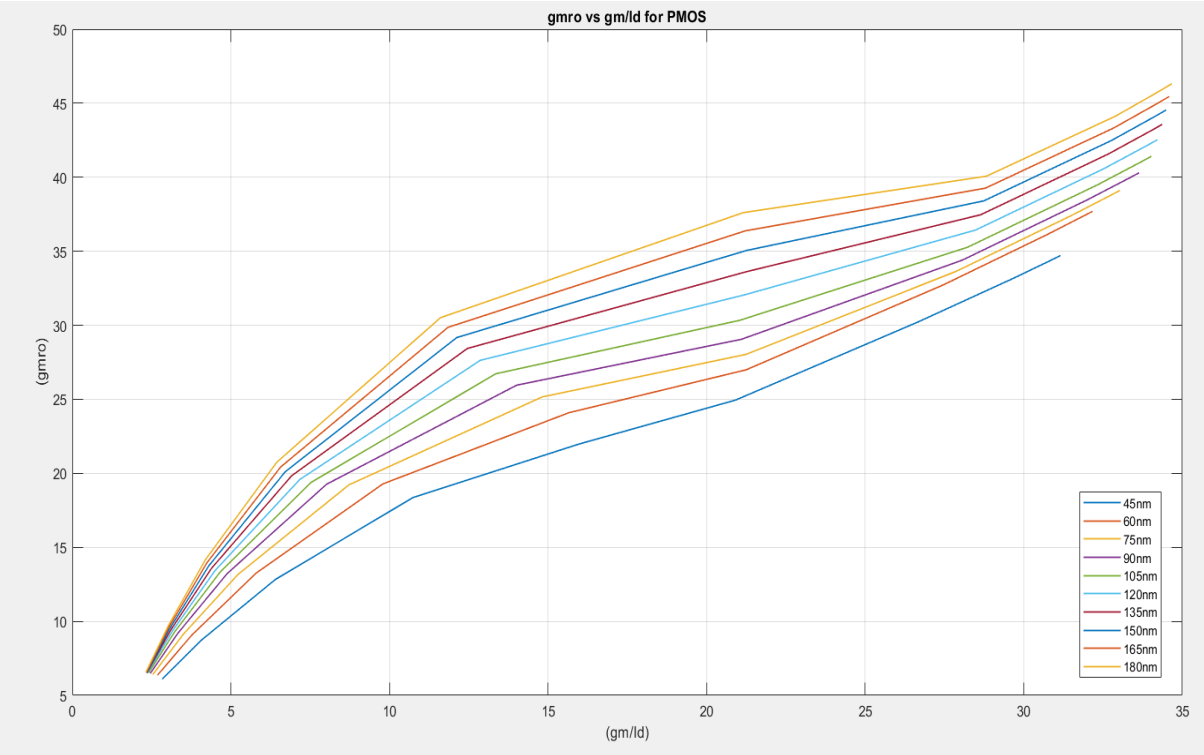

Figure 7: PMOS Techplots after Matlab postprocessing - gmro

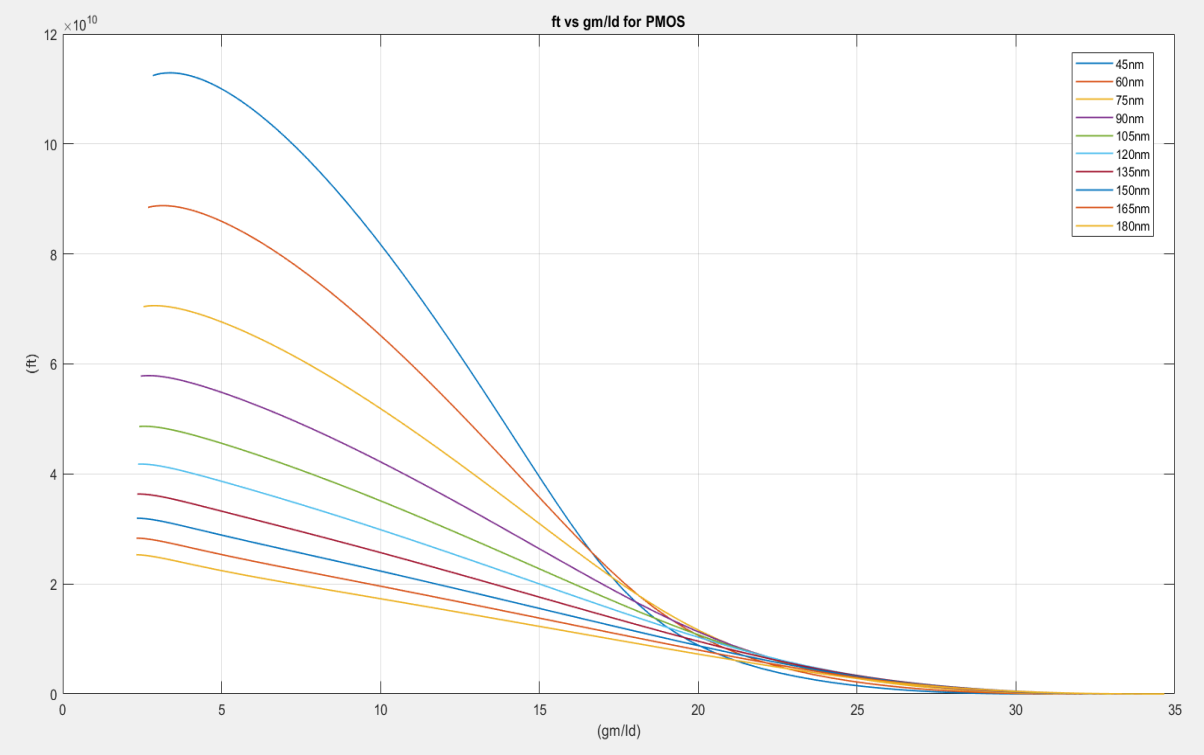

Figure 8: PMOS Techplots after Matlab postprocessing - fT

4. FET Sizes

Theory: By sizing the Transistors we can bias them to operate in saturation region. Below are the sizes for our transistors that are used in this particular design and from DC Operating point analysis we can see that all of them operates in saturation region.

Table 3: Sizing of the Transistors

Transistor Type	Length	Width
PMOS Pass FET	90nm	250µm
Diff-Amp PMOS Load	75nm	400nm
Diff-Amp Input Pair	75nm	320nm
NMOS for current mirror	720nm	10µm

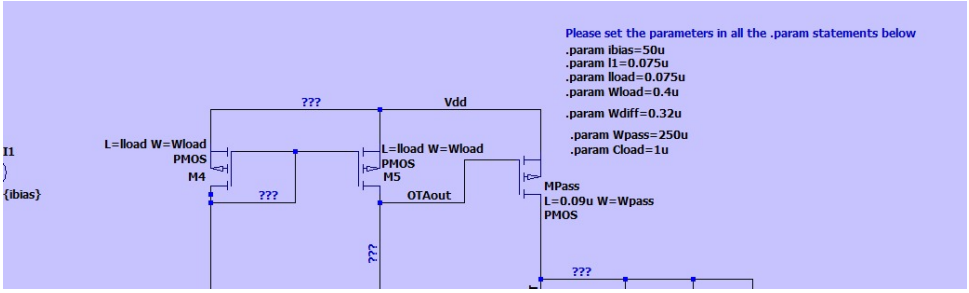

Figure 9: Pass FET and PMOS Load Sizing.

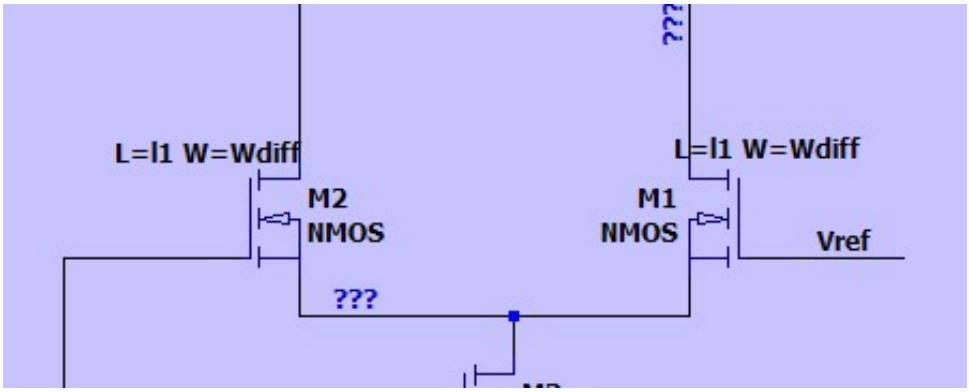

Figure 10: NMOS Input Pair Sizing.

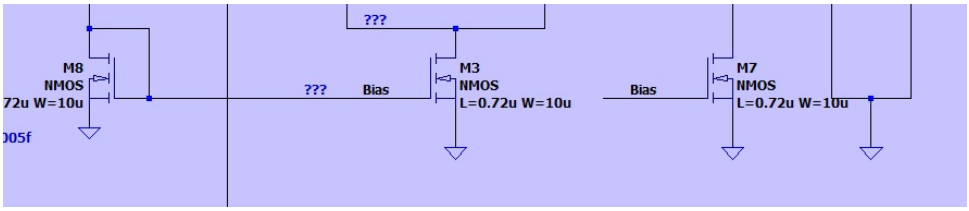

Figure 11: Current Mirror Sizing.

SPICE Output Log: C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo.asc
Start Time: Fri Dec  6 12:34:20 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
WARNING: Node NC_02 is floating.

WARNING: Less than two connections to node nc_01.  This node is used by v3.
WARNING: Less than two connections to node nc_02.  This node is used by r1.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:       m1          m2          m3          m7          m8
Model:    nmos        nmos        nmos        nmos        nmos
Id:     2.49e-05    2.49e-05    4.98e-05    5.07e-05    5.00e-05
Vgs:    5.67e-01    5.67e-01    5.50e-01    5.50e-01    5.50e-01
Vds:    3.11e-01    3.02e-01    4.33e-01    1.00e+00    5.50e-01
Vbs:    0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:    4.64e-01    4.64e-01    4.69e-01    4.69e-01    4.69e-01
Vdsat:  1.20e-01    1.20e-01    1.15e-01    1.15e-01    1.15e-01
Gm:     2.81e-04    2.81e-04    7.01e-04    7.13e-04    7.04e-04
Gds:    8.30e-06    8.45e-06    2.03e-06    1.61e-06    1.80e-06
Gmb     6.39e-05    6.38e-05    1.59e-04    1.62e-04    1.60e-04
Cbd:    1.46e-16    1.47e-16    4.44e-15    3.98e-15    4.33e-15
Cbs:    2.56e-16    2.56e-16    8.00e-15    8.00e-15    8.00e-15

Name:       m4          m5          mpass
Model:    pmos        pmos        pmos
Id:    -2.49e-05   -2.48e-05   -1.01e-02
Vgs:   -6.65e-01   -6.65e-01   -6.56e-01
Vds:   -6.65e-01   -6.56e-01   -4.00e-01
Vbs:    0.00e+00    0.00e+00    0.00e+00
Vth:   -4.78e-01   -4.78e-01   -4.87e-01
Vdsat: -1.95e-01   -1.95e-01   -1.83e-01
Gm:     2.14e-04    2.14e-04    9.58e-02
Gds:    6.91e-06    6.91e-06    2.44e-03
Gmb     4.59e-05    4.58e-05    2.03e-02
Cbd:    1.69e-16    1.69e-16    1.12e-13
Cbs:    3.20e-16    3.20e-16    2.00e-13

Total elapsed time: 0.062 seconds.
```

Figure 12: DC Biasing and Proof that all transistors are in saturation.

5. Stability Analysis

Theory: As load increases in externally compensated LDOs, the dominant pole moves away from the origin, while the nondominant pole stays fixed. This reduces the gap between unity gain frequency and nondominant pole at higher load currents, compromising stability.

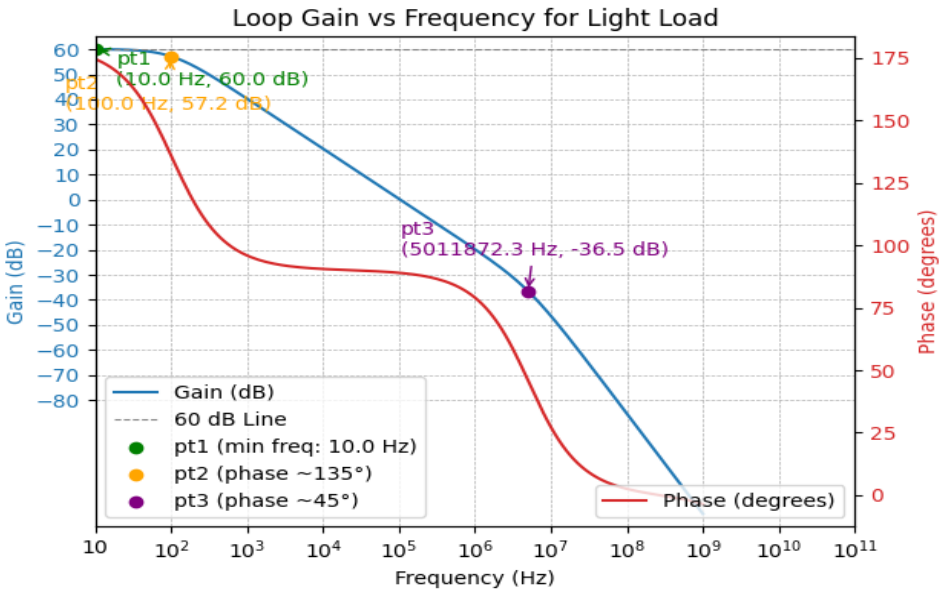

Figure 13: Python Plot.

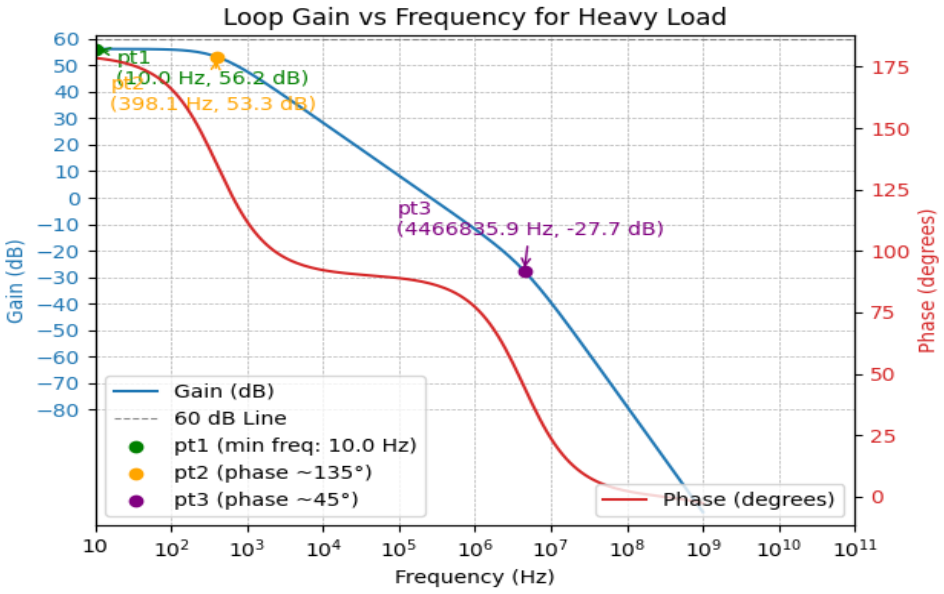

Figure 14: Python Plot.

Table 4: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	56.22db	60.001db
Unity Gain Bandwidth (Hz)	266.39kHz	100kHz
Phase Margin (degrees)	86.6 degree	88.94 degree
Pole 1 (Hz)	405Hz	103Hz
Pole 2 (Hz)	4.41MHz	5.14MHz

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at it's output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as PSRR = 20log(vout/vin), where vout and vin refer to magnitudes of input and output ripples.

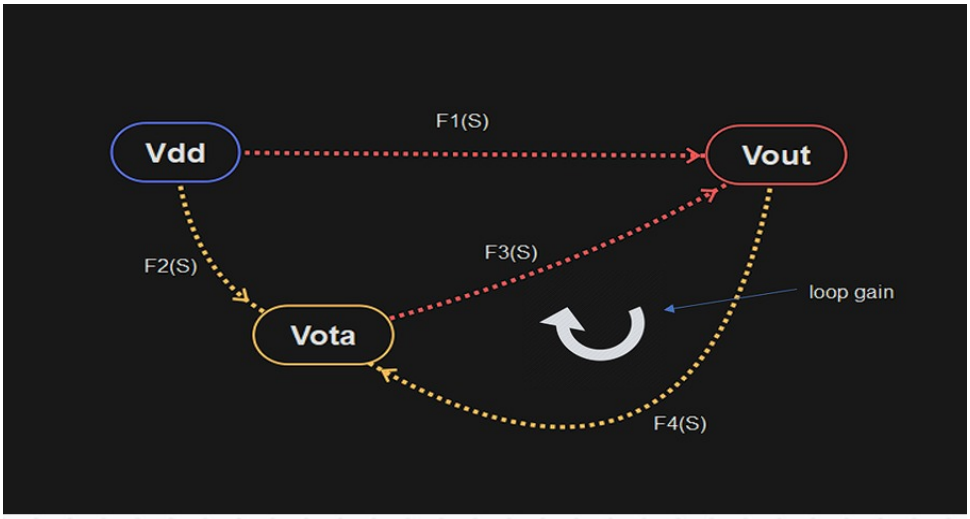

Figure 15: Signal flow graph for PSRR calculation.

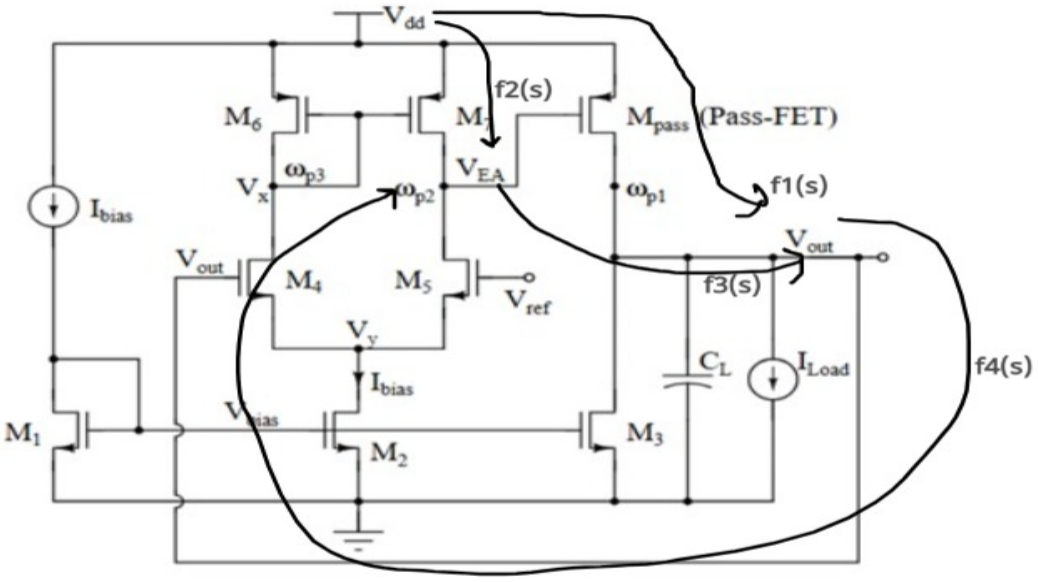

Figure 16: PSRR analysis paths of an LDO.

7. PSRR Simulation Results

We have designed three schematics in LTSpice to evaluate three different conditions. A simulation artifact has been created to analyze these conditions.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Case 1:- Loop gain analysis

Explanation of the artifact used:-

To calculate the loop gain, an RC circuit is placed in the feedback loop along with an AC source of 1V amplitude. This ensures that the AC voltage at the output remains constant at 1V. Additionally, the circuit requires biasing, particularly for the gate of the NMOS in the differential amplifier. To achieve this, a DC voltage is applied to the gate while the RC circuit prevents DC current from flowing to ground, yet directs high-frequency AC signals to ground.

The RC circuit is designed with a high resistance to ensure minimal voltage drop across the resistor, as the current flowing into the MOSFET gate is nearly zero. This configuration allows for effective biasing of the circuit while enabling loop gain calculation without interfering with the DC operating point.

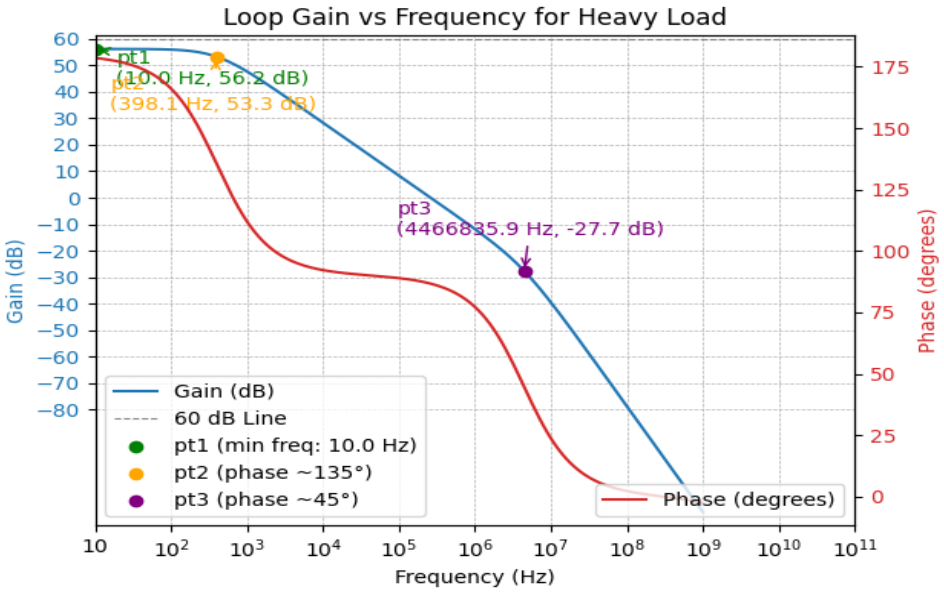

Figure 17: PSRR simulation results - heavy load.

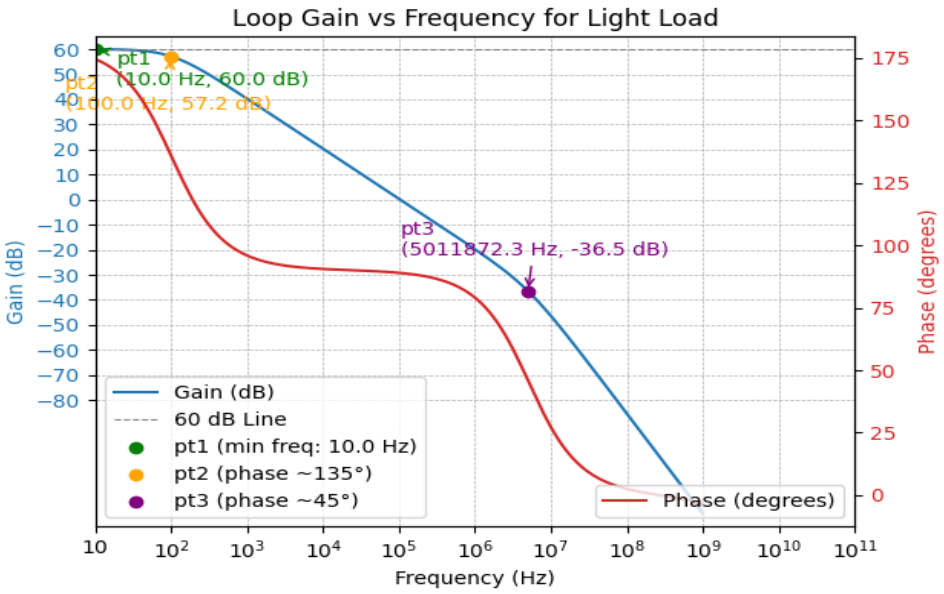

Figure 18: PSRR simulation results - light load.

Case 2:- Open Loop PSRR calculation

Explanation of the artifact used:-

The open loop PSRR measurement involves applying an AC signal (amplitude = 1) to VDD, which connects to both the pass FET source and differential amplifier PMOS source.

The differential amplifier is biased using an RC circuit, with AC 0 indicating the open loop condition. Since there's no feedback path in this configuration, noise rejection is poor and significant noise appears at the output - this is expected for open loop PSRR measurement.

The ultimate goal is that when the circuit is closed with feedback, this noise getting through the differential amplifier will enable proper noise rejection at the final LDO output, producing a clean DC voltage.

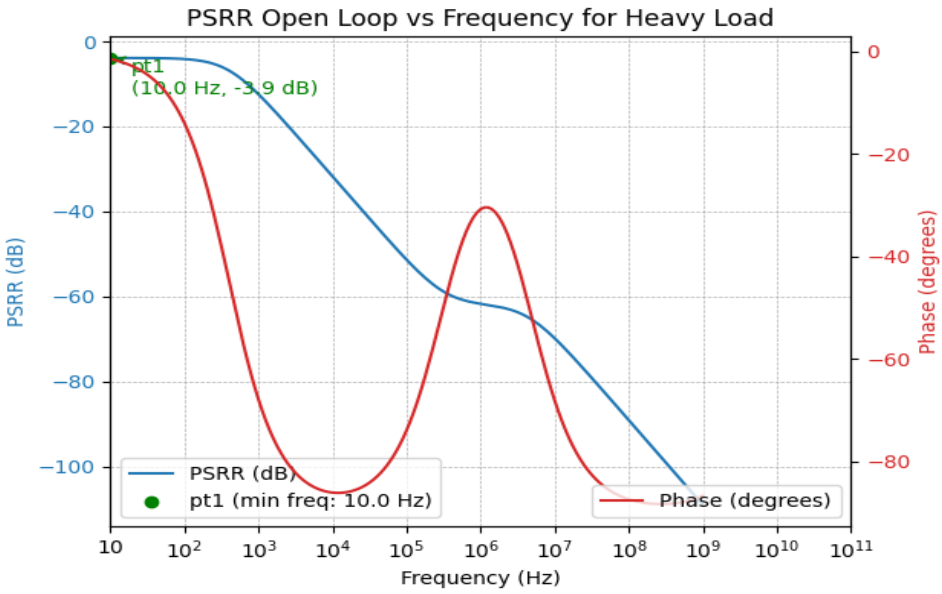

Figure 19: PSRR simulation results - heavy load.

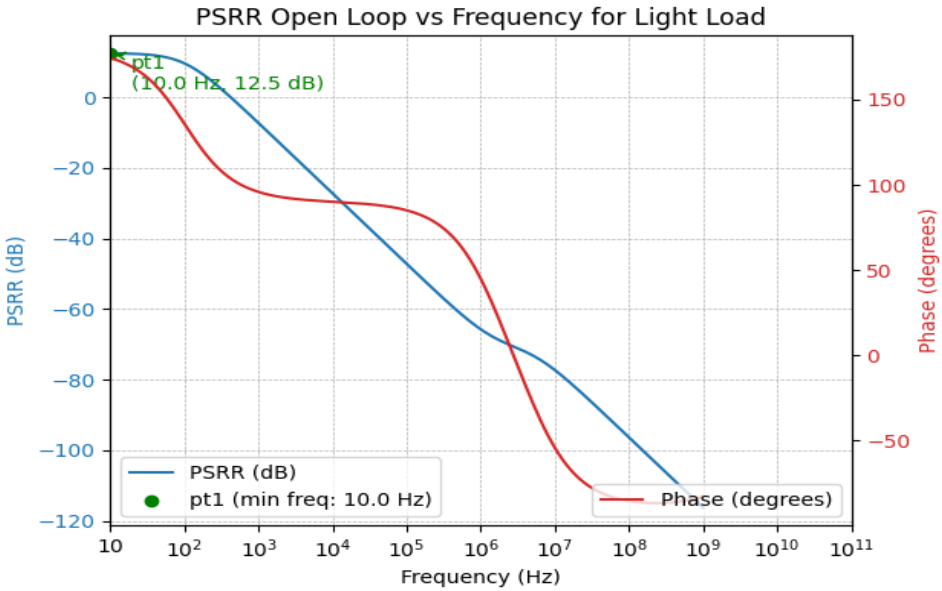

Figure 20: PSRR simulation results - light load.

Case 3:- Closed Loop PSRR Calculation

Explanation of the artifact used:-

In this circuit, we have applied an AC voltage source to VDD. The purpose of the setup is to observe the negative feedback effect, which leads to the cancellation of the output voltage (as part of a small signal analysis). According to our specifications, we expect to see a high Power Supply Rejection Ratio (PSRR) of 60dB, demonstrating that the sizing of the components is optimal. The feedback path is implemented by routing the output signal back to the input of the differential amplifier, ensuring effective feedback control and confirming the accuracy of our design.

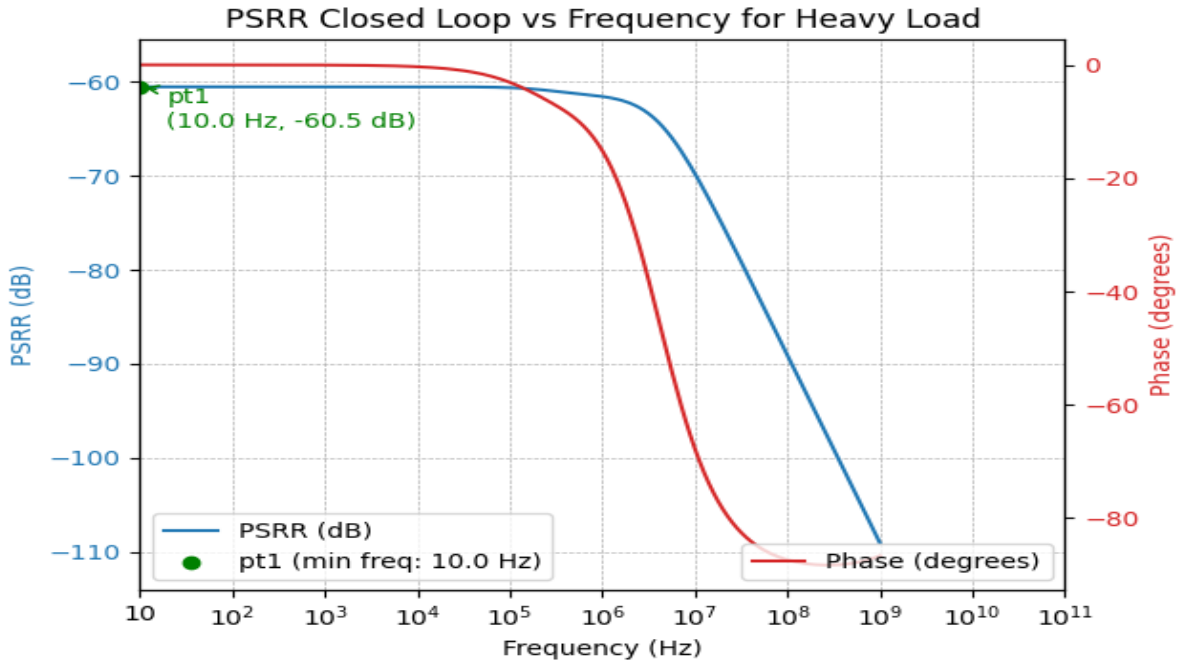

Figure 21: PSRR simulation results - heavy load.

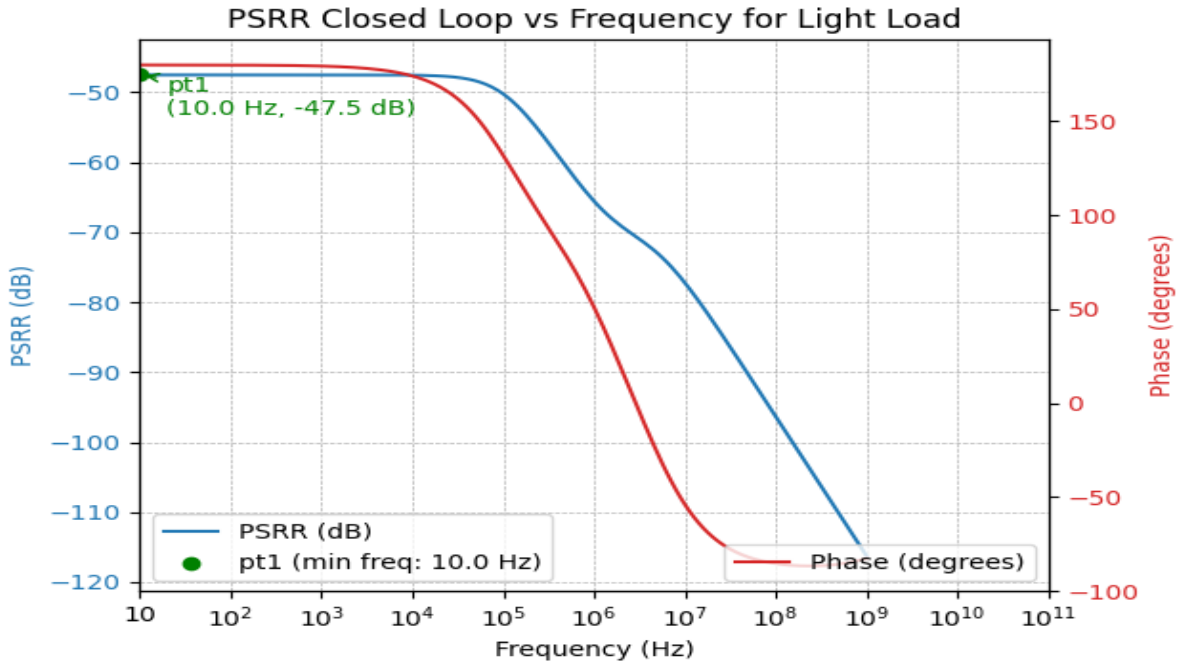

Figure 22: PSRR simulation results - light load.

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

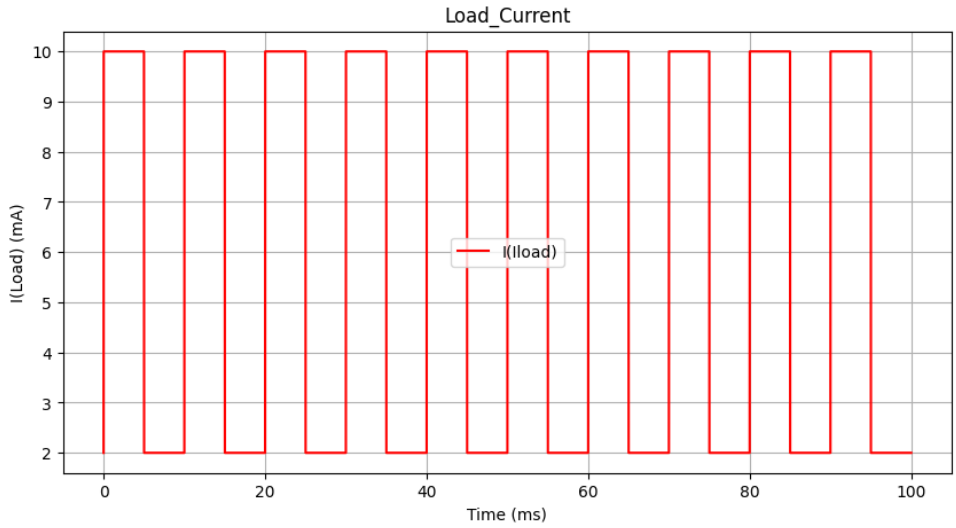

Figure 23: Load Currnt.

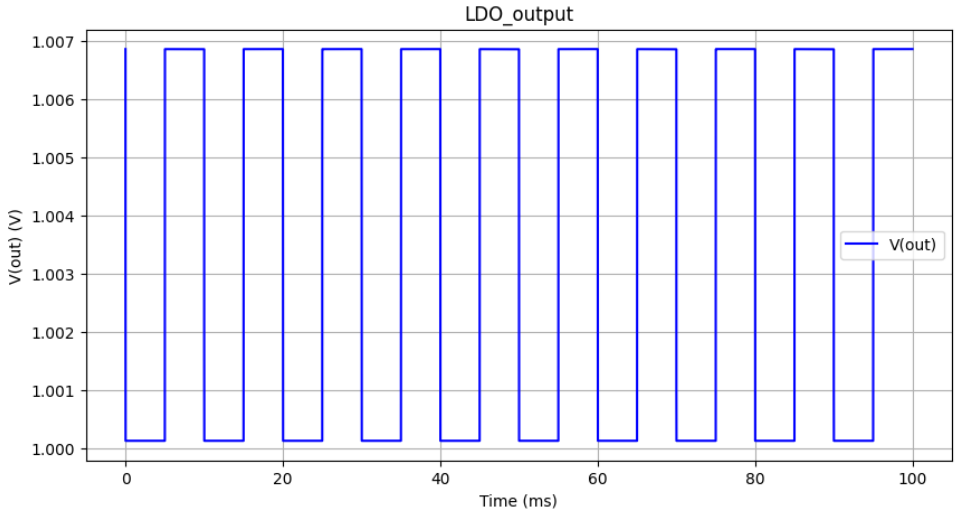

Figure 24: Node Voltage at LDO output.

9. Simulation vs. Hand Calculations

Instructions: Compare simulation results with hand calculations using techplots. Highlight agreements and discrepancies in a table.

Table 5: Simulation vs. Hand Calculations with Percentage Error

Parameter	**Simulation**	**Hand-Calculation**	**% Error**
Heavy Load Loop Gain (dB)	56.23	60	6.28%
Light Load Loop Gain (dB)	60.03	60	0.05%
Heavy Load PSRR (dB)	-60.53	-60	0.88%
Light Load PSRR (dB)	-47.52	-60	20.8%
Heavy Load Phase Margin (degrees)	86	45	91.1%
Light Load Phase Margin (degrees)	88.94	45	97.6%
Heavy Load Unity Gain Bandwidth (Hz)	266k	292k	9.7%
Light Load Unity Gain Bandwidth (Hz)	100k	106k	6%

Internally Compensated LDO Design

1. Specifications

Design: The specifications used in our design are as follows.

Table 6: Specifications Summary

Parameter	Value
Input voltage	1.4V
Output Voltage	1V
PSRR @ Heavy Load	60dB
Iload, min	2mA
Iload,Max	10mA
Cload	2nF
Iq	50uA
Transient Time	1us

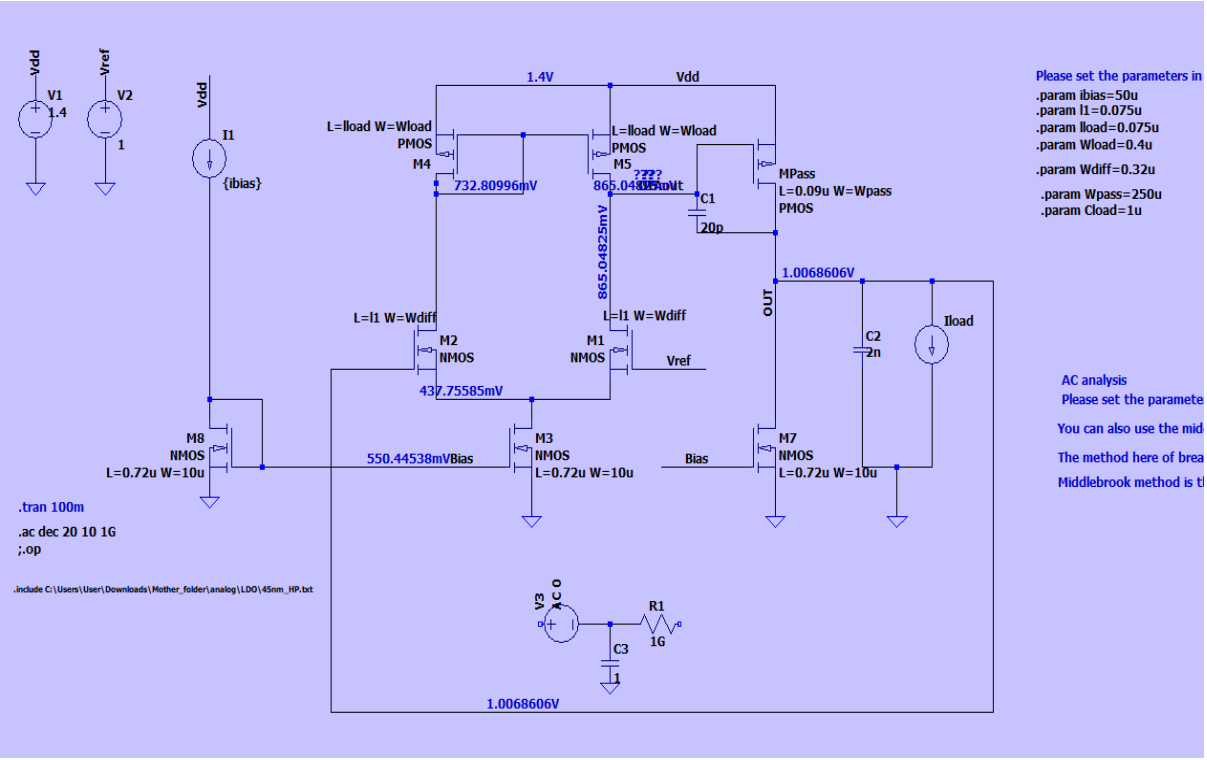

Figure 25: Our LDO schematic

Table 7: Sizing of the Transistors

Transistor Type	**Length**	**Width**
PMOS Pass FET	90nm	250µm
Diff-Amp PMOS Load	75nm	400nm
Diff-Amp Input Pair	75nm	320nm
NMOS for current mirror	720nm	10µm

SPICE Output Log: C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo - Internal.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo - Internal.asc
Start Time: Fri Dec  6 12:35:51 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
WARNING: Node NC_02 is floating.

WARNING: Less than two connections to node nc_01.  This node is used by v3.
WARNING: Less than two connections to node nc_02.  This node is used by r1.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:       m1          m2          m3          m7          m8
Model:    nmos        nmos        nmos        nmos        nmos
Id:      2.49e-05    2.49e-05    4.98e-05    5.07e-05    5.00e-05
Vgs:     5.67e-01    5.67e-01    5.50e-01    5.50e-01    5.50e-01
Vds:     3.11e-01    3.02e-01    4.33e-01    1.00e+00    5.50e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:     4.64e-01    4.64e-01    4.69e-01    4.69e-01    4.69e-01
Vdsat:   1.20e-01    1.20e-01    1.15e-01    1.15e-01    1.15e-01
Gm:      2.81e-04    2.81e-04    7.01e-04    7.13e-04    7.04e-04
Gds:     8.30e-06    8.45e-06    2.03e-06    1.61e-06    1.80e-06
Gmb      6.39e-05    6.38e-05    1.59e-04    1.62e-04    1.60e-04
Cbd:     1.46e-16    1.47e-16    4.44e-15    3.98e-15    4.33e-15
Cbs:     2.56e-16    2.56e-16    8.00e-15    8.00e-15    8.00e-15

Name:       m4          m5          mpass
Model:    pmos        pmos        pmos
Id:     -2.49e-05   -2.48e-05   -1.01e-02
Vgs:    -6.65e-01   -6.65e-01   -6.56e-01
Vds:    -6.65e-01   -6.56e-01   -4.00e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00
Vth:    -4.78e-01   -4.78e-01   -4.87e-01
Vdsat:  -1.95e-01   -1.95e-01   -1.83e-01
Gm:      2.14e-04    2.14e-04    9.58e-02
Gds:     6.91e-06    6.91e-06    2.44e-03
Gmb      4.59e-05    4.58e-05    2.03e-02
Cbd:     1.69e-16    1.69e-16    1.12e-13
Cbs:     3.20e-16    3.20e-16    2.00e-13


Total elapsed time: 0.061 seconds.
```

Figure 26: Our LDO schematic

3. Stability Analysis

Theory: As load increases in internally compensated LDOs, the non-dominant pole moves away from the origin. This increases the gap between unity gain frequency and nondominant pole at higher load currents, improving stability.

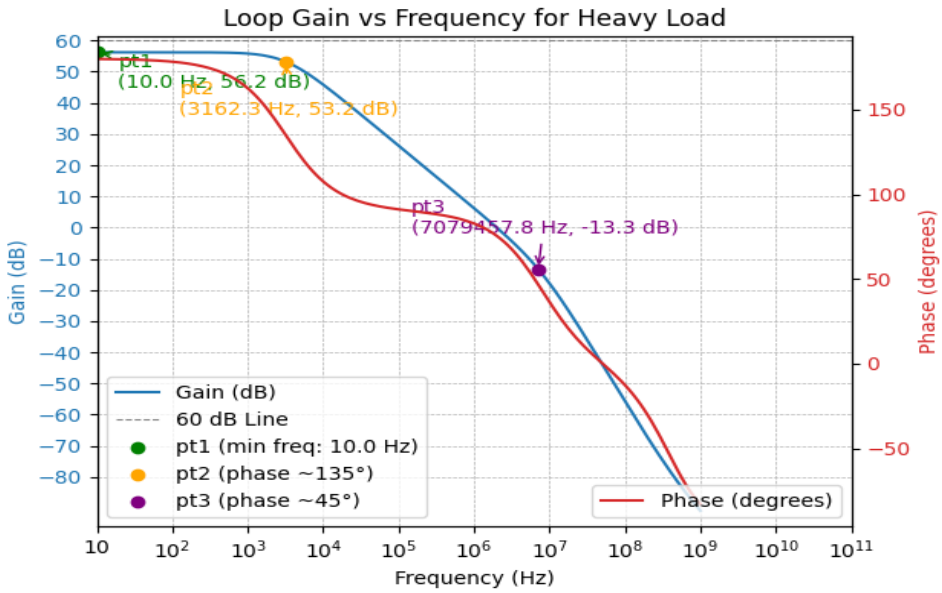

Figure 27: Python Plot.

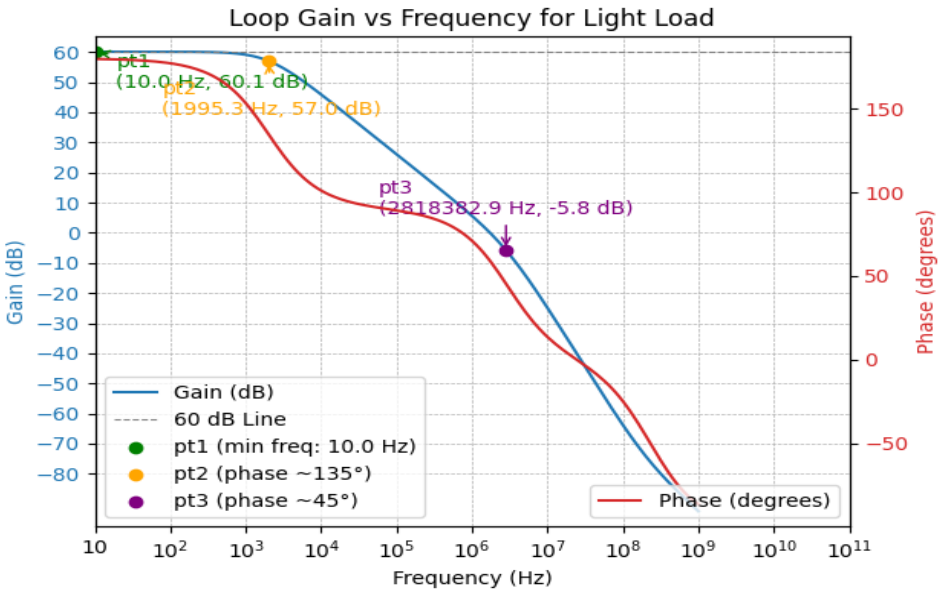

Figure 28: Python Plot.

Table 8: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	56.2db	60.1db
Unity Gain Bandwidth (Hz)	2.01MHz	1.73MHz
Phase Margin (degrees)	75.29 degree	58.97 degree
Pole 1 (Hz)	3.16kHz	1.99kHz
Pole 2 (Hz)	7.07MHz	2.81MHz

4. PSRR Simulation Results

We have designed three schematics in LTSpice to evaluate three different conditions. A simulation artifact has been created to analyze these conditions.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Case 1:- Loop gain analysis

Explanation of the artifact used:-

To calculate the loop gain, an RC circuit is placed in the feedback loop along with an AC source of 1V amplitude. This ensures that the AC voltage at the output remains constant at 1V. Additionally, the circuit requires biasing, particularly for the gate of the NMOS in the differential amplifier. To achieve this, a DC voltage is applied to the gate while the RC circuit prevents DC current from flowing to ground, yet directs high-frequency AC signals to ground.

The RC circuit is designed with a high resistance to ensure minimal voltage drop across the resistor, as the current flowing into the MOSFET gate is nearly zero. This configuration allows for effective biasing of the circuit while enabling loop gain calculation without interfering with the DC operating point.

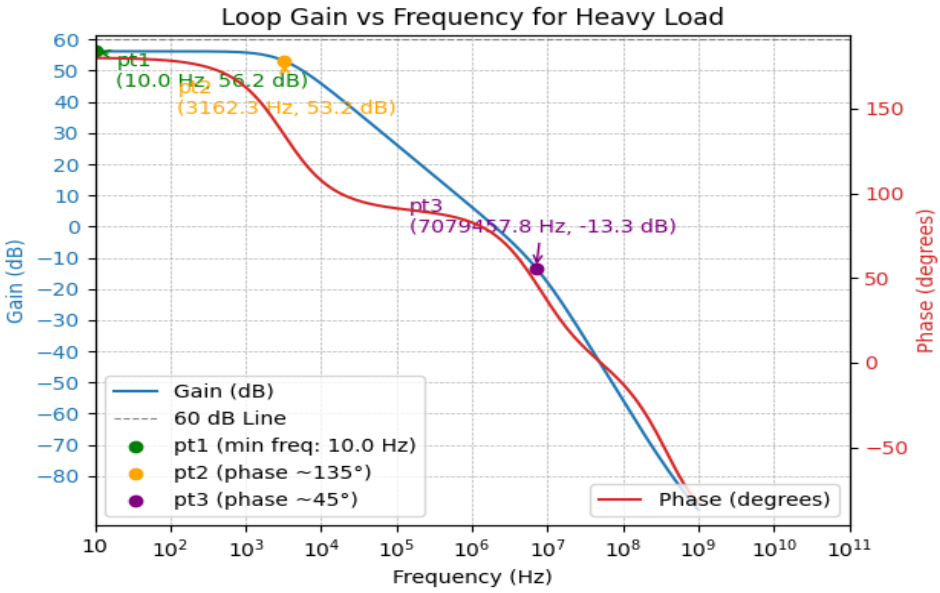

Figure 29: Python Plot.

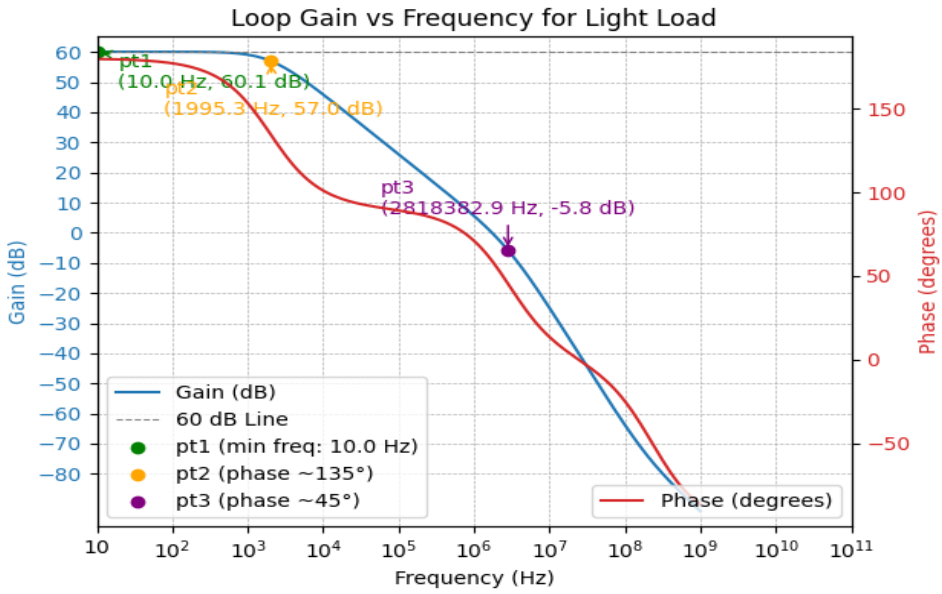

Figure 30: Python Plot.

Case 2:- Open Loop PSRR calculation

Explanation of the artifact used:-

The open loop PSRR measurement involves applying an AC signal (amplitude = 1) to VDD, which connects to both the pass FET source and differential amplifier PMOS source.

The differential amplifier is biased using an RC circuit, with AC 0 indicating the open loop condition. Since there's no feedback path in this configuration, noise rejection is poor and significant noise appears at the output - this is expected for open loop PSRR measurement.

The ultimate goal is that when the circuit is closed with feedback, this noise getting through the differential amplifier will enable proper noise rejection at the final LDO output, producing a clean DC voltage.

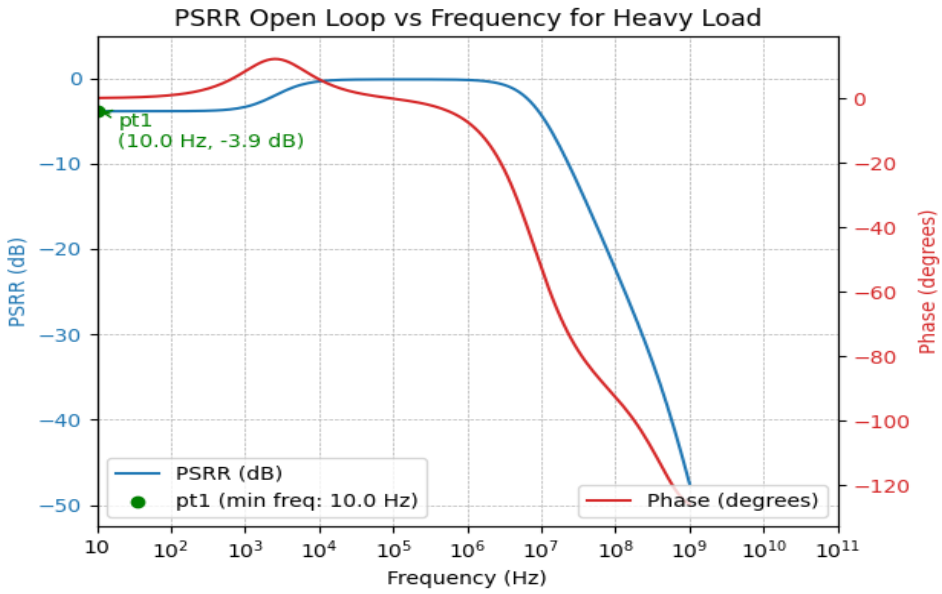

Figure 31: PSRR simulation results - heavy load.

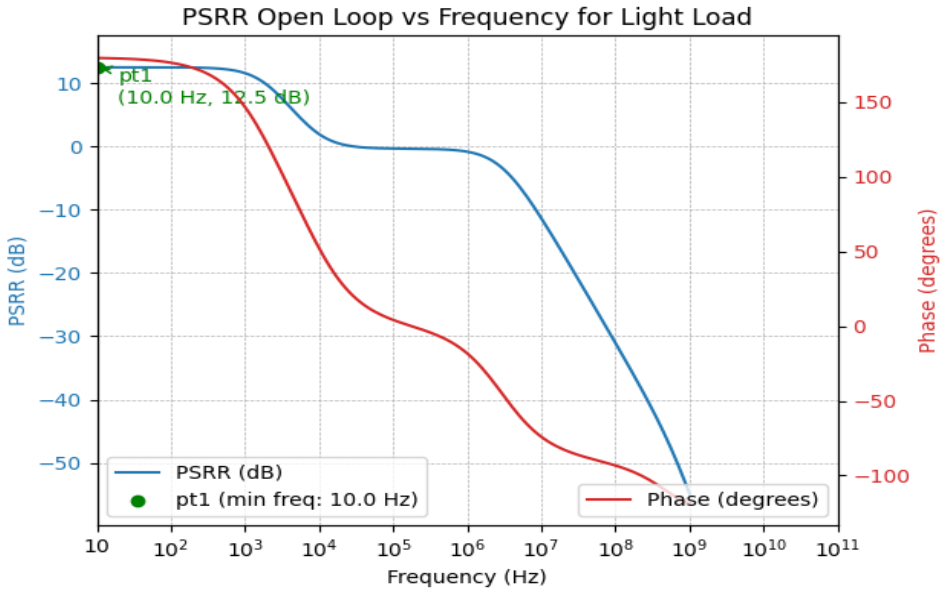

Figure 32: PSRR simulation results - light load.

Case 3:- Closed Loop PSRR Calculation

Explanation of the artifact used:-

In this circuit, we have applied an AC voltage source to VDD. The purpose of the setup is to observe the negative feedback effect, which leads to the cancellation of the output voltage (as part of a small signal analysis). According to our specifications, we expect to see a high Power Supply Rejection Ratio (PSRR) of 60dB, demonstrating that the sizing of the components is optimal. The feedback path is implemented by routing the output signal back to the input of the differential amplifier, ensuring effective feedback control and confirming the accuracy of our design.

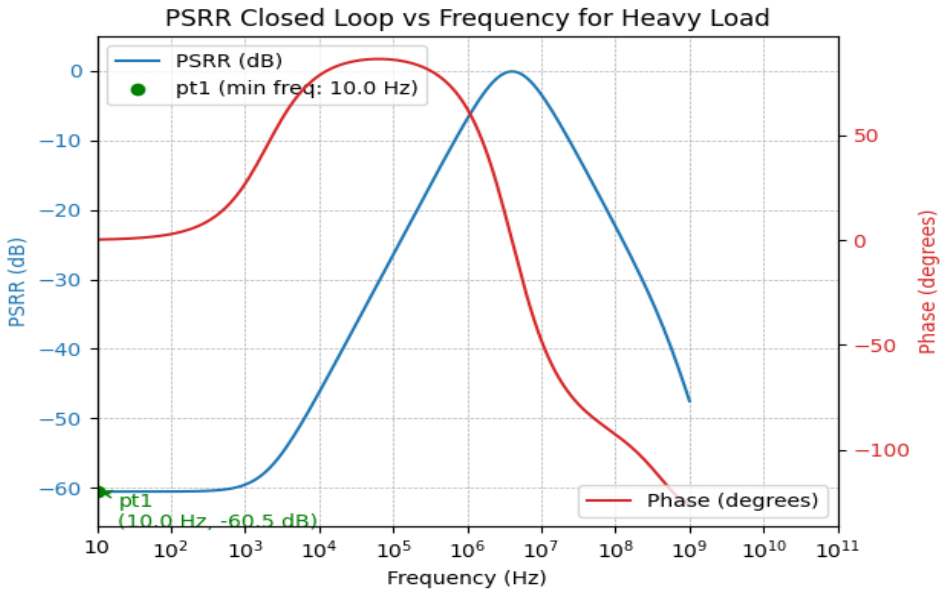

Figure 33: PSRR simulation results - heavy load.

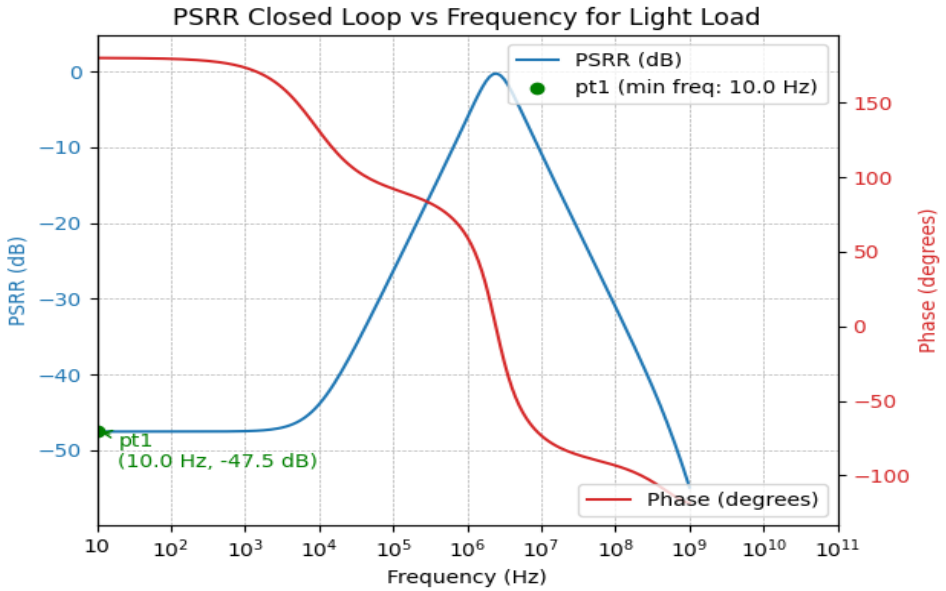

Figure 34: PSRR simulation results - light load.

5. Transient Simulation Results

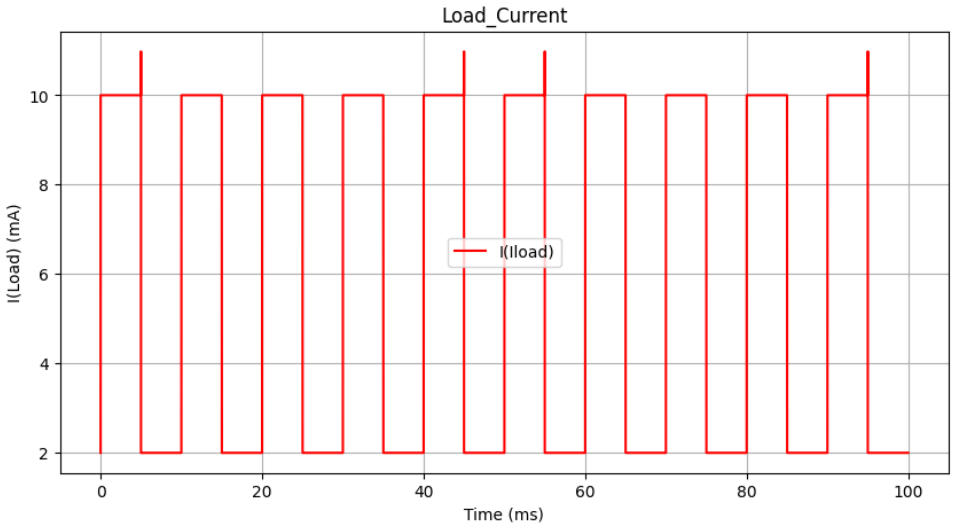

Figure 35: Load Currnt.

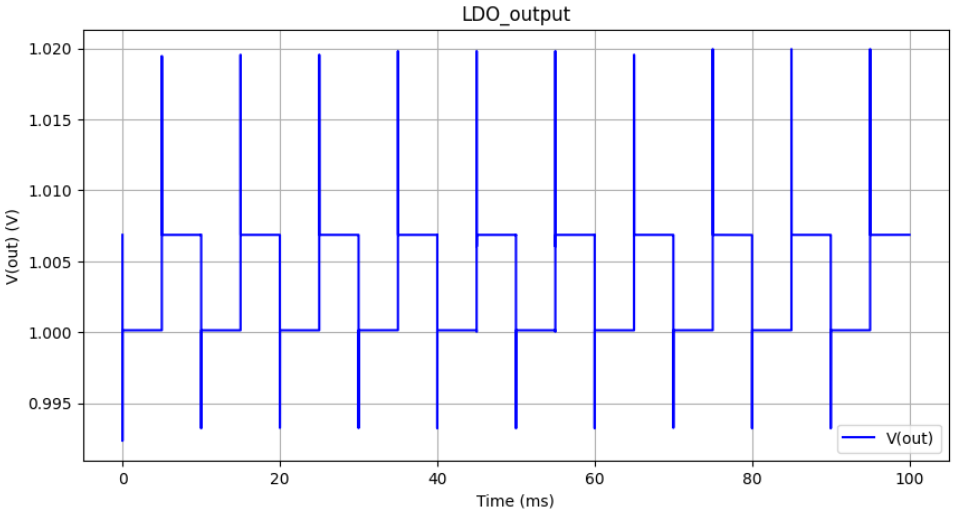

Figure 36: Node Voltage at LDO output.

6. Simulation vs. Hand Calculations

Instructions: Compare simulation results with hand calculations using techplots. Highlight agreements and discrepancies in a table.

Table 9: Simulation vs. Hand Calculations with Percentage Error

Parameter	**Simulation**	**Hand-Calculation**	**% Error**
Heavy Load Loop Gain (dB)	56.23	60	6.28%
Light Load Loop Gain (dB)	60.07	60	0.12%
Heavy Load PSRR (dB)	-60.53	-60	0.88%
Light Load PSRR (dB)	-47.52	-60	20.8%
Heavy Load Phase Margin (degrees)	75.29	45	67.3%
Light Load Phase Margin (degrees)	58.97	45	31.04%
Heavy Load Unity Gain Bandwidth (Hz)	2.01M	2.1M	4.285%
Light Load Unity Gain Bandwidth (Hz)	1.73M	2.03M	14.77%

Ultra Low Output Capacitance LDO Design (C_L) for PSRR

Maximize PSRR with minimal quiescent current while avoiding subthreshold operation. Aim for the lowest possible load capacitance.

1. Specifications

Design: The specifications used in our design are as follows.

Table 10: Specifications Summary

Parameter	Value
Input voltage	1.4V
Output Voltage	1V
PSRR @ Heavy Load	60dB
Iload, min	2mA
Iload,Max	10mA
Cload	2pF
Iq	10uA

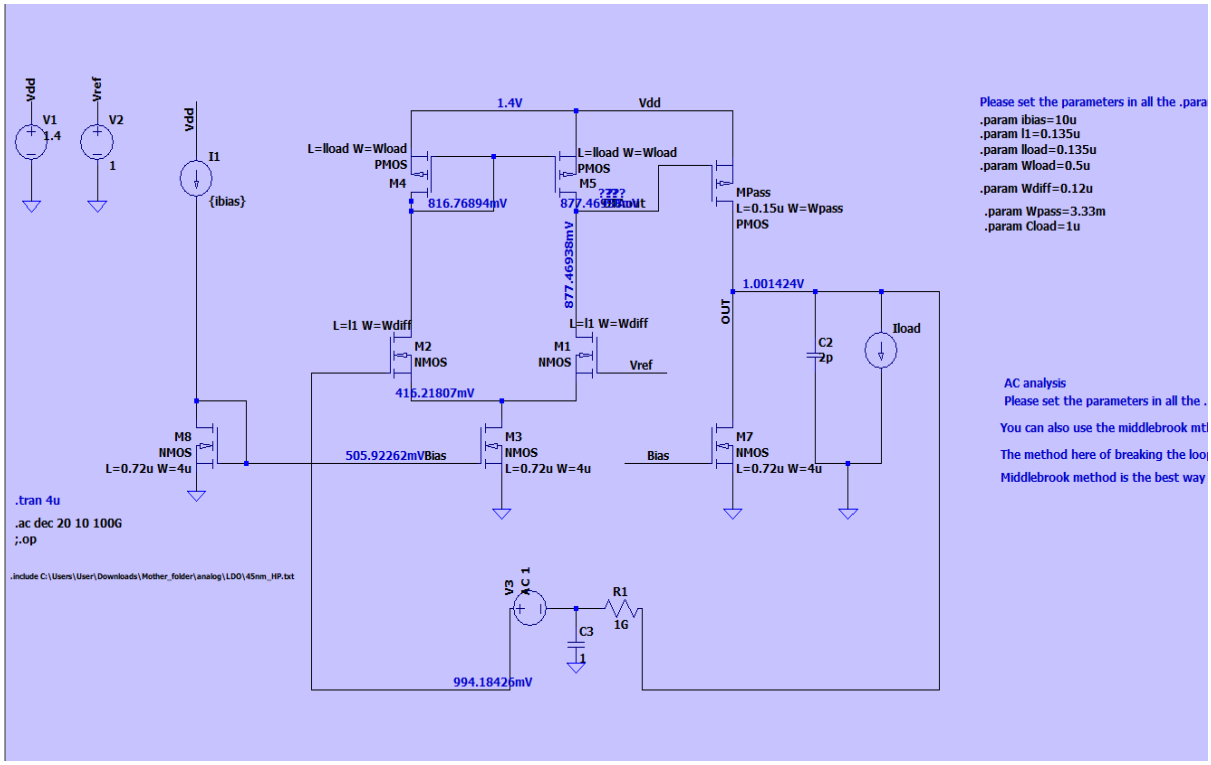

Figure 37: Our LDO schematic

Table 11: Sizing of the Transistors

Transistor Type	**Length**	**Width**
PMOS Pass FET	150nm	3.33mm
Diff-Amp PMOS Load	135nm	500nm
Diff-Amp Input Pair	135nm	120nm
NMOS for current mirror	720nm	4µm

SPICE Output Log: C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo-internal-lowCap.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\User\Downloads\Mother_folder\analog\LDO\Design\##VL502_PSRR_Demo\VL502_1st_LDO\502_Demo-internal-lowCap.asc
Start Time: Fri Dec  6 12:30:16 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
WARNING: Node NC_02 is floating.

WARNING: Less than two connections to node nc_01.  This node is used by v3.
WARNING: Less than two connections to node nc_02.  This node is used by r1.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m7           m8
Model:     nmos         nmos         nmos         nmos         nmos
Id:      5.16e-06     4.80e-06     9.96e-06     1.02e-05     1.00e-05
Vgs:     5.84e-01     5.78e-01     5.06e-01     5.06e-01     5.06e-01
Vds:     4.61e-01     4.01e-01     4.16e-01     9.94e-01     5.06e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.68e-01     4.68e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.35e-01     1.31e-01     8.88e-02     8.88e-02     8.88e-02
Gm:      5.87e-05     5.62e-05     1.68e-04     1.72e-04     1.69e-04
Gds:     5.07e-07     5.16e-07     4.41e-07     3.66e-07     4.07e-07
Gmb      1.35e-05     1.29e-05     3.78e-05     3.85e-05     3.79e-05
Cbd:     5.29e-17     5.37e-17     1.78e-15     1.59e-15     1.75e-15
Cbs:     9.60e-17     9.60e-17     3.20e-15     3.20e-15     3.20e-15

Name:       m4           m5         mpass
Model:    pmos         pmos         pmos
Id:     -4.80e-06    -4.76e-06    -1.00e-02
Vgs:    -5.83e-01    -5.83e-01    -5.22e-01
Vds:    -5.83e-01    -5.22e-01    -4.06e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.89e-01    -4.90e-01    -4.90e-01
Vdsat:  -1.26e-01    -1.26e-01    -8.69e-02
Gm:      6.78e-05     6.74e-05     1.86e-01
Gds:     5.71e-07     5.86e-07     1.32e-03
Gmb      1.41e-05     1.40e-05     3.83e-02
Cbd:     2.15e-16     2.18e-16     1.49e-12
Cbs:     4.00e-16     4.00e-16     2.66e-12

Total elapsed time: 0.067 seconds.
```

Figure 38: Our LDO schematic

2. Stability Analysis

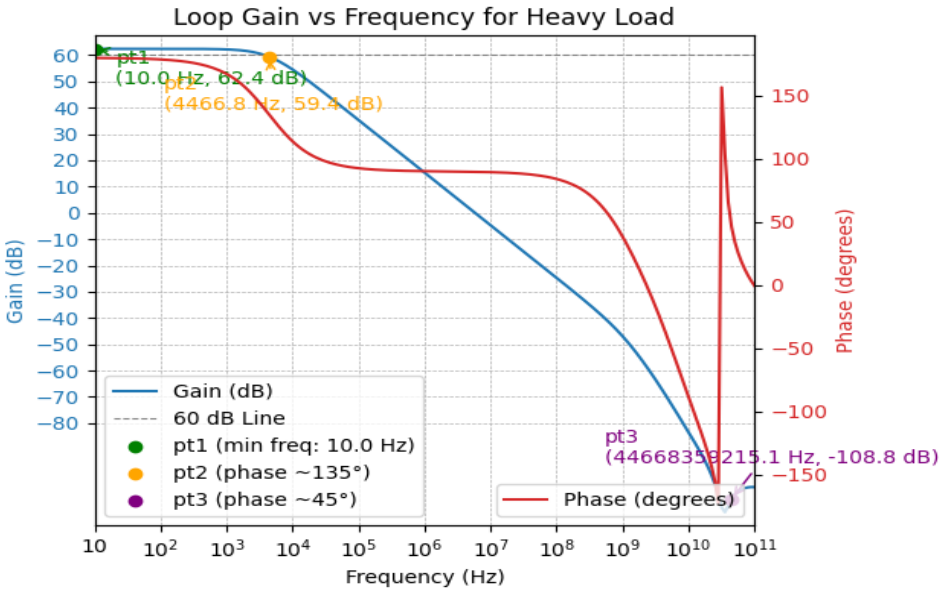

Figure 39: Python Plot.

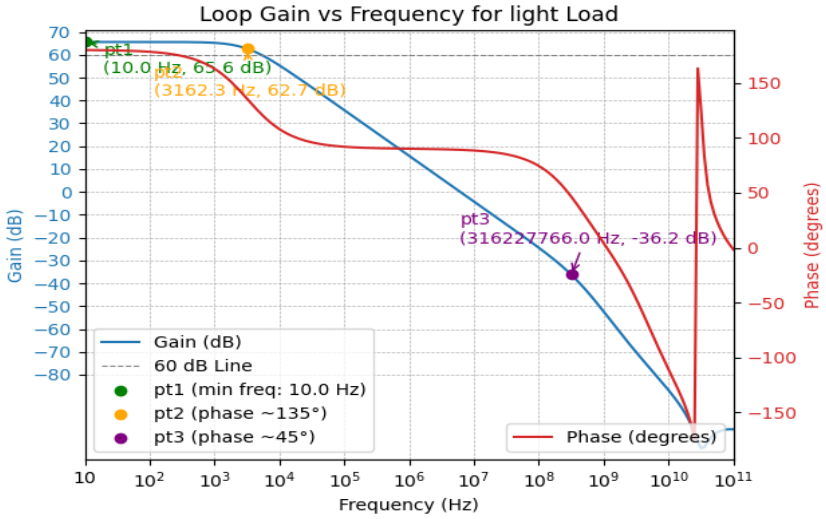

Figure 40: Python Plot.

Table 12: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	62.4db	65.6db
Unity Gain Bandwidth (Hz)	5.75MHz	6.1MHz
Phase Margin (degrees)	89.69 degree	89.05 degree
Pole 1 (Hz)	4.4kHz	3.16kHz
Pole 2 (Hz)	446MHz	316MHz

3. PSRR Simulation Results

We have designed three schematics in LTSpice to evaluate three different conditions. A simulation artifact has been created to analyze these conditions.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Case 1:- Loop gain analysis

Explanation of the artifact used:-

To calculate the loop gain, an RC circuit is placed in the feedback loop along with an AC source of 1V amplitude. This ensures that the AC voltage at the output remains constant at 1V. Additionally, the circuit requires biasing, particularly for the gate of the NMOS in the differential amplifier. To achieve this, a DC voltage is applied to the gate while the RC circuit prevents DC current from flowing to ground, yet directs high-frequency AC signals to ground.

The RC circuit is designed with a high resistance to ensure minimal voltage drop across the resistor, as the current flowing into the MOSFET gate is nearly zero. This configuration allows for effective biasing of the circuit while enabling loop gain calculation without interfering with the DC operating point.

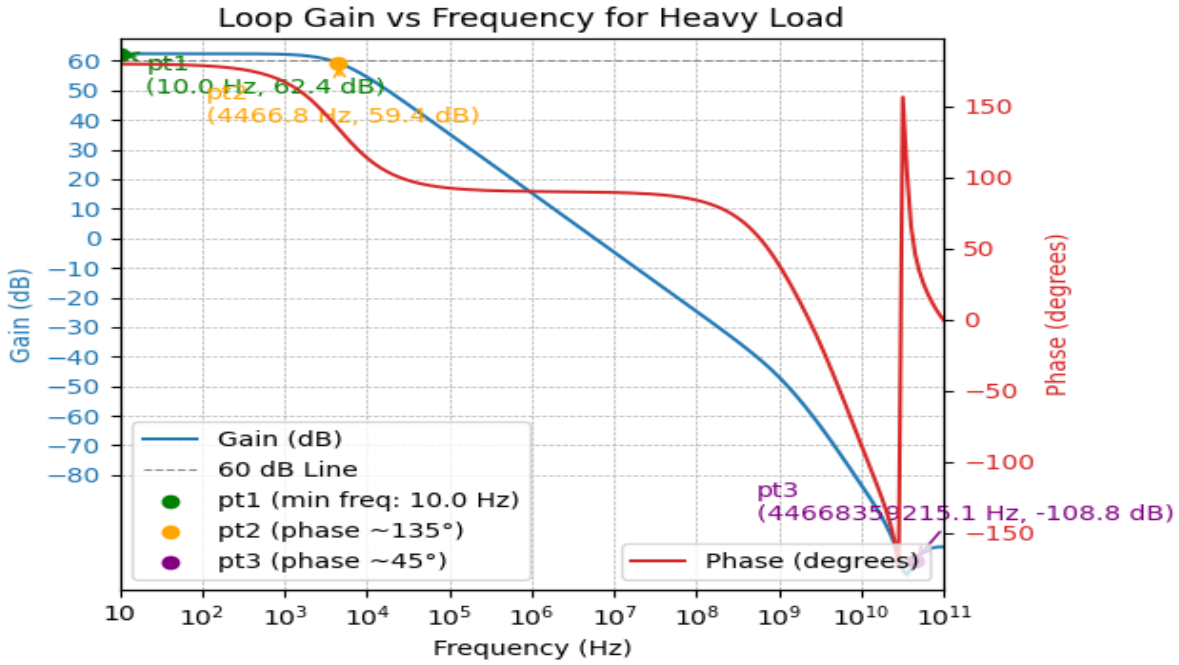

Figure 41: PSRR simulation results - heavy load.

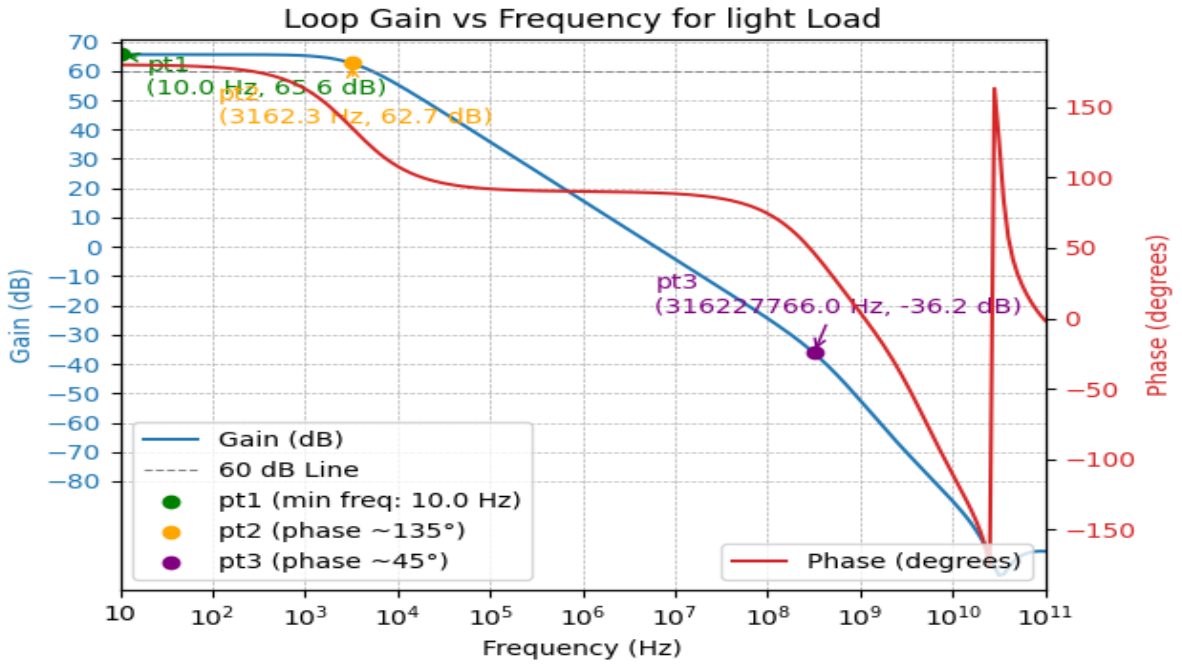

Figure 42: PSRR simulation results - light load.

Case 2:- Open Loop PSRR calculation

Explanation of the artifact used:-

The open loop PSRR measurement involves applying an AC signal (amplitude = 1) to VDD, which connects to both the pass FET source and differential amplifier PMOS source.

The differential amplifier is biased using an RC circuit, with AC 0 indicating the open loop condition. Since there's no feedback path in this configuration, noise rejection is poor and significant noise appears at the output - this is expected for open loop PSRR measurement.

The ultimate goal is that when the circuit is closed with feedback, this noise getting through the differential amplifier will enable proper noise rejection at the final LDO output, producing a clean DC voltage.

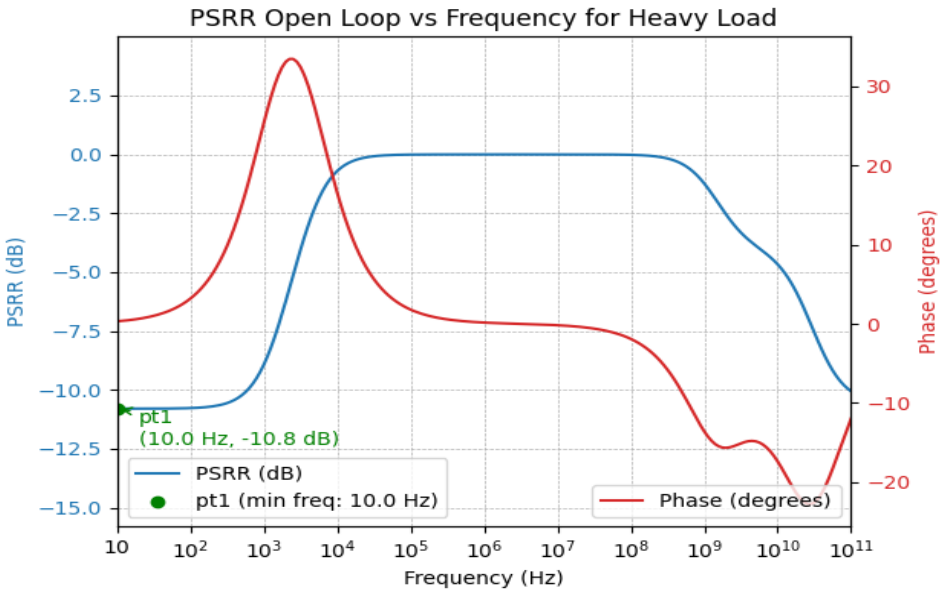

Figure 43: PSRR simulation results - heavy load.

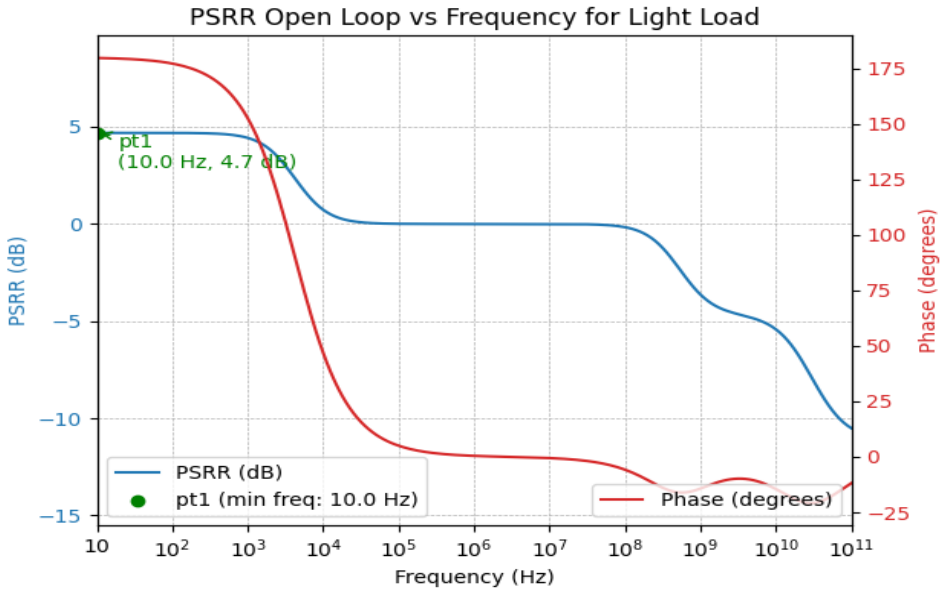

Figure 44: PSRR simulation results - light load.

Case 3:- Closed Loop PSRR Calculation

Explanation of the artifact used:-

In this circuit, we have applied an AC voltage source to VDD. The purpose of the setup is to observe the negative feedback effect, which leads to the cancellation of the output voltage (as part of a small signal analysis). According to our specifications, we expect to see a high Power Supply Rejection Ratio (PSRR) of 60dB, demonstrating that the sizing of the components is optimal. The feedback path is implemented by routing the output signal back to the input of the differential amplifier, ensuring effective feedback control and confirming the accuracy of our design.

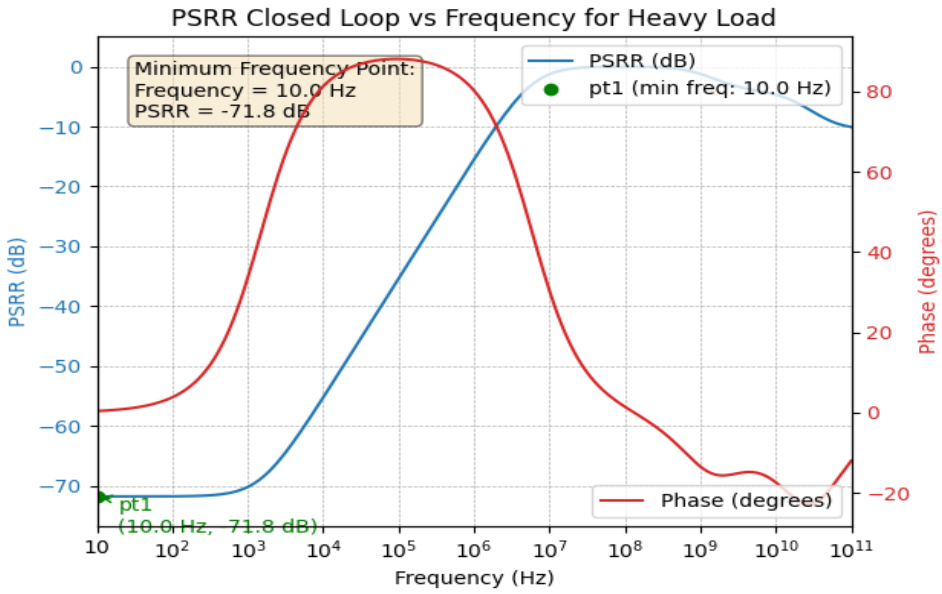

Figure 45: PSRR simulation results - heavy load.

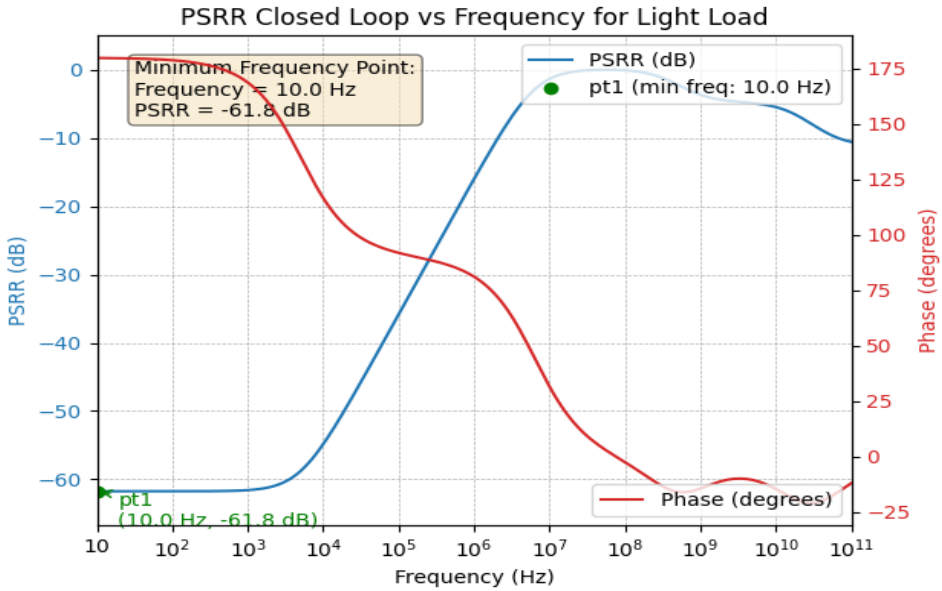

Figure 46: PSRR simulation results - light load.

Subthreshold LDO Design

Utilize subthreshold MOSFETs to achieve a low quiescent current (Iq) in the LDO. Characterize the 180 nm process for high gm/Id values up to 25.

1. Specifications

Design: The specifications used in our design are as follows.

Table 13: Specifications Summary

Parameter	Value
Input voltage	1.4V
Output Voltage	1V
PSRR @ Heavy Load	60dB
Iload, min	2mA
Iload,Max	10mA
Cload	1uF
Iq	10uA

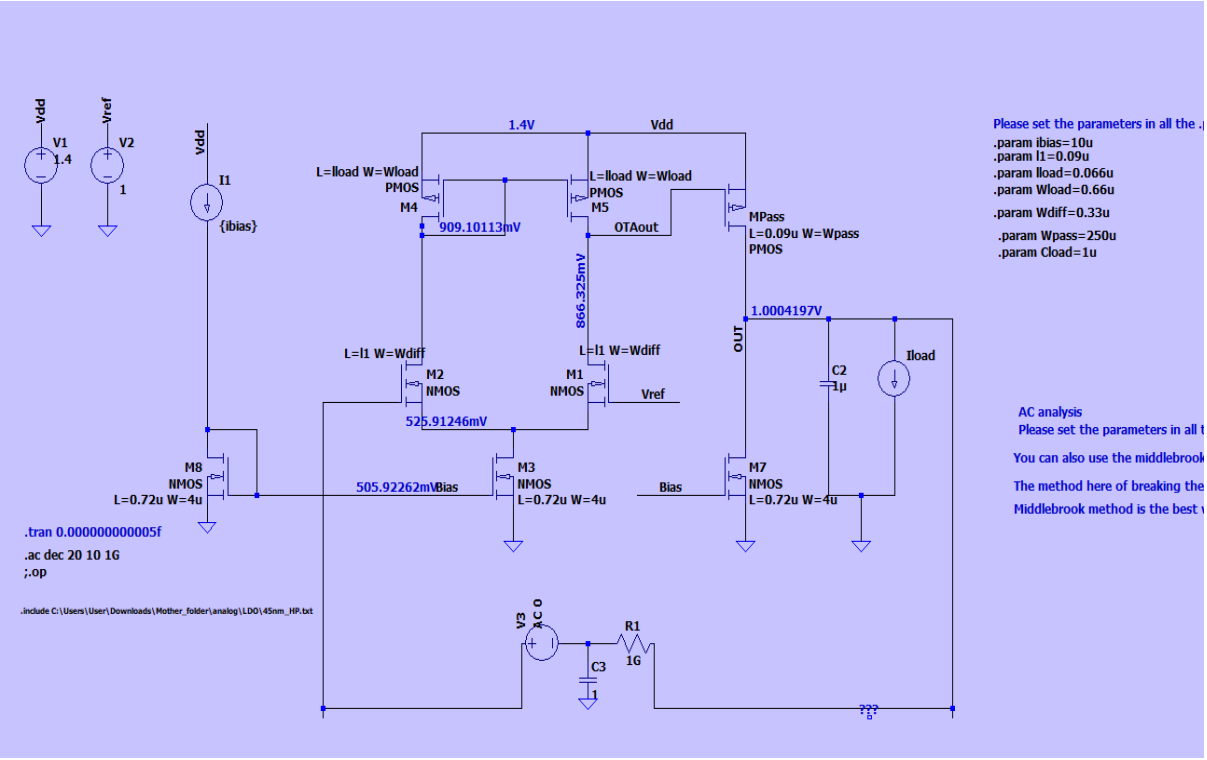

Figure 47: Our LDO schematic

Table 14: Sizing of the Transistors

Transistor Type	**Length**	**Width**
PMOS Pass FET	90nm	250um
Diff-Amp PMOS Load	66nm	660nm
Diff-Amp Input Pair	90nm	330nm
NMOS for current mirror	720nm	4µm

Table 15: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	54.7db	59.1db
Unity Gain Bandwidth (Hz)	214.27kHz	87.75kHz
Phase Margin (degrees)	83.26 degree	87.5 degree
Pole 1 (Hz)	398Hz	100Hz
Pole 2 (Hz)	1.77MHz	1.99MHz

2. Stability Analysis

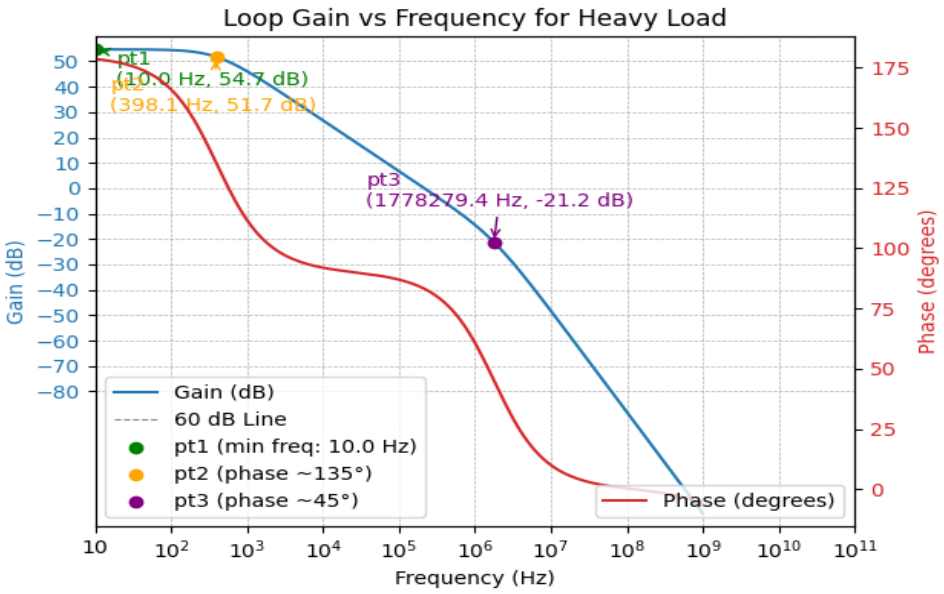

Figure 48: Python Plot.

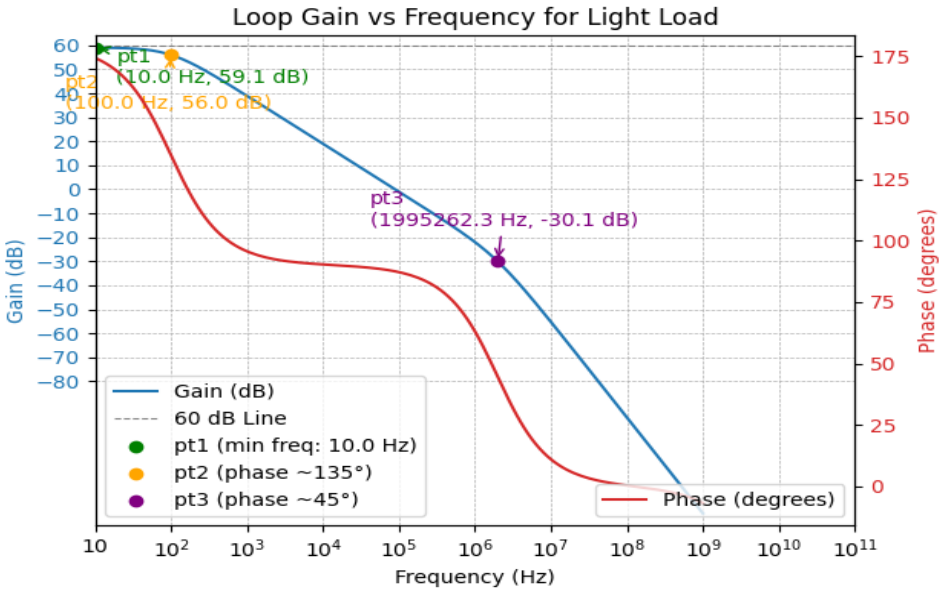

Figure 49: Python Plot.

3. PSRR Simulation Results

We have designed three schematics in LTSpice to evaluate three different conditions. A simulation artifact has been created to analyze these conditions.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Case 1:- Loop gain analysis

Explanation of the artifact used:-

To calculate the loop gain, an RC circuit is placed in the feedback loop along with an AC source of 1V amplitude. This ensures that the AC voltage at the output remains constant at 1V. Additionally, the circuit requires biasing, particularly for the gate of the NMOS in the differential amplifier. To achieve this, a DC voltage is applied to the gate while the RC circuit prevents DC current from flowing to ground, yet directs high-frequency AC signals to ground.

The RC circuit is designed with a high resistance to ensure minimal voltage drop across the resistor, as the current flowing into the MOSFET gate is nearly zero. This configuration allows for effective biasing of the circuit while enabling loop gain calculation without interfering with the DC operating point.

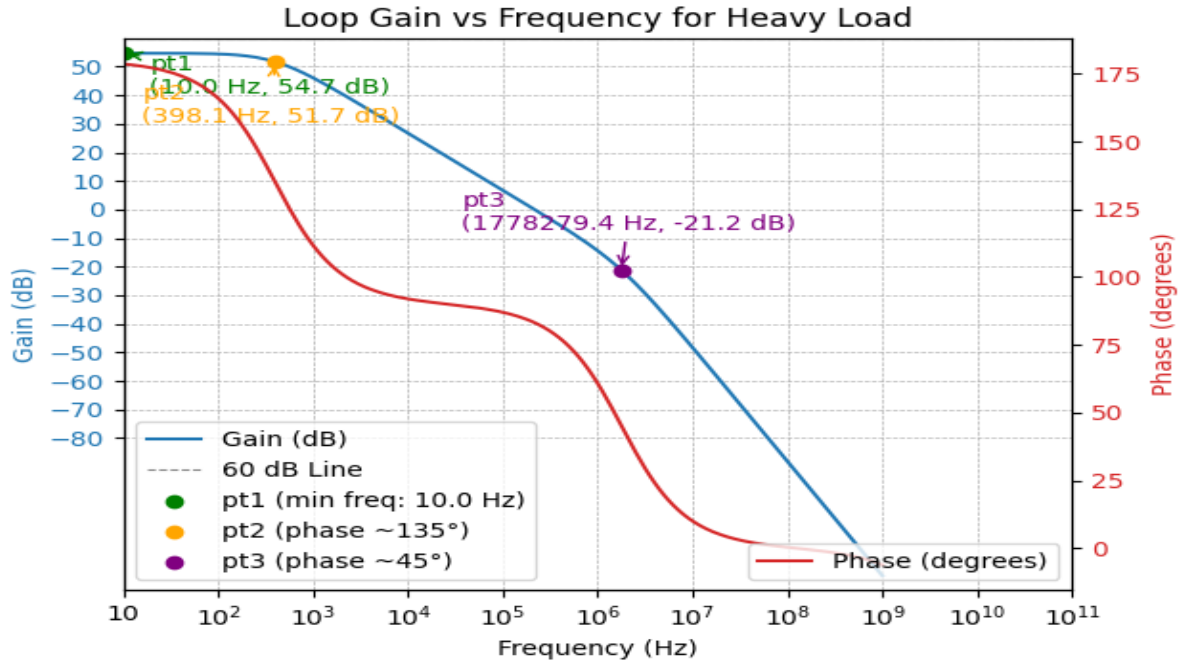

Figure 50: Python Plot.

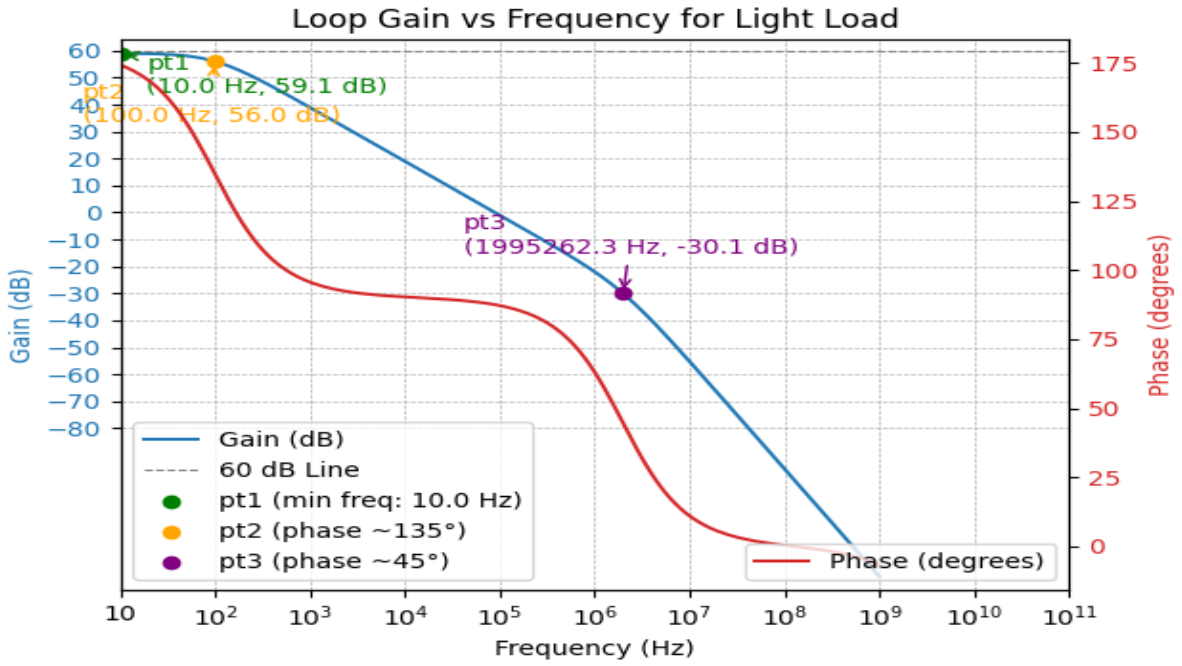

Figure 51: Python Plot.

Case 2:- Open Loop PSRR calculation

Explanation of the artifact used:-

The open loop PSRR measurement involves applying an AC signal (amplitude = 1) to VDD, which connects to both the pass FET source and differential amplifier PMOS source.

The differential amplifier is biased using an RC circuit, with AC 0 indicating the open loop condition. Since there's no feedback path in this configuration, noise rejection is poor and significant noise appears at the output - this is expected for open loop PSRR measurement.

The ultimate goal is that when the circuit is closed with feedback, this noise getting through the differential amplifier will enable proper noise rejection at the final LDO output, producing a clean DC voltage.

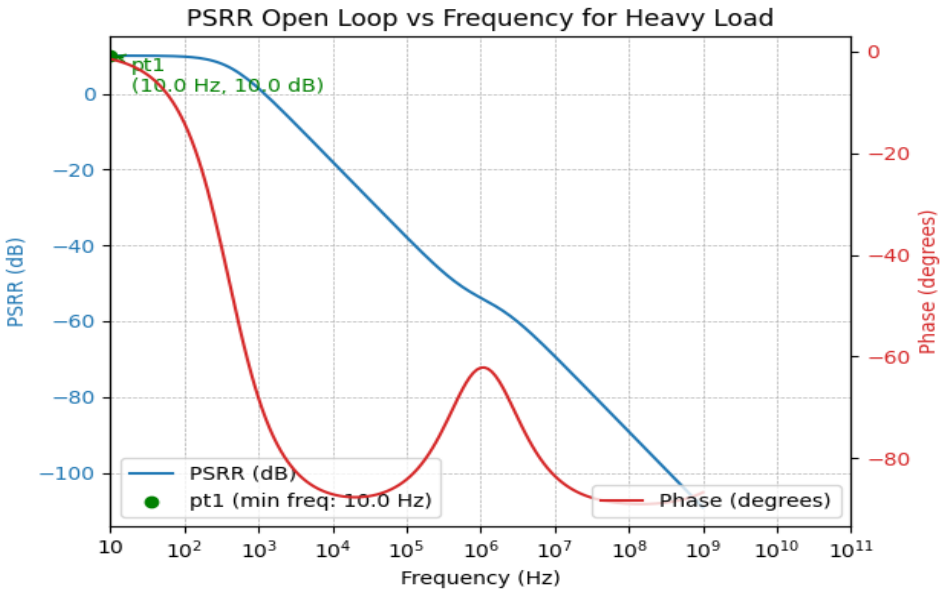

Figure 52: PSRR simulation results - heavy load.

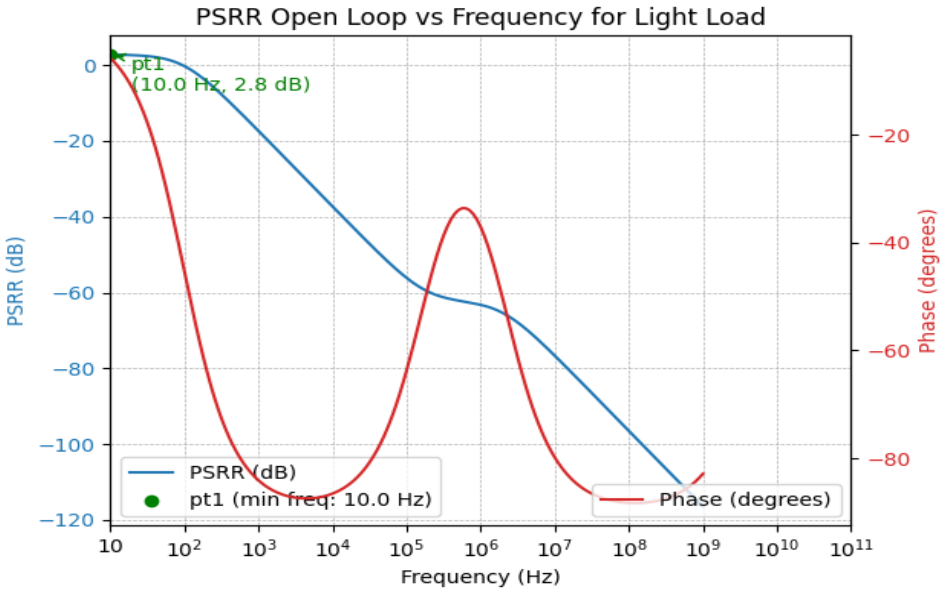

Figure 53: PSRR simulation results - light load.

Case 3:- Closed Loop PSRR Calculation

Explanation of the artifact used:-

In this circuit, we have applied an AC voltage source to VDD. The purpose of the setup is to observe the negative feedback effect, which leads to the cancellation of the output voltage (as part of a small signal analysis). According to our specifications, we expect to see a high Power Supply Rejection Ratio (PSRR) of 60dB, demonstrating that the sizing of the components is optimal. The feedback path is implemented by routing the output signal back to the input of the differential amplifier, ensuring effective feedback control and confirming the accuracy of our design.

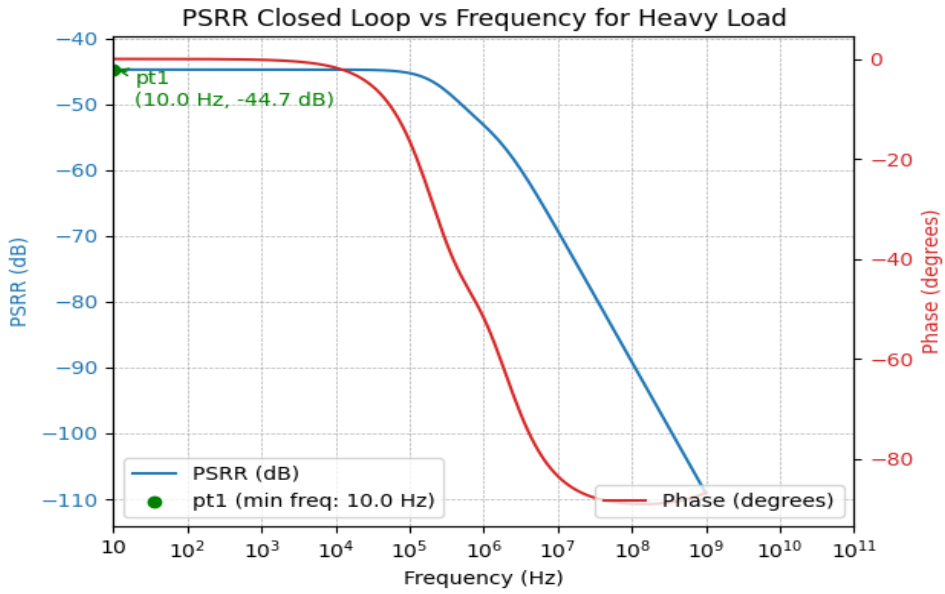

Figure 54: PSRR simulation results - heavy load.

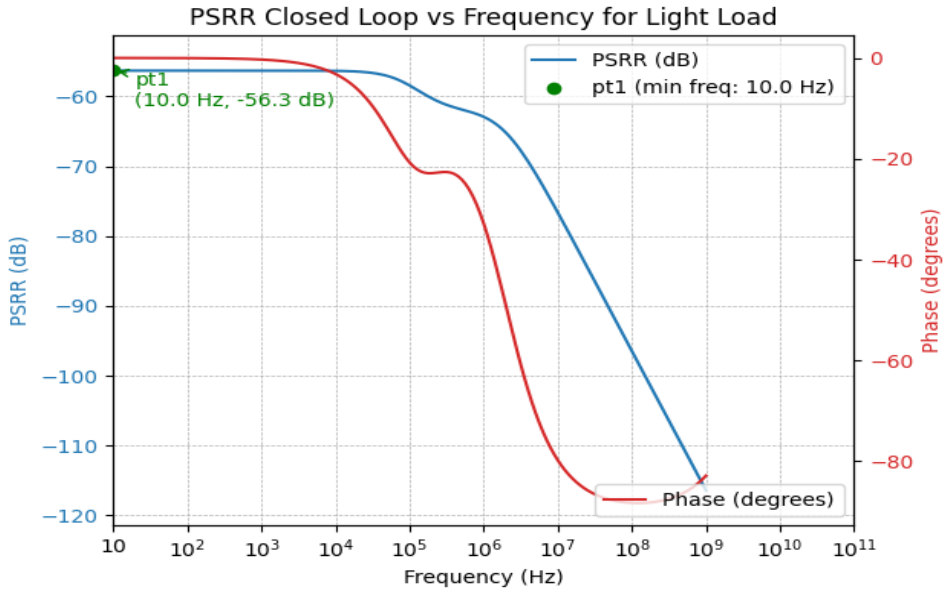

Figure 55: PSRR simulation results - light load.