

EE5311 Tutorial 6b Report - EE22B070

Draw the schematic of an 8-bit ripple-carry adder using the above mirror-symmetric full adder and trace its critical path.

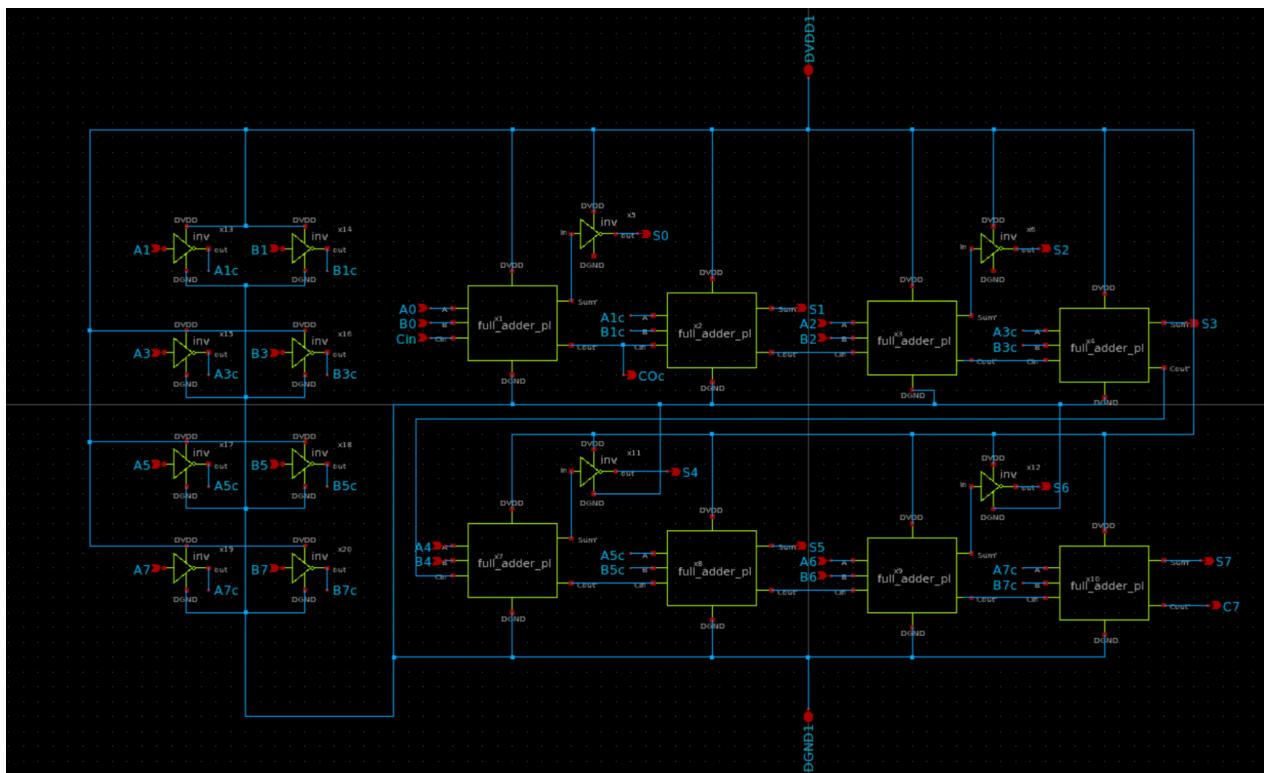
(a) Measure the delay of the critical path if the MSB sum and carry bits (S_7, C_7) drive a unit inverter each.

(b) Compare the measured delay with the delay estimated using logical/electrical/branching effort.

(c) Draw the layout of the complete ripple-carry adder using the above full-adder layout and inverter layout from Assignment 5. Ensure that the aspect ratio (width/height) of your layout is in the range [0.9, 1.1].
Measure the layout extracted delay and compare it with the pre-layout delay

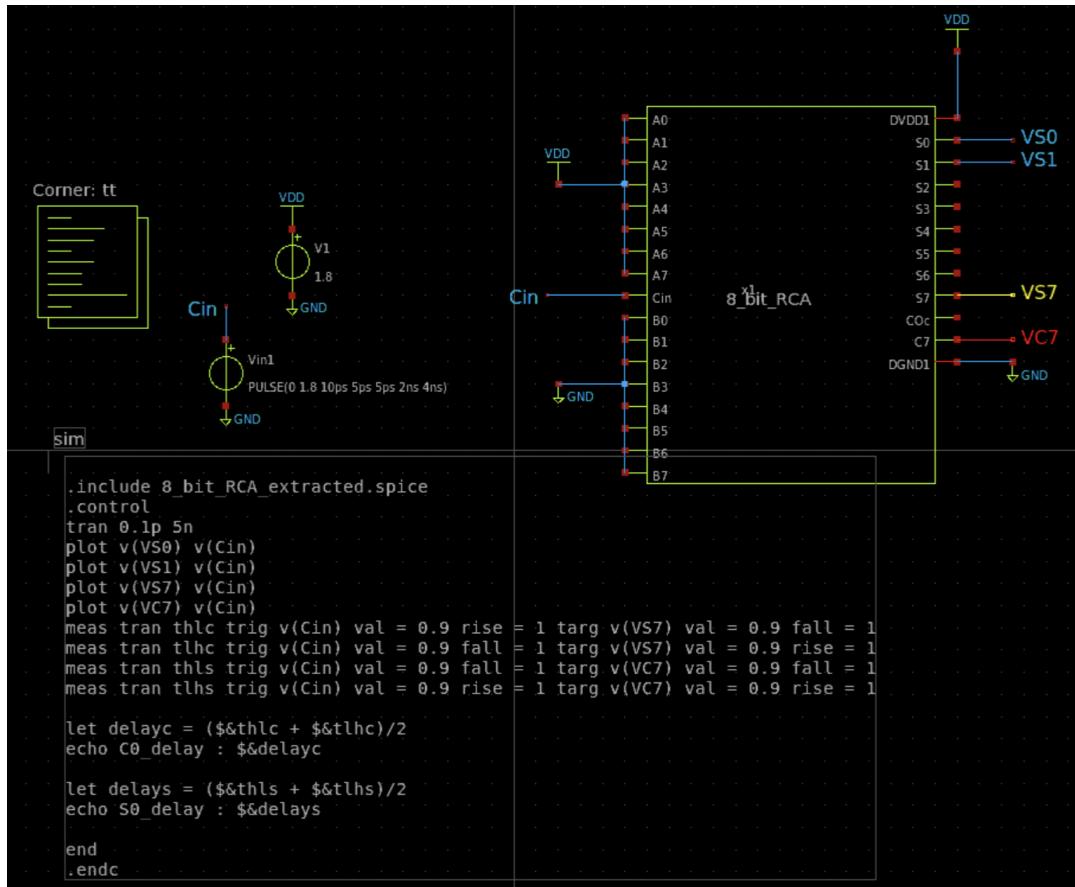
Schematic:

8-bit Ripple Carry Adder Schematic:



The critical path is from C_1 to S_7 , going through all the carry logic.

Simulation Schematic:



Calculation:

after correction of calculation from (6a)

for a full adder whose \bar{S} has a ref. inverter as load
and \bar{C}_{out} has another full adder as the load :

$$d_{C_n - \bar{C}_{out}} = 84 \text{ ps}, \quad d_{C_{in} - \bar{S}} = 168 \text{ ps}.$$

All FA except last one will follow this

for last FA: load of \bar{C}_{out} is ref. inv.

$$n = \frac{C_{load}}{C_n} = \frac{C_{inv}}{C_{in_carry}} = \frac{6}{8+4} = \frac{1}{2},$$

$$\begin{aligned} d &= \tau(h_{gep}) = 10.5 \left(\frac{1}{2} \times 2 + 4 \right) \\ &= 52.5 \text{ ps}. \end{aligned}$$

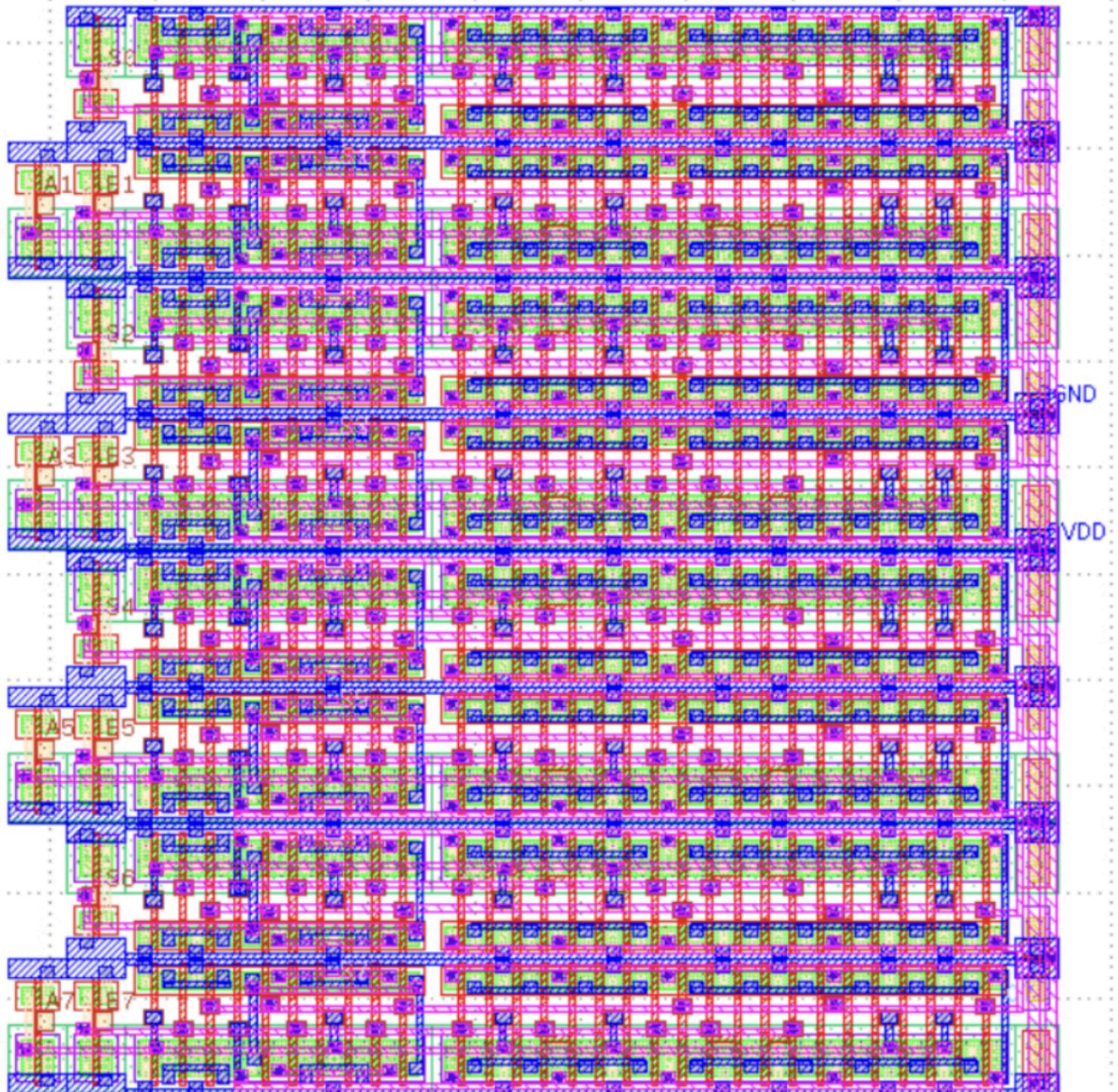
$$d_{C_{in} - \bar{S}_7} = 7 \times (105) + 168 = 903 \text{ ps}$$

$$d_{C_1 - \bar{C}_9} = 7 \times 105 + 52.5 = 787.5 \text{ ps},$$

$d_{\text{L1 to S7}} = 908 \text{ ps}$

$d_{\text{L1 to C7}} = 787.5 \text{ ps}$

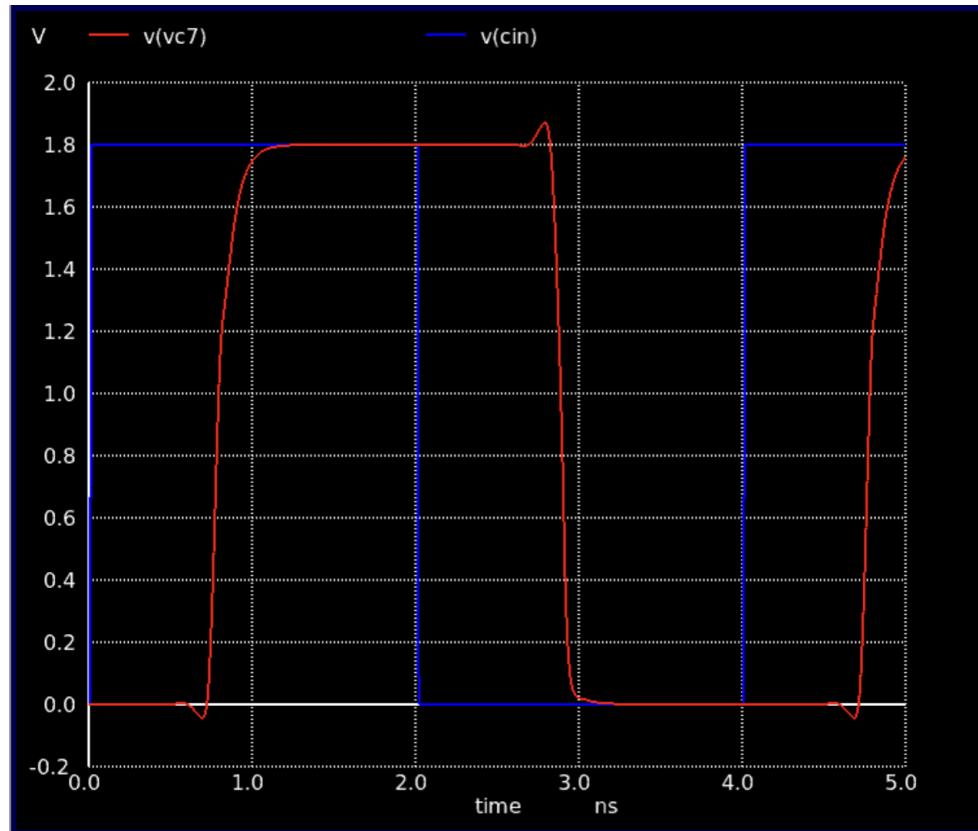
Layout:

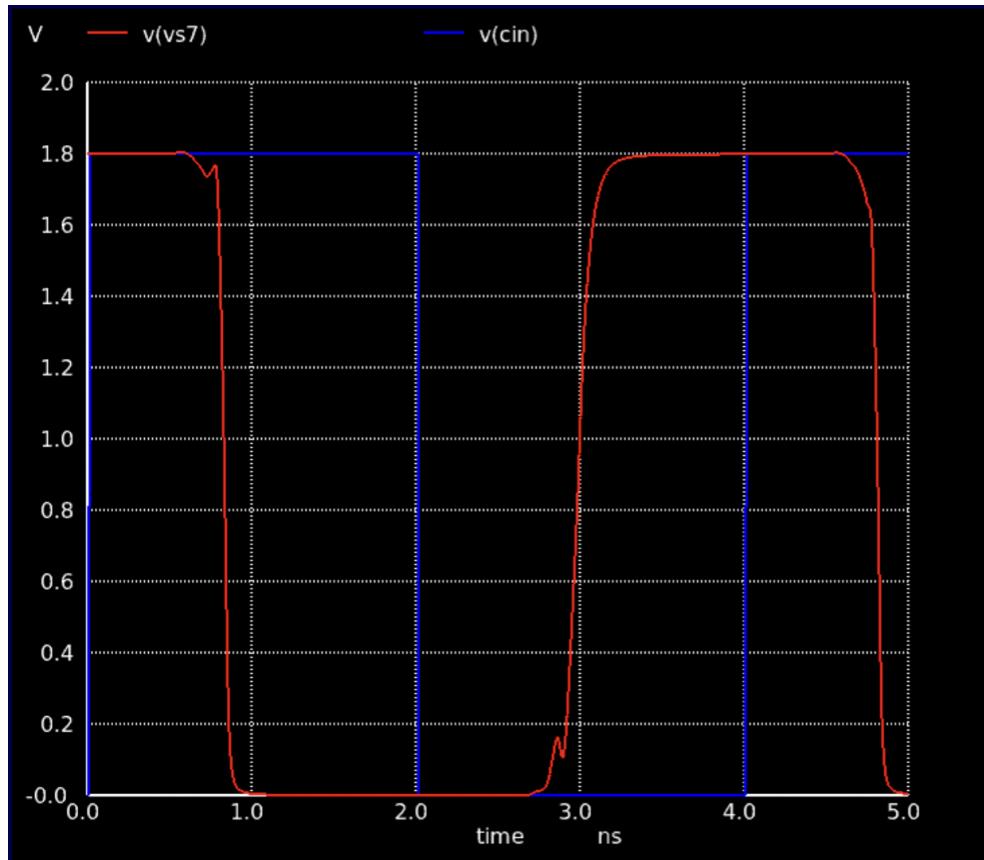


Width = 24.74um, Height = 25.6um, Aspect Ratio = 0.96

Measurements:

Pre-layout Simulation:

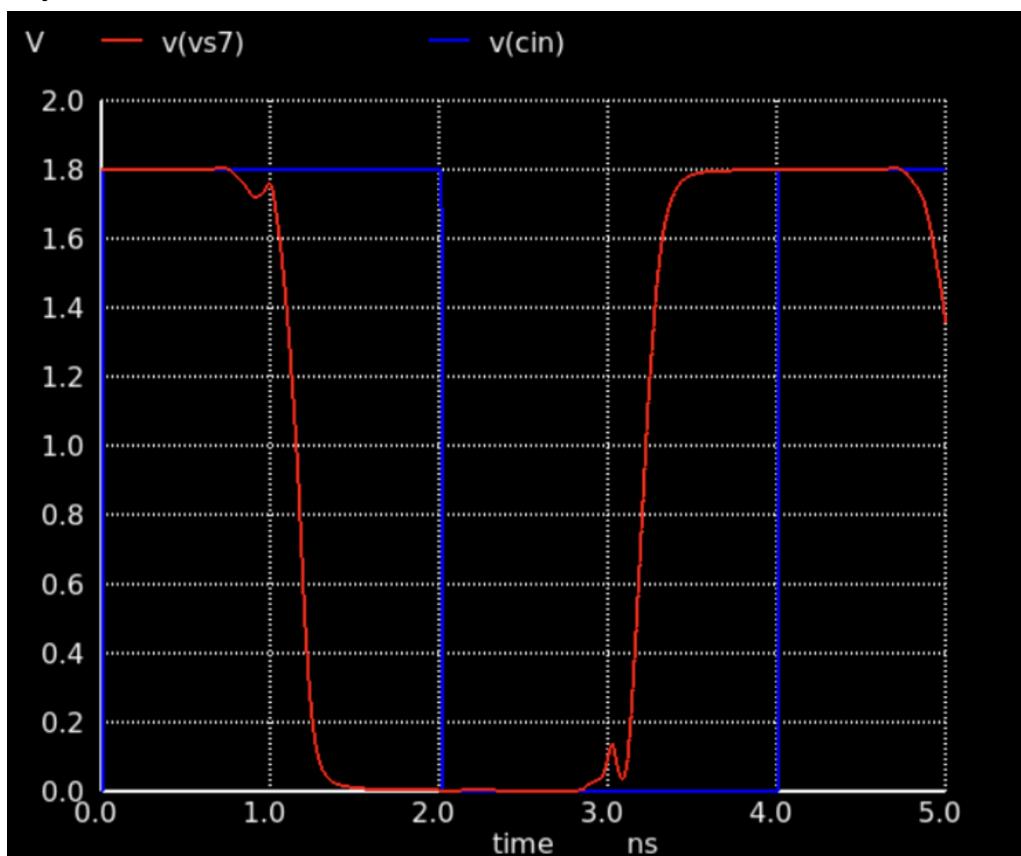


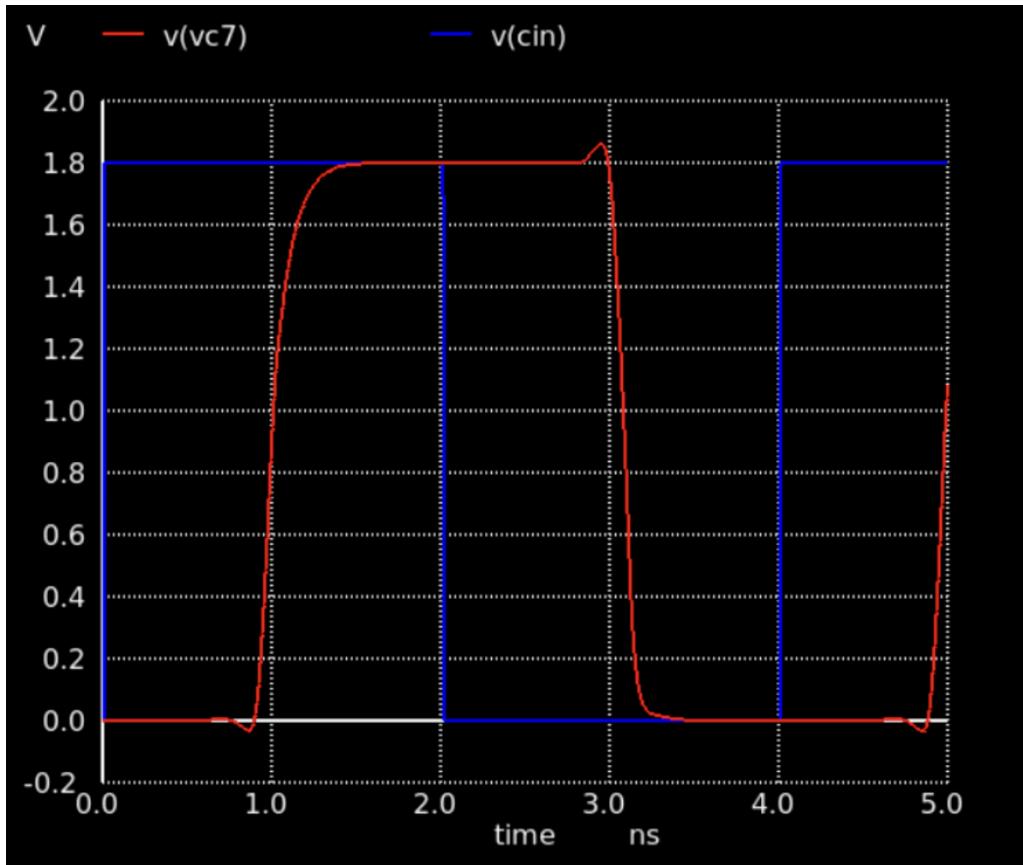


$$d_{1 \text{ to } S7} = 898.71 \text{ ps}$$

$$d_{1 \text{ to } C7} = 827.0 \text{ ps}$$

Post-Layout Simulation:





$$d_{\text{1 to S7}} = 1175 \text{ ps}$$

$$d_{\text{1 to C7}} = 1030 \text{ ps}$$

The difference in the delay values is because of the parasitics added during layout extraction.