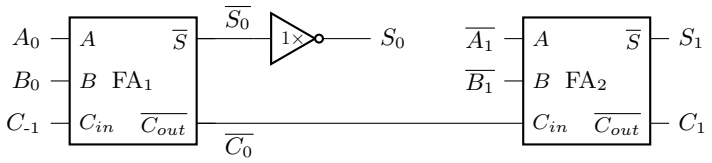
EC 5311 Digital IC Design: Assignment 6
Ripple-carry adder – schematic and layout extracted simulation

1. Draw schematic for the carry and sum logic in a mirror-symmetric full adder done in class. Size the p/nMOS to minimize the delay from input to output carry and the stage effort of the carry logic is four when used in a ripple carry adder. Create a symbol for the full adder and connect two full adders as shown below:



   (a) Measure the delays: (i) from C_{-1} to $\overline{C_0}$, and (ii) from C_{-1} to $\overline{S_0}$.

   (b) How do the measured delays compare against that estimated using logical and electrical effort?

   (c) Draw the layout for the full-adder and measure the layout extracted delay and compare it against the pre-layout delay. Use diffusion sharing and num fingers to create a compact layout. The height of the full adder should be the same as the inverter in Assignment 5.

2. Draw the schematic of a 8-bit ripple-carry adder using the above mirror-symmetric full adder and trace its critical path.

   (a) Measure the delay of the critical path if the MSB sum and carry bits (S_7, C_7) drive a unit inverter each.

   (b) Compare the measured delay with the delay estimated using logical/electrical/branching effort.

   (c) Draw the layout of the complete ripple-carry adder using the above full-adder layout and inverter layout from Assignment 5. Ensure that aspect ratio (width/height) of your layout is in the range $[0.9, 1.1]$. Measure the layout extracted delay and compare it with the pre-layout delay.