EC 5311 Digital IC Design: Assignment 9
Synthesis and STA

1 Synthesis using Yosys

- Input: Verilog netlist
- Output: Synthesised and library mapped gate level netlist
- Example: Full adder with clocked inputs

```
// full adder with clocked inputs and outputs
module fa(output reg sum, output reg cout, input a, input b, input cin, input clk);
// Q pins of D-flipflop
reg a_q, b_q, cin_q;
// sum and carry logic of full adder
assign sum_d = a_q ^ b_q ^ cin_q;
assign cout_d = (a_q & b_q) | (b_q & cin_q) | (cin_q & a_q);
// register input and outputs with posedge of clock
always @(posedge clk)
begin
    a_q <= a;
    b_q <= b;
    cin_q <= cin;
    sum <= sum_d;
    cout <= cout_d;
end
endmodule
```

- Invoke Yosys shell using the command: `yosys`
- Execute the following commands:

```
# Read the tt liberty file
read_liberty -lib /cad/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
# Read the input Verilog
read_verilog fa.v
# synthesize the top module
synth -top fa
# lib map the combinational cells
abc -liberty /cad/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
# lib map the seqeuential cells
dfflibmap -liberty /cad/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
# write the synthesized gate-level netlist
write_verilog -noattr fa_synth.v
# optionally visualize the netlist
show
```

2 STA using OpenSTA

- Invoke OpenSTA shell using the command: `sta`
- Execute the following commands:

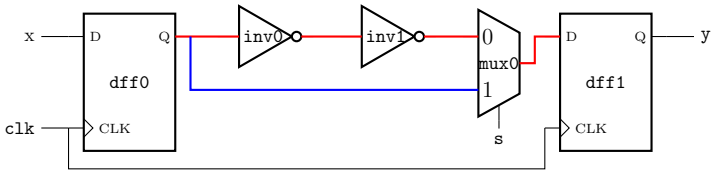
```
# Read the tt liberty file
read_liberty /cad/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
# Read the synthesized gate-level netlist
read_verilog fa_synth.v
# Set the top module
link_design fa
# Create a clock with the required time period
create_clock -name clk -period 3 {clk}
# Report critical paths for setup and hold violations
report_checks -path_delay max
```

3 False paths in STA

A path in the circuit that is not exercised by any input or is redundant during operation is a false path.

3.1 Example

In the below example, upon ignoring the interconnect delays, the red path implements the same logic and is always slower than the blue path. The red path is an example of a false path. Such a path can be excluded during STA using the `set_false_path` command.



3.1.1 Verilog gate-level netlist

Below is the gate-level verilog netlist of the above circuit using Sky130 standard cells:

```
module example(output y, input x, s, clk);
  wire xinv, x_q, xbuf, y_d;
  sky130_fd_sc_hd__dfxtp_1 dff0(.CLK(clk), .D(x), .Q(x_q));
  sky130_fd_sc_hd__inv_1   inv0(.A(x_q),  .Y(xinv));
  sky130_fd_sc_hd__inv_1   inv1(.A(xinv), .Y(xbuf));
  sky130_fd_sc_hd__mux2_1  mux0(.A0(x_q), .A1(xbuf), .S(s), .X(y_d));
  sky130_fd_sc_hd__dfxtp_1 dff1(.CLK(clk), .D(y_d), .Q(y));
endmodule
```

3.1.2 False path specification

The command `set_false_path` is used to specify the false paths. The `-through` argument indicates all paths that pass through the vertex are marked as false paths. Below commands specify specification:

```
read_liberty /cad/share/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
read_verilog ex.v
link_design example
create_clock -name clk -period 0.67 clk
report_checks -path_delay max
# set all paths passing through xbuf as false paths
set_false_path -through xbuf
report_checks -path_delay max
```

3.1.3 STA report showing the false path

Before specifying the false path, STA reports the red critical path:

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ dff0/CLK (sky130_fd_sc_hd__dfxtp_1)
   0.28    0.28 v dff0/Q (sky130_fd_sc_hd__dfxtp_1)
   0.04    0.32 ^ inv0/Y (sky130_fd_sc_hd__inv_1)
   0.03    0.35 v inv1/Y (sky130_fd_sc_hd__inv_1)
   0.27    0.62 v mux0/X (sky130_fd_sc_hd__mux2_1)
   0.00    0.62 v dff1/D (sky130_fd_sc_hd__dfxtp_1)
           0.62   data arrival time

   0.67    0.67   clock clk (rise edge)
   0.00    0.67   clock network delay (ideal)
   0.00    0.67   clock reconvergence pessimism
           0.67 ^ dff1/CLK (sky130_fd_sc_hd__dfxtp_1)
  -0.12    0.55   library setup time
           0.55   data required time
---------------------------------------------------------
           0.55   data required time
          -0.62   data arrival time
---------------------------------------------------------
          -0.07   slack (VIOLATED)
```

3.1.4 STA report excluding the false path

After specifying the false path, STA ignores the red path and reports the blue critical path:

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ dff0/CLK (sky130_fd_sc_hd__dfxtp_1)
   0.28    0.28 v dff0/Q (sky130_fd_sc_hd__dfxtp_1)
   0.26    0.54 v mux0/X (sky130_fd_sc_hd__mux2_1)
   0.00    0.54 v dff1/D (sky130_fd_sc_hd__dfxtp_1)
           0.54   data arrival time

   0.67    0.67   clock clk (rise edge)
   0.00    0.67   clock network delay (ideal)
   0.00    0.67   clock reconvergence pessimism
           0.67 ^ dff1/CLK (sky130_fd_sc_hd__dfxtp_1)
  -0.12    0.55   library setup time
           0.55   data required time
---------------------------------------------------------
           0.55   data required time
          -0.54   data arrival time
---------------------------------------------------------
           0.01   slack (MET)
```