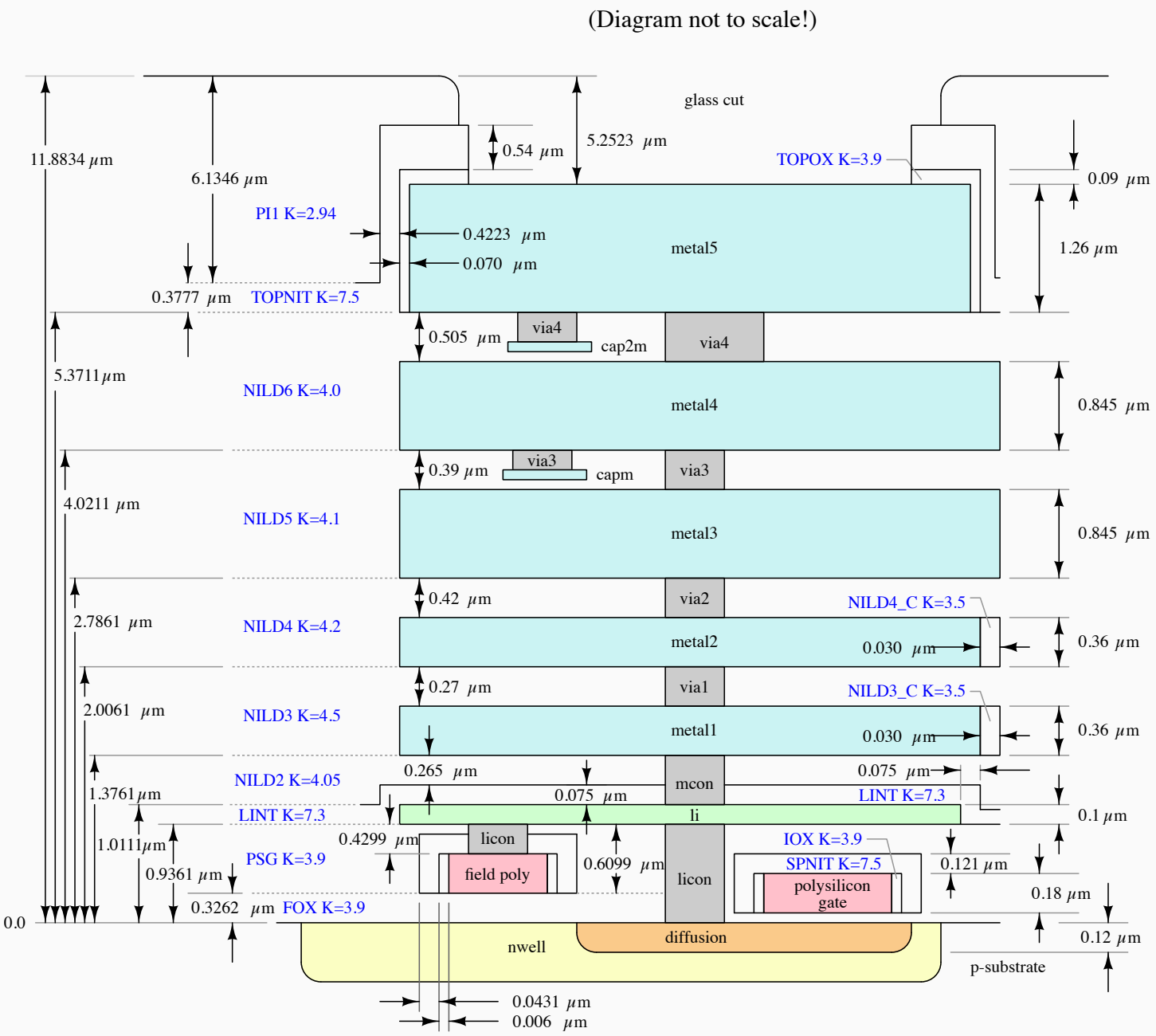
EE5311: Digital IC Design

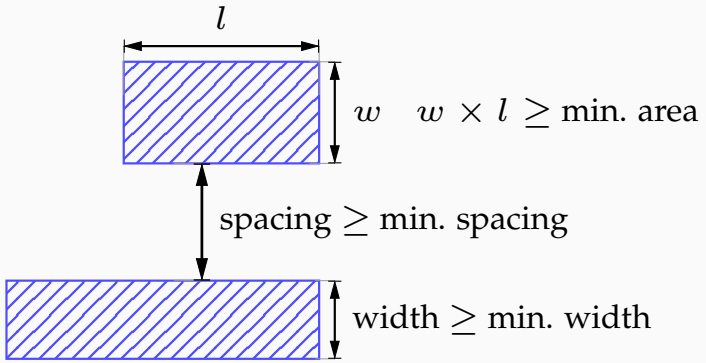
Tutorial 5 - Inverter layout and post-layout simulation

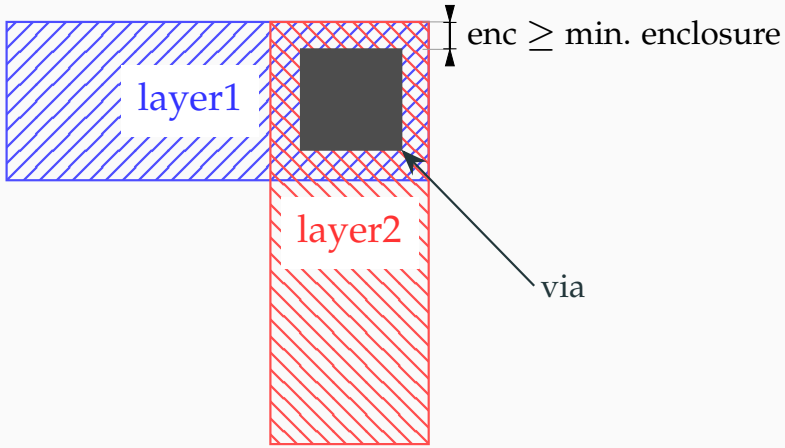
Skywater 130nm layer stack



Layout Rules - Rudimentary Design Rule Checks (DRC)

- Basic DRCs that will get you an *almost* DRC clean layout:





- Exhaustive list of DRCs:
  https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html

Layers and DRCs

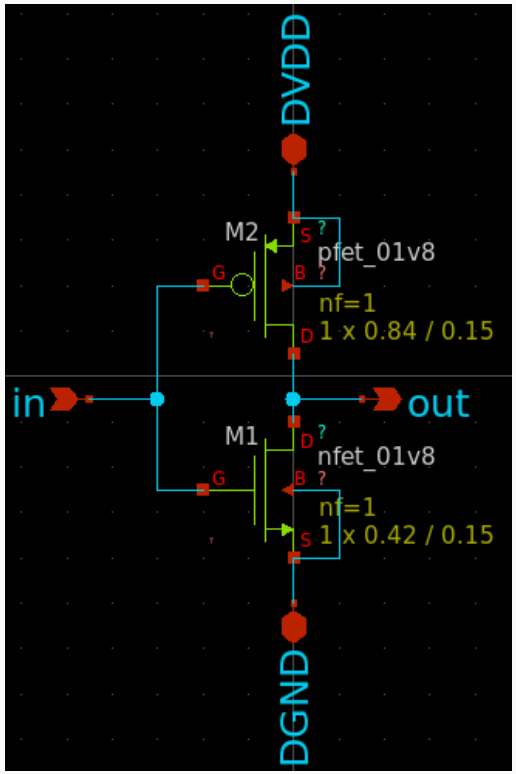
PDK layer	KLayout layer	Purpose	Min. width (µm)	Min. spac-ing (µm)	Min. area (μm^2)
nwell	nwell.drawing	N-well for pMOS	0.84	1.27	–
diffusion	diff.drawing	Source/Drain diffusion for n/p-MOS	0.15	0.27	0.265(n) 0.255(p)
polysilicon	poly.drawing	Polysilicon gate	0.15	0.21	–
licon	licon1.drawing	via between diff/poly li	0.17	0.17	–
li	li1.drawing	local interconnect	0.17	0.17	0.0561
mcon	mcon.drawing	via between li and metal1	0.17	0.19	–
metal1	met1.drawing	Metal-1 routing layer	0.14	0.14	0.083
via1	via.drawing	via between metal1 and metal2	0.15	0.17	–
metal2	met2.drawing	Metal-2 routing layer	0.14	0.14	0.0676
via2	via.drawing	via between metal2 and metal3	0.20	0.20	–
metal3	met3.drawing	Metal-3 routing layer	0.30	0.30	0.240
via3	via.drawing	via between metal3 and metal4	0.20	0.20	–
metal4	met4.drawing	Metal-4 routing layer	0.30	0.30	0.240
via4	via.drawing	via between metal4 and metal5	0.80	0.80	–
metal5	met5.drawing	Metal-5 routing layer	1.60	1.60	4.000

Layers and DRCs ...

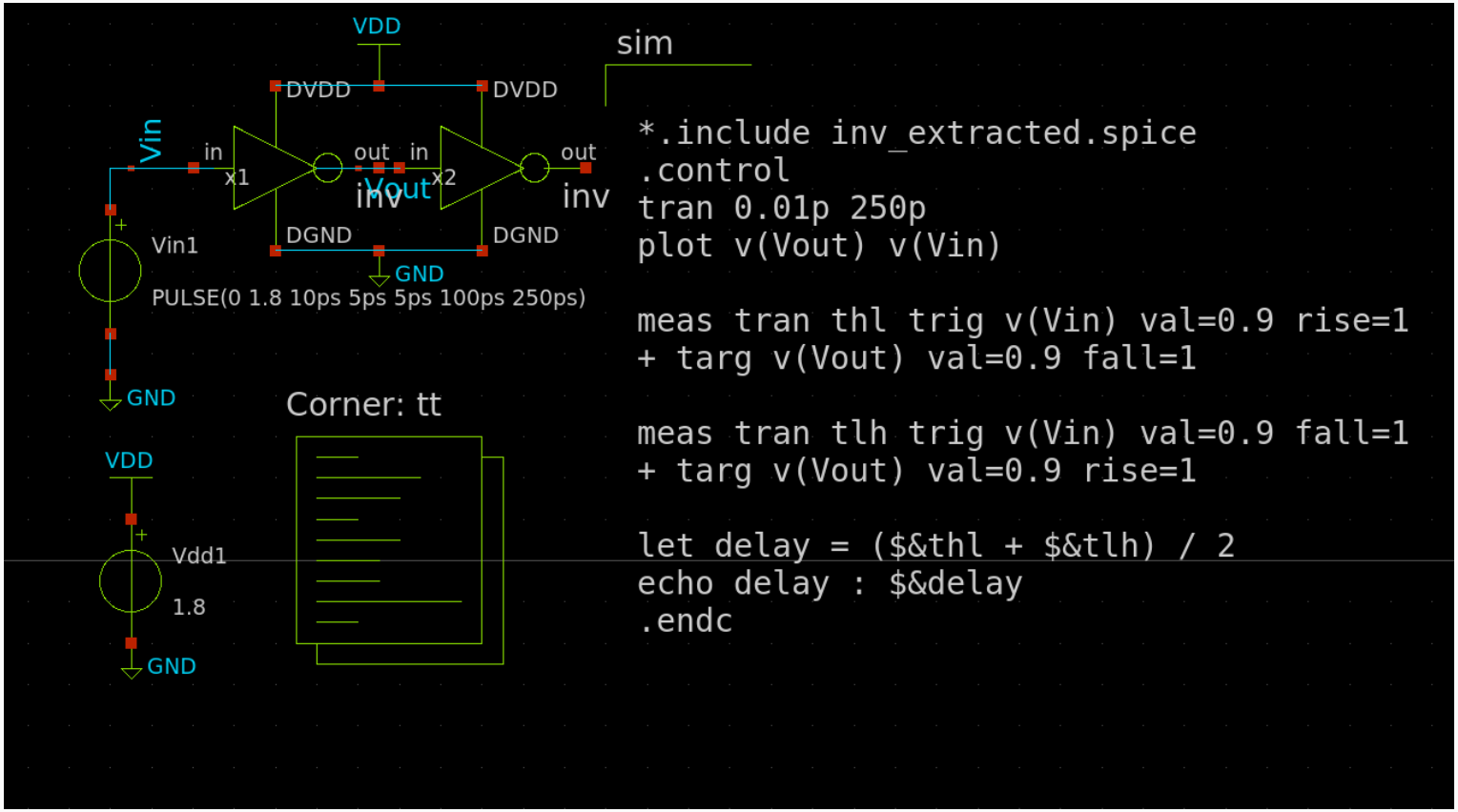
Via layer	Adjacent layer	Min. enclosure (µm) (values on the adjacent edges of the enclosing metal)
licon	diffusion	0.06/0.06
licon	poly	0.05/0.08
licon	li	0.08/0.08
mcon	li	0.00/0.00
mcon	metal1	0.03/0.06
via1	metal1	0.055/0.085
via1	metal2	0.055/0.085
via2	metal2	0.040/0.085
via2	metal3	0.065/0.065
via3	metal3	0.06/0.09
via3	metal4	0.065/0.065
via4	metal4	0.19/0.19
via4	metal5	0.31/0.31

Inverter schematic

- Use the `pfet_01v8` and `nfet_01v8` devices to construct an inverter as shown below
- Use `DVDD` and `DGND` signals to connect to p/nMOS bulk and source terminals instead of the global `VDD` and `GND` signals.



Measure delay of the inverter



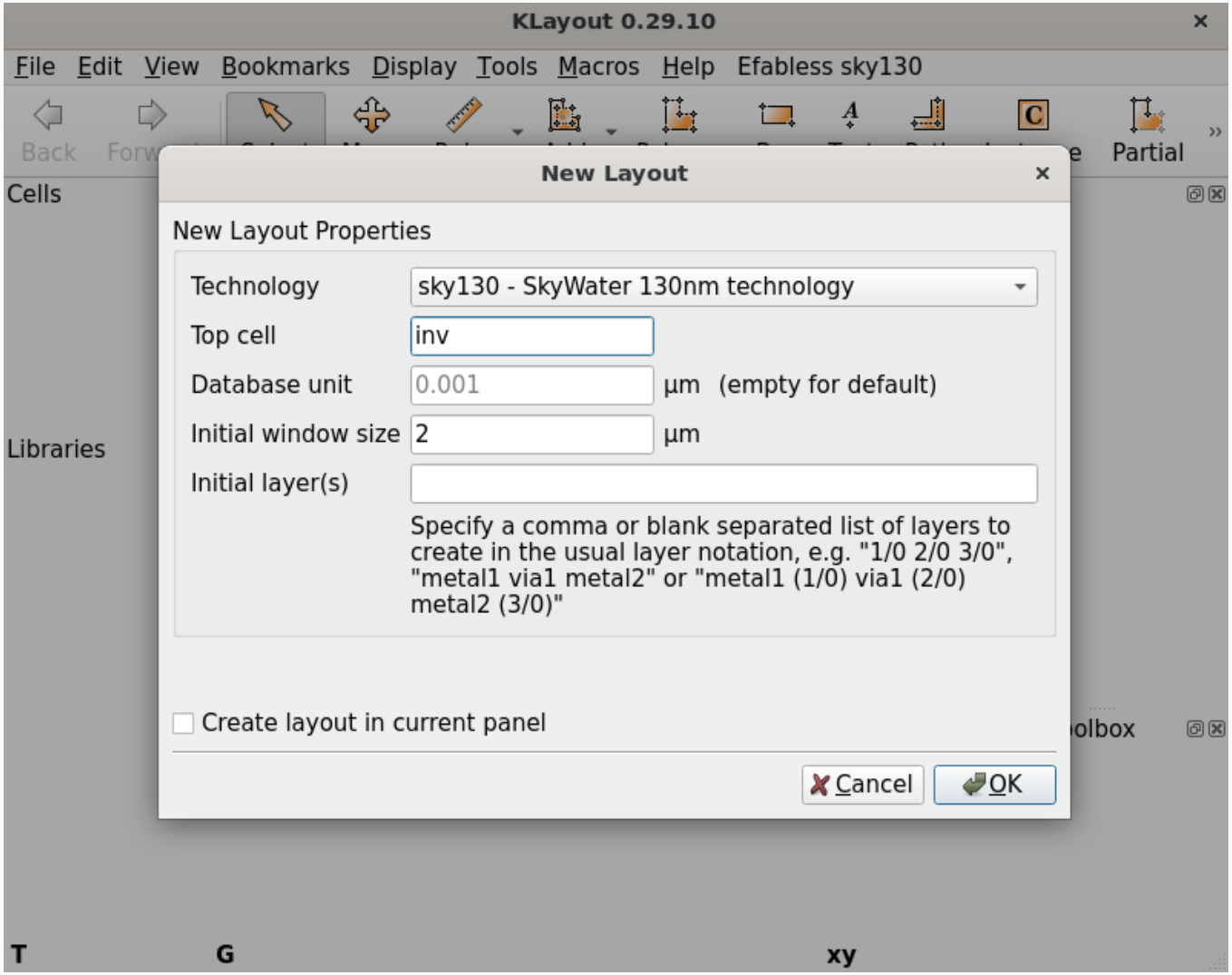
KLayout - setup, invocation and shortcuts

- Before invoking `klayout` for the first time execute the command `source /cad/setup/layout_init.sh`. *Execute this only once.*
- Invoke klayout in edit mode using: `klayout -e`
- Shortcuts:

Function	Shortcut
Create an instance	`i`
Create a box on the selected layer	`b`
Stretch an edge of a polygon/rectangle	`s`
Select an object	`Left mouse click`
Move	`m`
Copy	`c`
Paste interactively	`p`
Insert a label	`l`
Draw ruler	`k`
Clear rulers	`Ctrl k`
Object properties	`q`
Save layout	`Ctrl s`
View all hierarchy	`*`
Undo	`Ctrl z`
Redo	`Ctrl y`

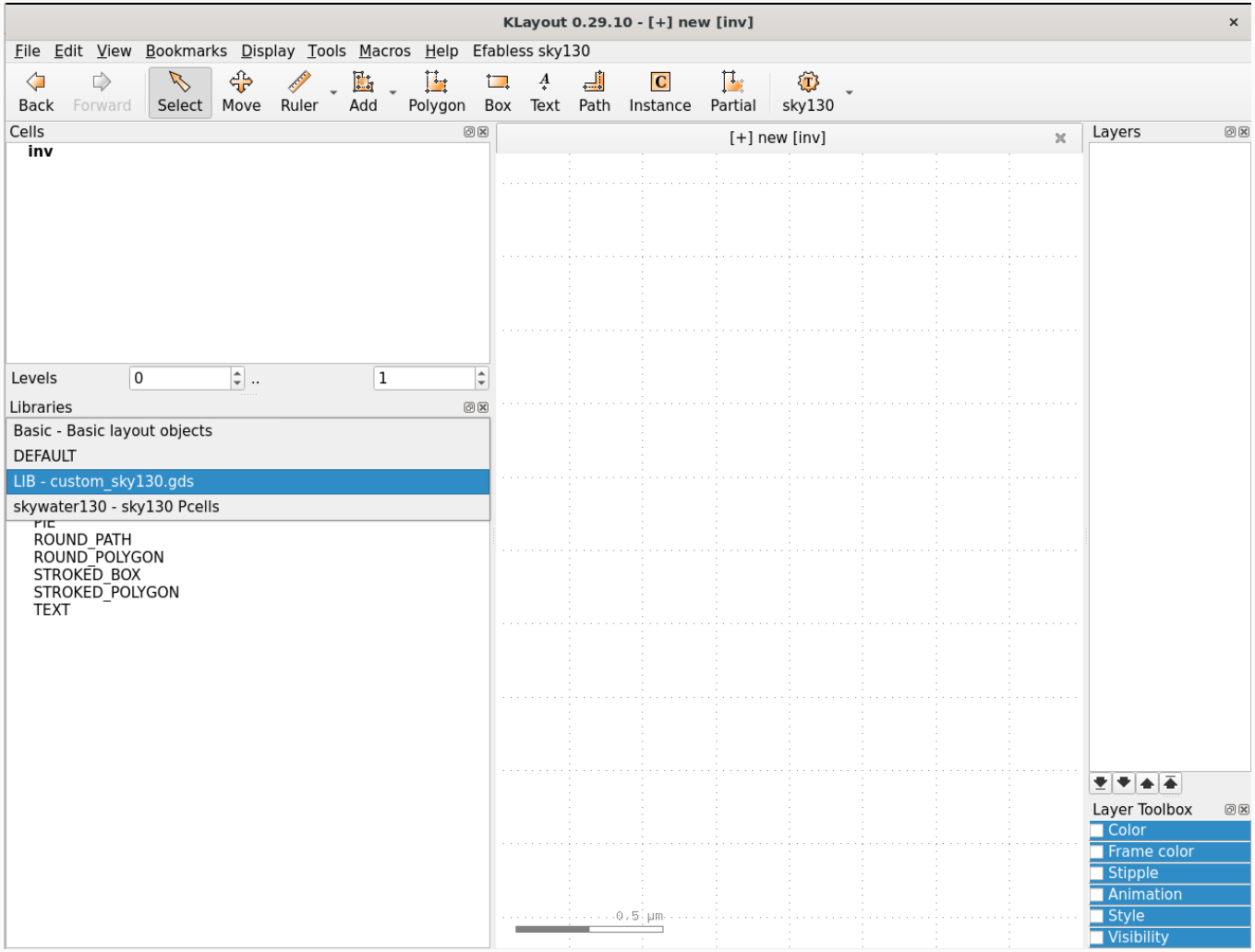
New layout

- Create a new layout in KLayout using `File` ▶ `New layout`
- Name the top cell as `inv` as shown below



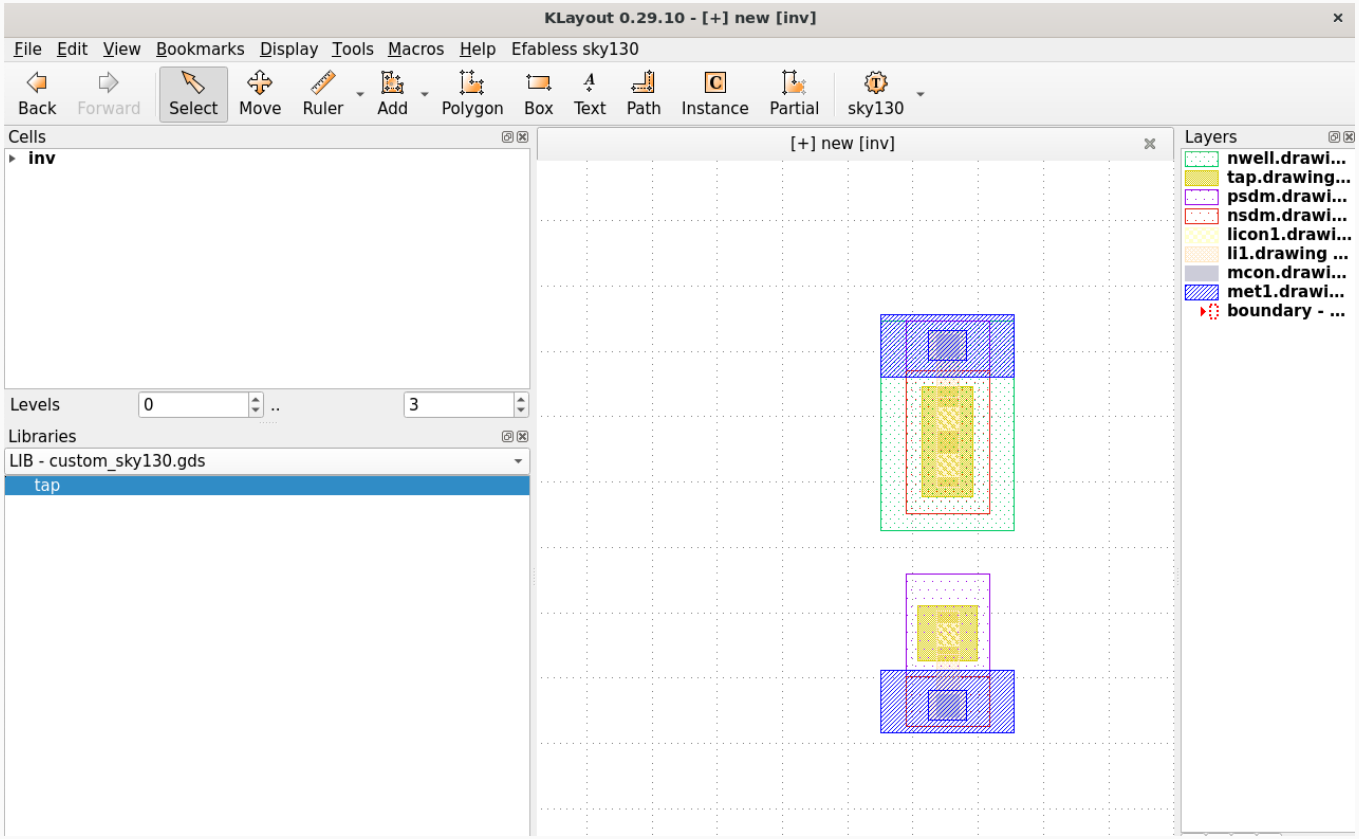
Select tap

- Choose the `custom_sky130.gds` in the `Libraries` list as below:



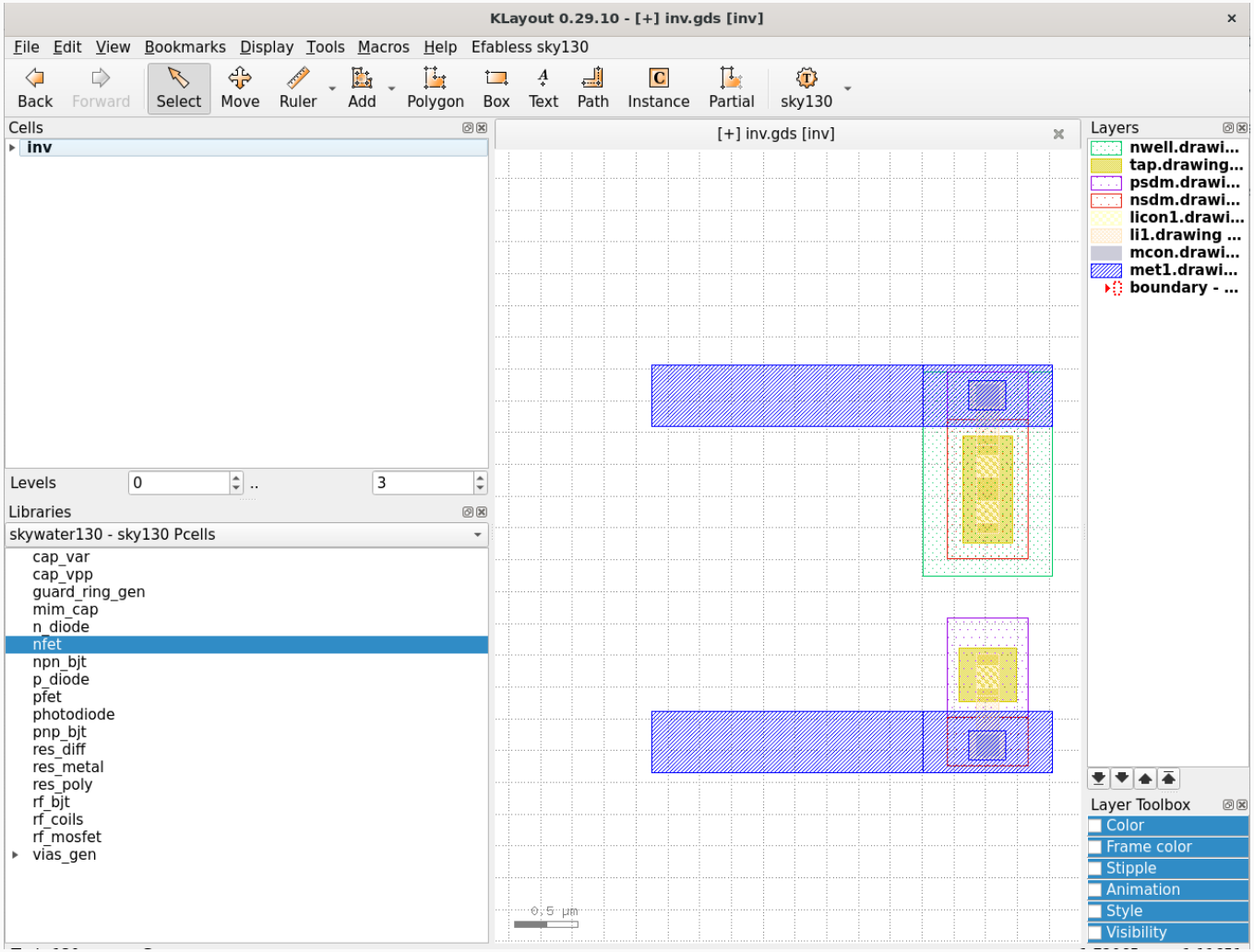
Insert tap

- Insert the `tap` cell by dragging and dropping it onto the canvas
- Press `*` to show the contents of tap cell
- Top and bottom `met1.drawing` shapes connect the `nWell` and `pSubstrate` to the `DVDD` and `DGND` signals respectively
- The tap cell serves as the reference height for your standard cells



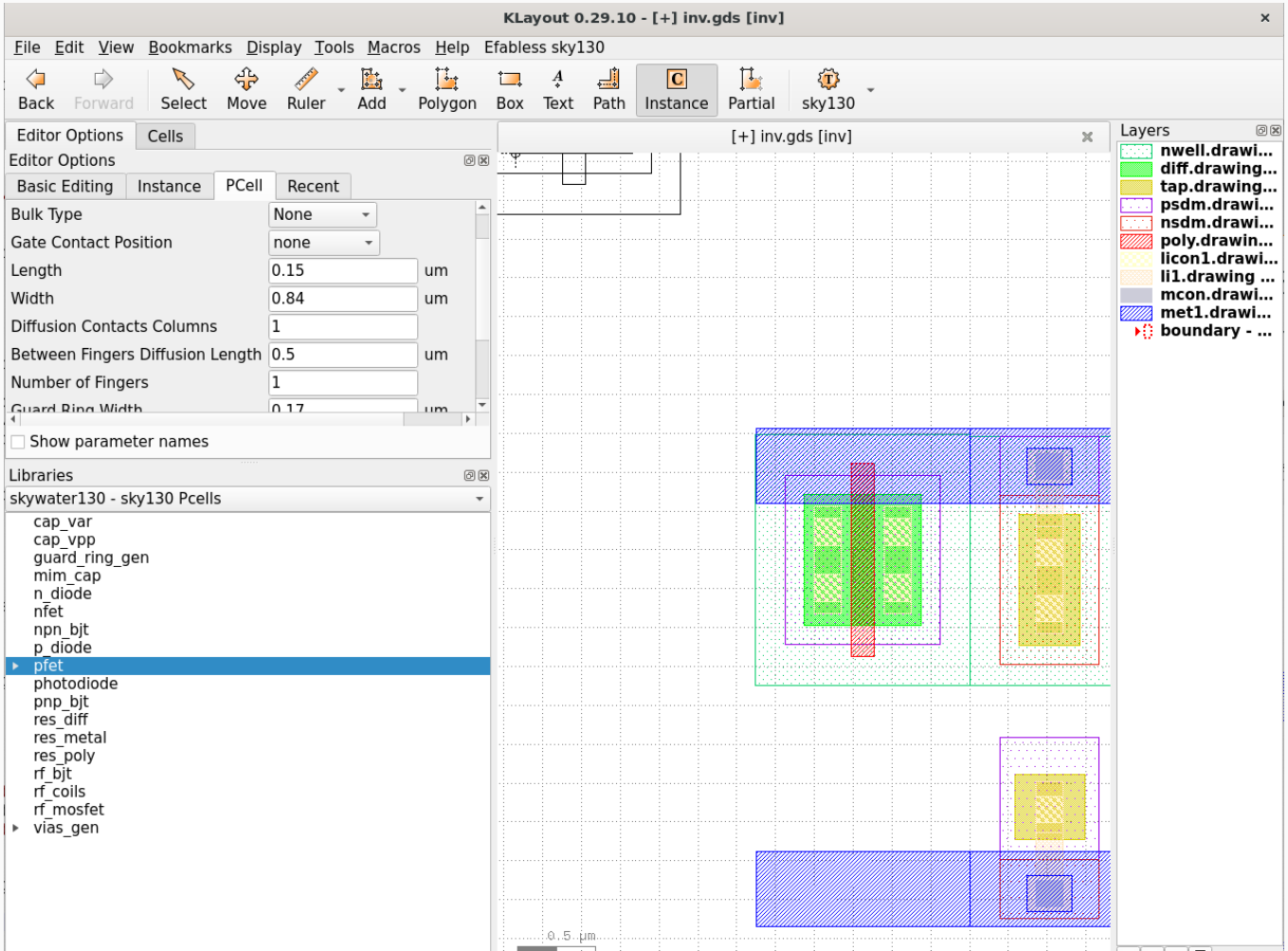
Extend power lines

- Extend the power and ground lines by drawing boxes on `met1.drawing` layer using the shortcut key: `b`



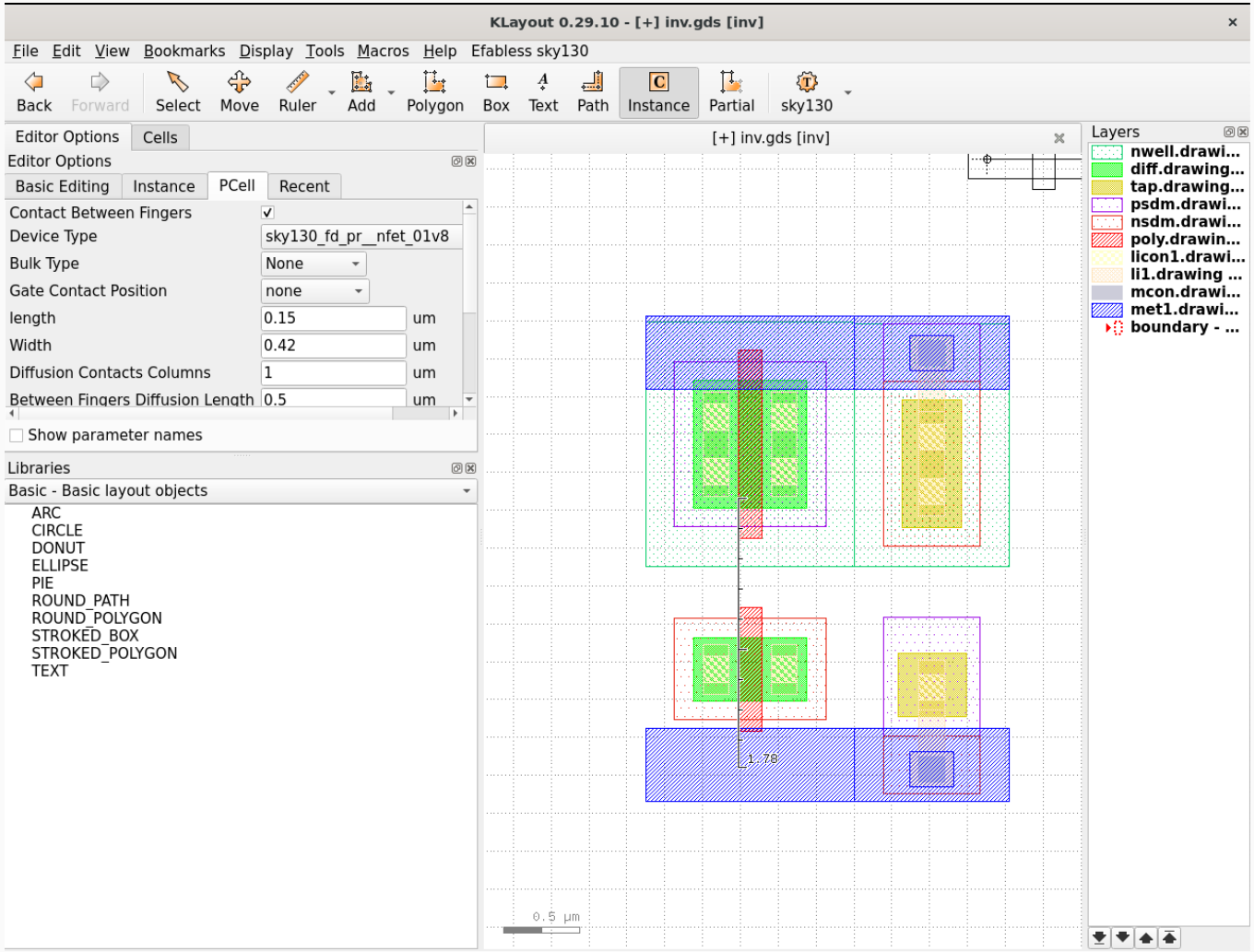
Insert pfet

- Switch to the sky130 Pcells library in the `Libraries` list
- Insert a `pfet` by dragging and dropping it on canvas
- Modify the `PCell` parameters `width = 0.84`
- Insert the `pfet` such that its `nwell` abuts the `nwell` of `tap`



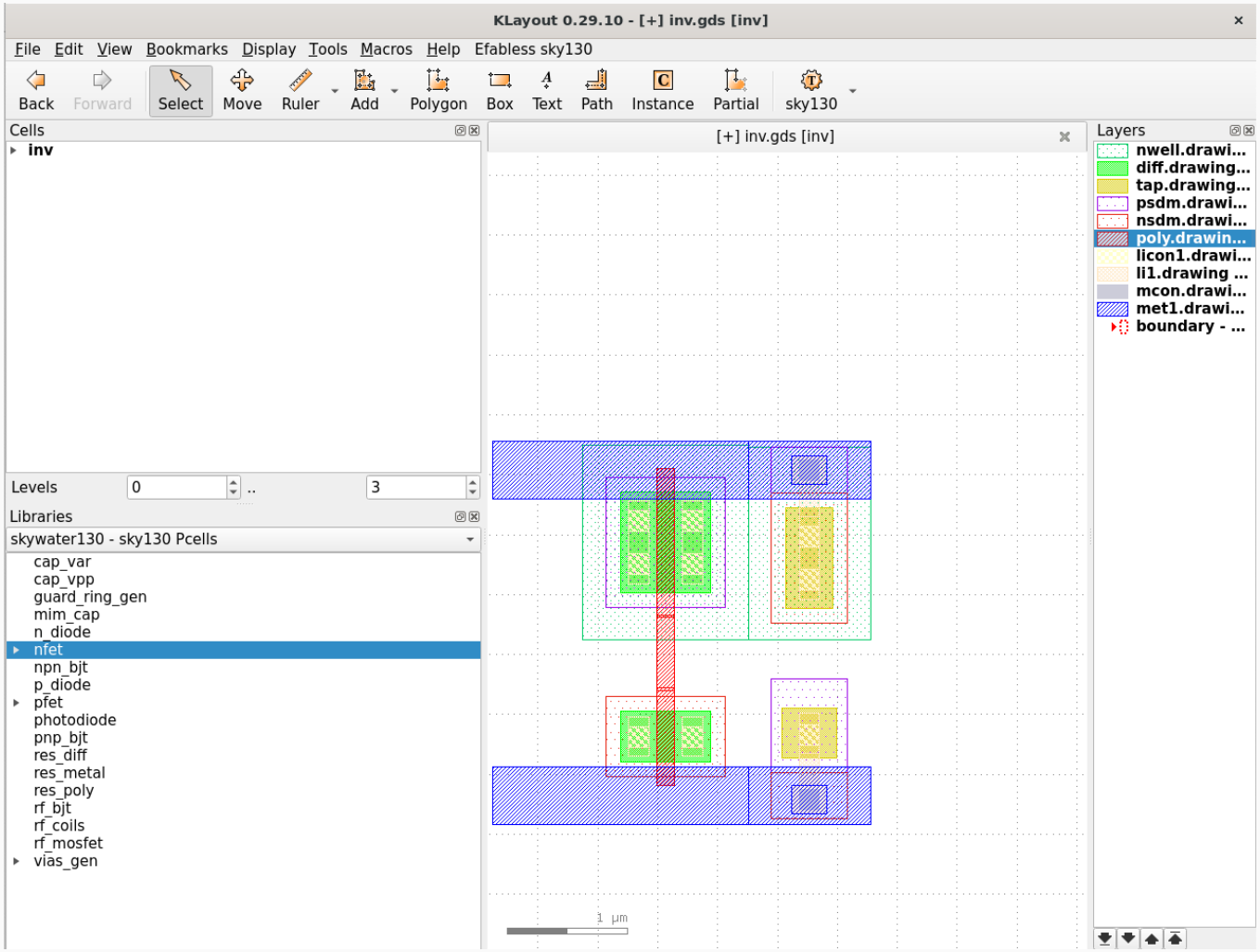
Insert nfet

- Insert a `nfet` by dragging and dropping it on canvas
- Insert the `nfet` such that its `poly` aligns with that of `pfet`
- Use the ruler (shortcut `k`) to align the polys



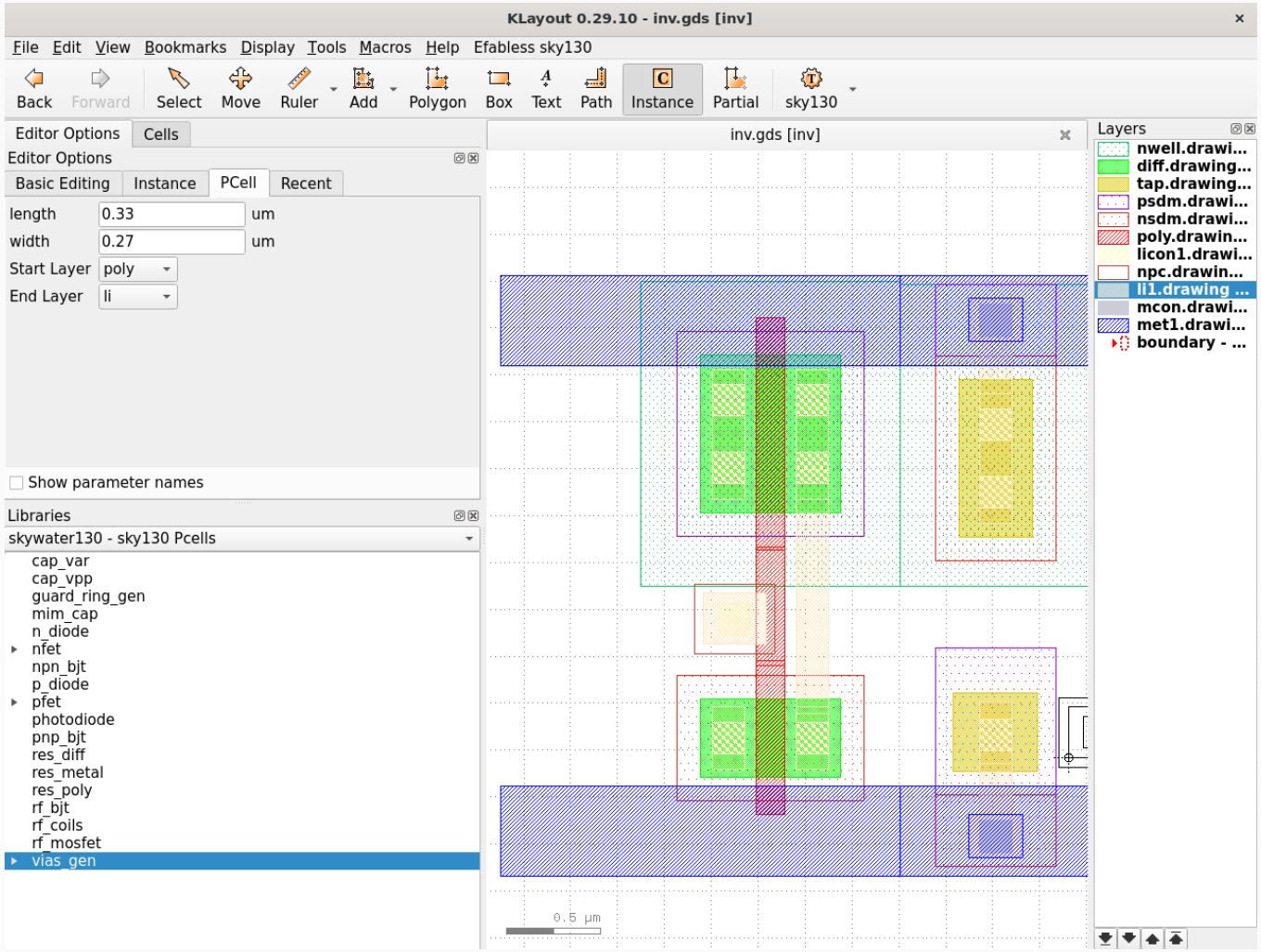
Connect polys

- Connect the `nfet` and `pfet` polys using a box on the `poly.drawing` layer (shortcut: `b`)



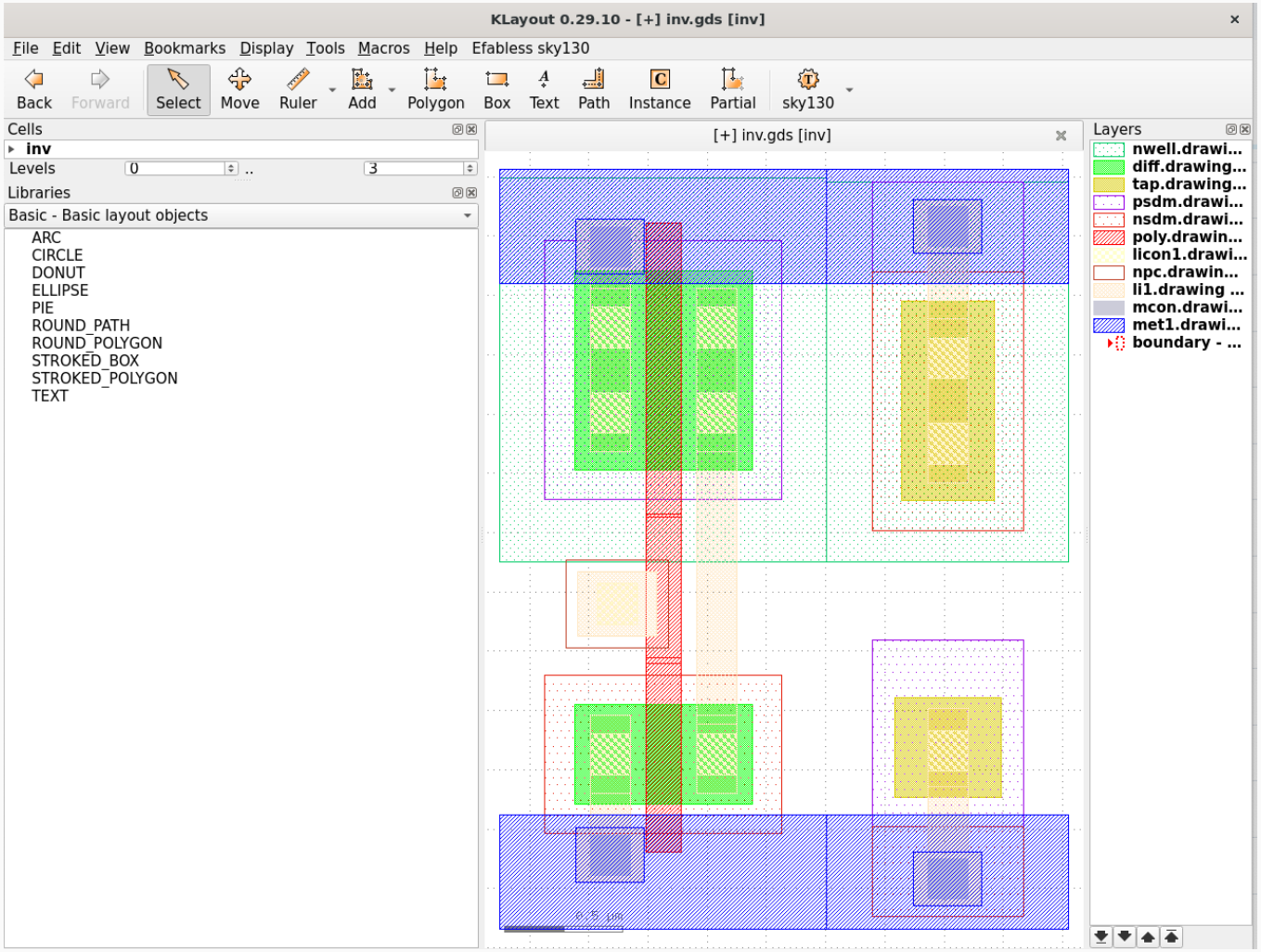
Connect drains

- Connect the `nfet` and `pfet` drains using a box on the `li1.drawing` layer (shortcut: `b`)
- Insert a via from the `poly` to `li` using the `Pcell vias_gen`



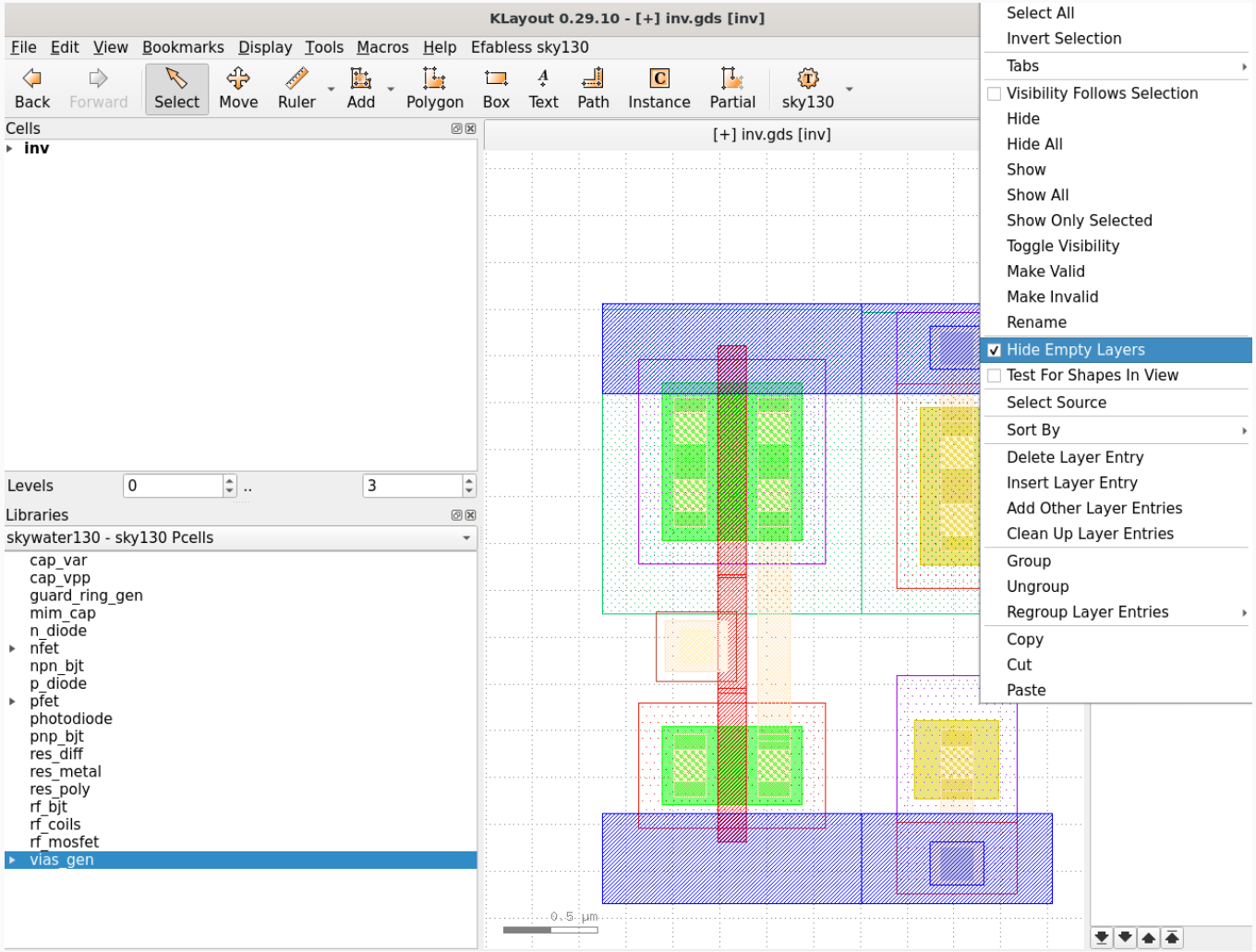
Connect sources to power and ground

- Connect `pfet` source to the top `metal1` using a box on the `li1` layer and a via from the `li` to `metal1` using the `vias_gen`
- Connect `nfet` source to the bottom `metal1` similarly



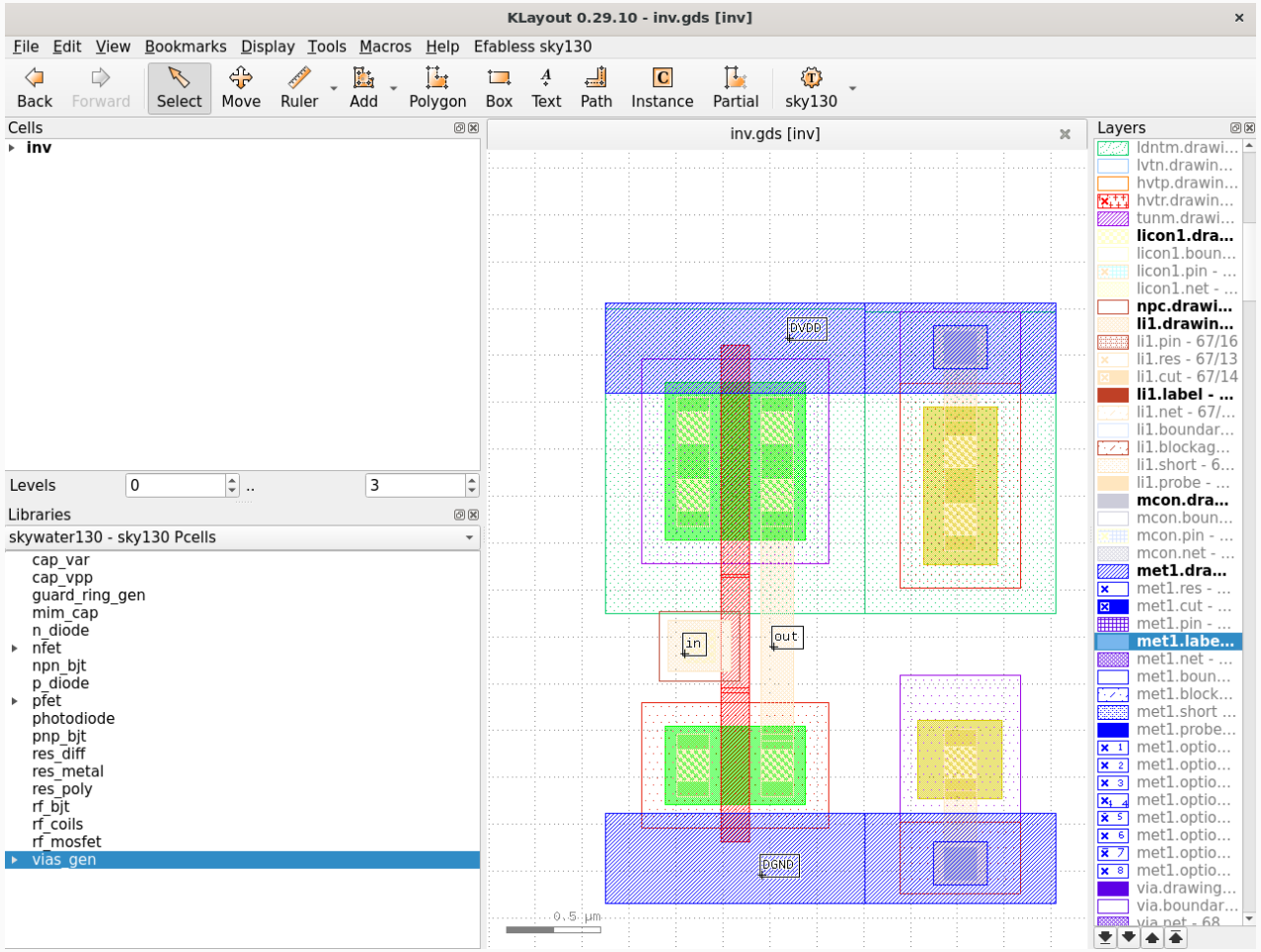
Unhide empty layers

- Unhide the empty layers by right clicking on the layers box and unchecking the checkbox shown below:



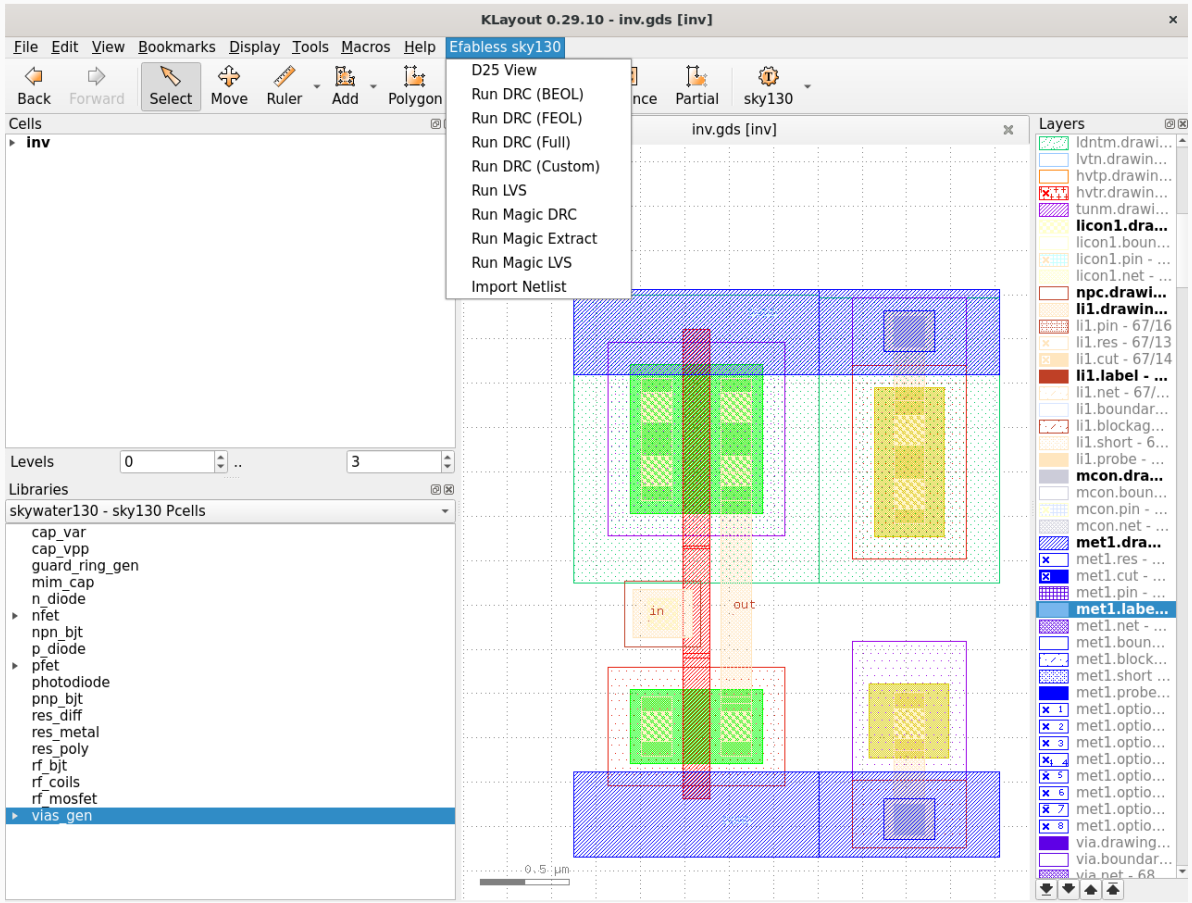
Insert labels

- Insert the labels `in` and `out` on the `li1.label` layer on the poly and diffusion contacts respectively (shortcut: `l`)
- Insert the labels `DVDD` and `DGND` on the `met1.label` layer on the top and bottom `met1` drawings.



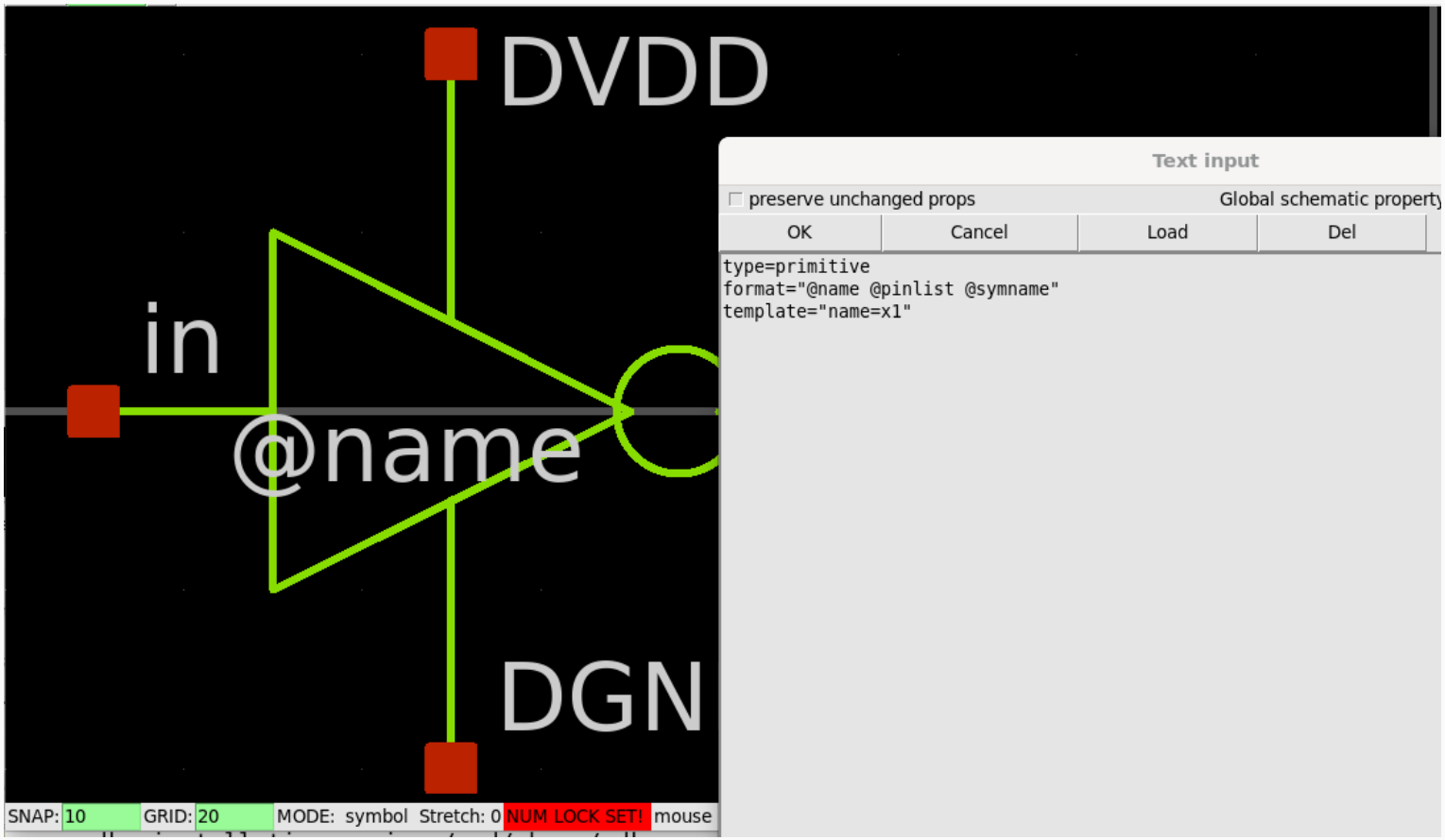
DRC, LVS and Extraction

- Run DRC using: `Efabless sky130 ▶ Run Magic DRC`
- Run LVS using: `Efabless sky130 ▶ Run Magic LVS`
- If you get any DRC/LVS errors fix them until there are none.
- Run Extract using: `Efabless sky130 ▶ Run Magic Extract`
- Post layout extracted netlist will be saved as: `inv_extracted.spice`



Post-layout simulation: Modify inverter symbol

To prevent `xschem` from netlisting the inverter, modify the symbol type from subcircuit to primitive as shown below:



Post-layout simulation: Measure delay of the inverter

Include the extracted netlist as shown below and find the delay of the inverter post-layout.