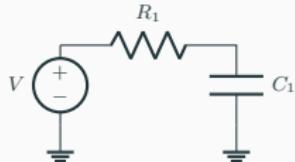


EE5311: Digital IC Design

Tutorial 1

ngspice setup

- To first ensure you have a working setup, try simulating a toy RC circuit:



- Save the equivalent SPICE netlist for the above circuit as `demo.spice`:

```
.title demo
V1 in GND dc 0 PULSE (0 5 1u 1u 1u 1 1)
R1 in out 10k
C1 out GND 1u
.tran 10u 50m
.end
```

- Load the netlist onto ngspice using: `ngspice demo.spice`
- Simulate the transient response of the RC circuit using the command `run` inside the ngspice shell
- Plot the voltage waveforms using: `plot v(in) v(out)`

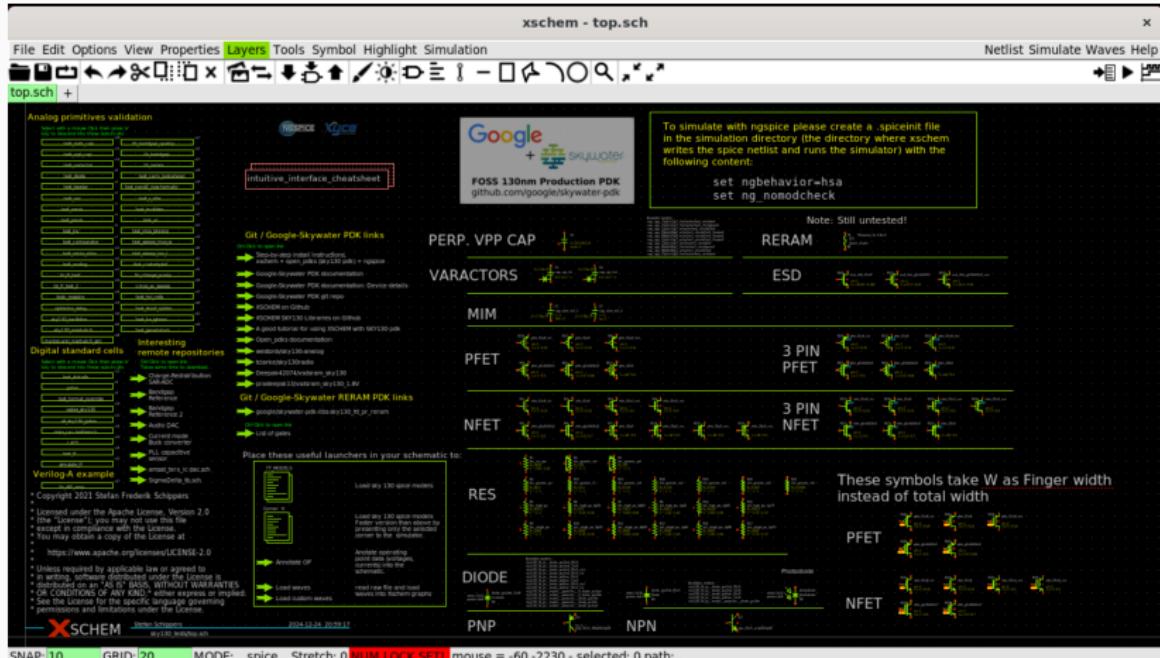
xschem setup

- Execute the script below **before you invoke xschem for the first time:**
`source /cad/setup/init.sh.`
- This script enables creation of schematic using Sky130 components.
- Create a directory ee5311 and organize all your tutorials in this directory
- For the first tutorial, create a separate directory, navigate into it and invoke xschem:

```
mkdir -p ${HOME}/ee5311/tutorial_1  
cd ${HOME}/ee5311/tutorial_1  
xschem
```

- If you get the error can't read "PDK_ROOT", use the command:
`export PDK_ROOT=/cad/share/pdk`

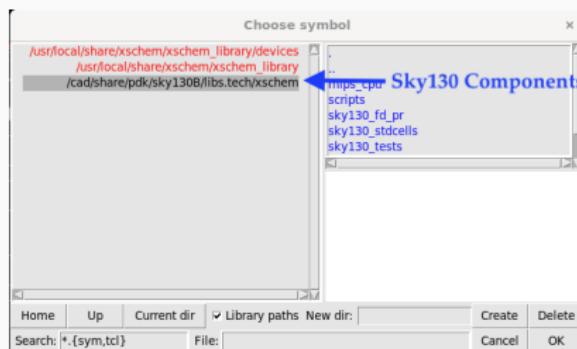
xschem front screen



Experiment 1

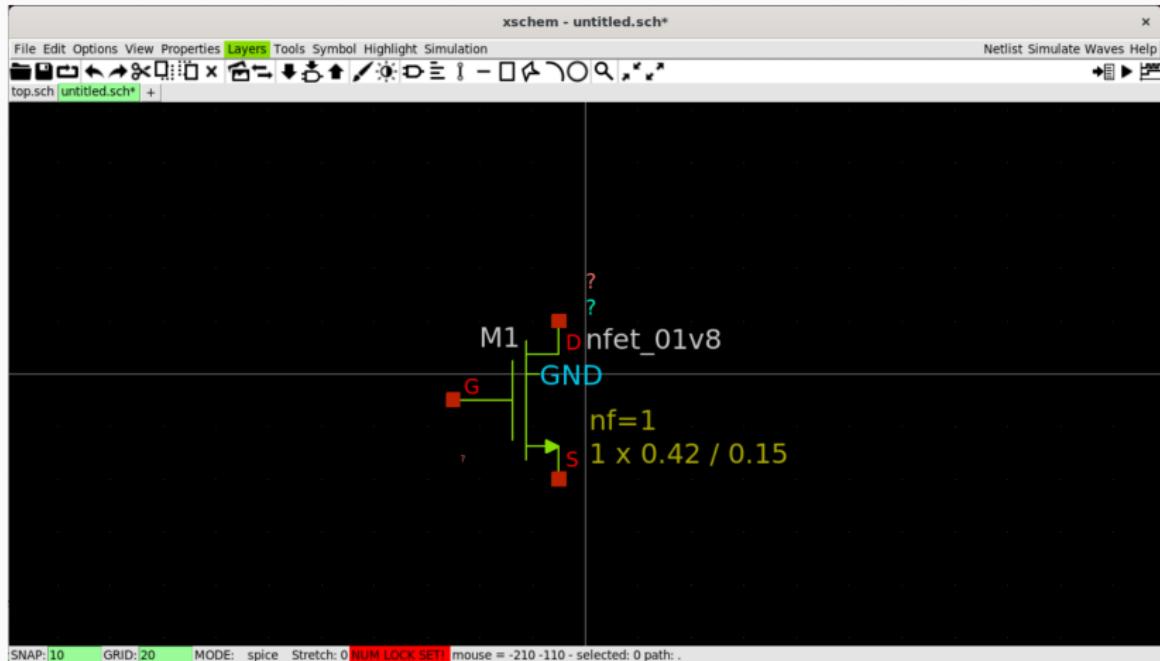
Plot I_{DS} vs V_{GS} for an nMOS $\left(\frac{W}{L} = \frac{0.42\mu m}{0.15\mu m}\right)$ with $V_{DS} = V_{GS}$ varied from 0 to V_{DD}

- Create new schematic
- Insert a new instance using the keys: Shift + I
- Choose nMOS instance from:
xschem ► sky130_fd_pr ► nfet3_01v8



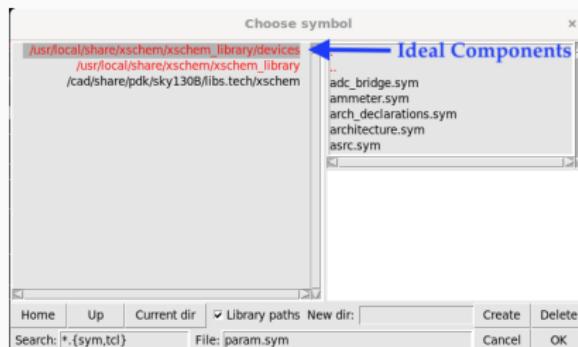
- Change the width of nMOS to $0.42\mu m$ by selecting it with left mouse click followed by the key q

Experiment 1...



Experiment 1...

- Insert GND pin at the source terminal of the nMOS using :
xschem_library ► devices ► gnd



- Insert a pin with label Vin at the gate terminal of nMOS using:
xschem_library ► devices ► lab_pin
Alt + R rotates the label.
- Connect the drain and gate terminals with a wire using the w key.
Change direction of wire using w or Space key.

Experiment 1...

- Create voltage source using:

xschem_library ► devices ► vsource

with name=Vin1, value=1.8V and connect it between Vin and GND

- Insert a SPICE code using:

xschem_library ► devices ► code_shown

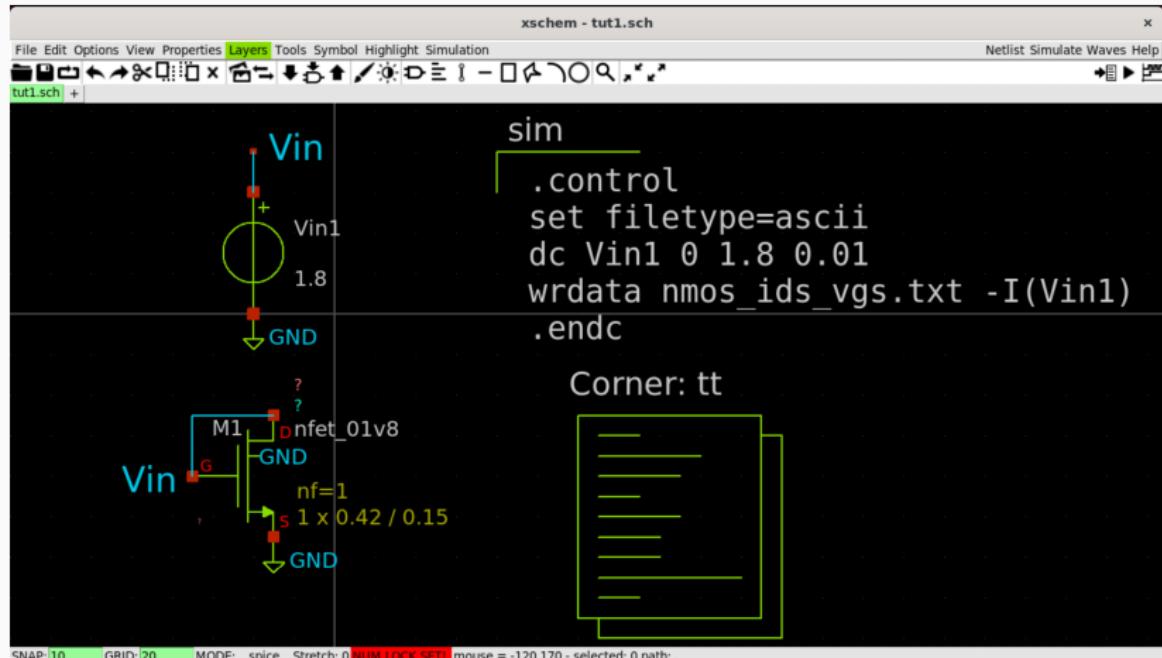
with name=sim and value=

```
".control  
set filetype=ascii  
dc Vin1 0 1.8 0.01  
wrdata nMOS_ids_vgs.txt -I(Vin1)  
.endc"
```

- Insert the simulation corner using:

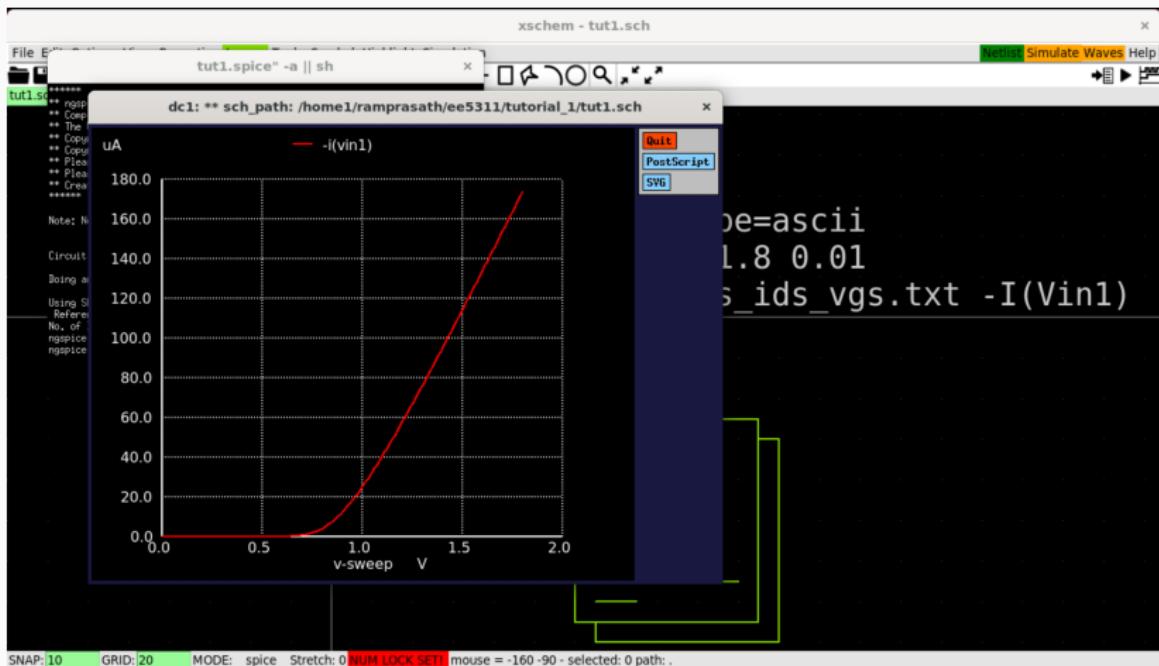
xschem ► sky130_fd_pr ► corner

Experiment 1 - complete schematic



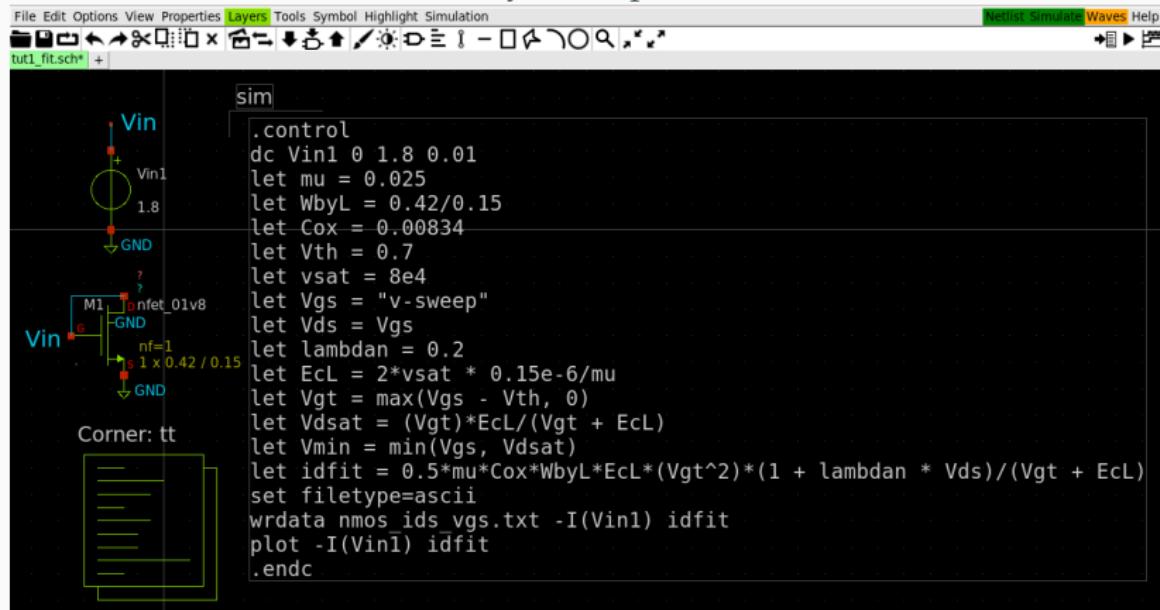
Experiment 1 - xschem I_{DS} vs V_{GS}

- Click Netlist on the top right and then Simulate
- In the ngspice terminal, type: plot -I(Vin1)
- The simulated I_{DS} vs V_{GS} data will be saved in: nmos_ids_vgs.txt
View the contents of the file using: gedit nmos_ids_vgs.txt

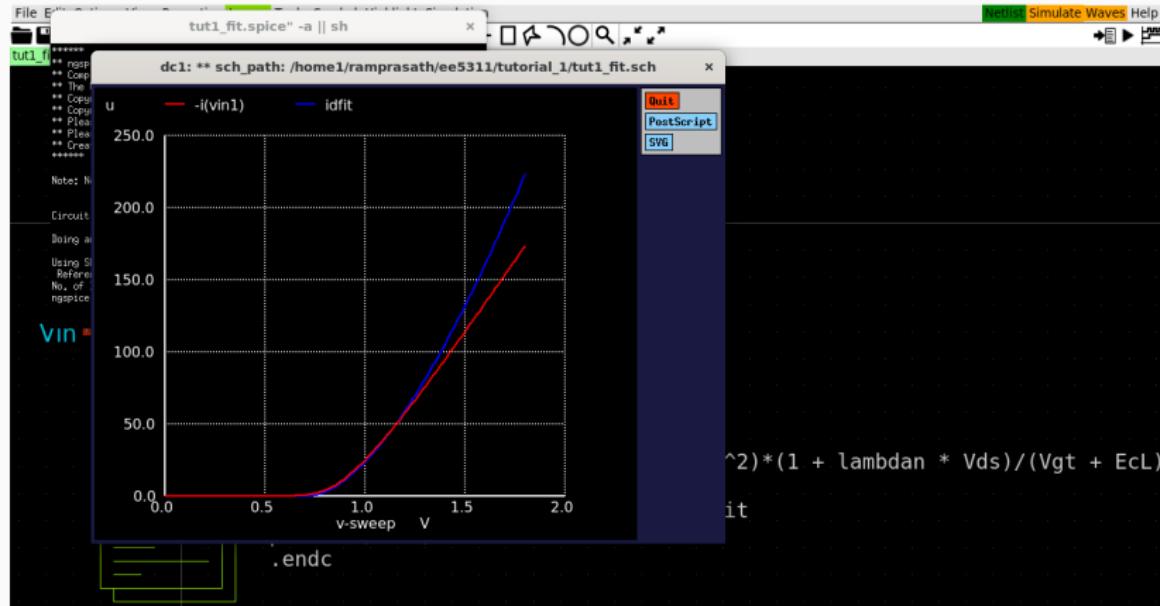


Experiment 1 - xschem I_{DS} , $I_{DS,fit}$ vs V_{GS}

Plot and save the simulated/analytical expressions:

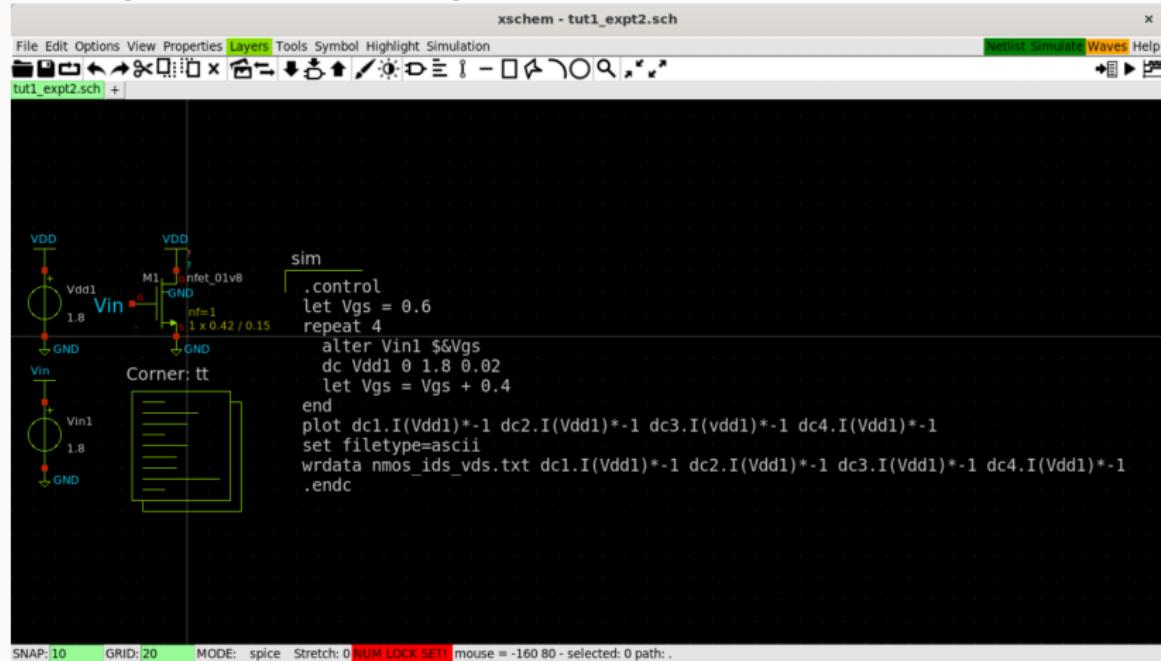


Experiment 1 - xschem I_{DS} , $I_{DS,fit}$ vs V_{GS}



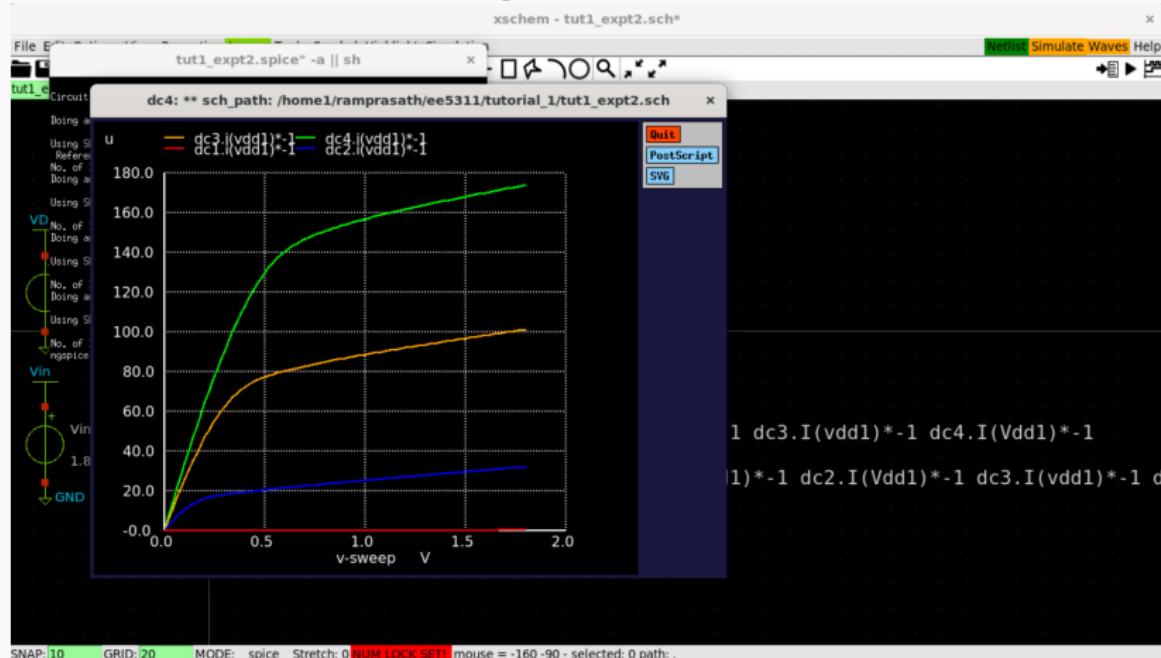
Experiment 2 - I_{DS} vs V_{DS} for different V_{GS}

Plot I_{DS} vs V_{DS} for a unit-sized nMOS $\left(\frac{W}{L} = \frac{0.42\mu m}{0.15\mu m}\right)$ with
 $V_{GS} \in \{0.6V, 1.0V, 1.4V, 1.8V\}$



Experiment 2 - I_{DS} vs V_{DS} for different V_{GS}

The simulated I_{DS} vs V_{DS} data should be in the file: nmos_ids_vds.txt.
View the contents of the file using: gedit nmos_ids_vds.txt



Experiment 3

Simulate the I_{DS} vs V_{DS} for $V_{GS} = V_{DD}$ for transistors of different W/L keeping W/L ratio constant while increasing the width.

The screenshot shows a schematic editor window titled "xschem - tut1_1.sch". The menu bar includes File, Edit, Options, View, Properties, Layers, Tools, Symbol, Highlight, Simulation, Netlist, Simulate, Waves, Help. The toolbar contains icons for selection, zoom, and various tools. A status bar at the bottom shows: SNAP: 10, GRID: 20, MODE: spice, Stretch: 0, NUM LOCK SET!, mouse = -80 210 - selected: 0 path: .

The circuit diagram on the left features two voltage sources: "Vdd1" with a value of 1.8 and "Vin" with a value of 1.8. A MOSFET M1 is connected between the "Vdd1" source and ground. The gate terminal of M1 is connected to the "Vin" source. The drain terminal of M1 is connected to a node labeled "nf=1". The source terminal of M1 is connected to ground. A corner model "Corner: tt" is applied to the M1 component. A simulation script "sim" is displayed on the right:

```
.param Width = 0.42
.param Length = 0.15
.dc Vdd1 0 1.8 0.01
.control
    let index = 1
    set cache =
    while index <= 10
        let newW = index * 0.42
        let newL = index * 0.15
        alterparam Width = $&newW
        alterparam Length = $&newL
        reset
        run
        set cache = ( $cache dc{$&index}.i(VDD1)*-1
        let index = index + 1
    end
.plot $cache
.endc
```

Experiment 3 – simulation output

