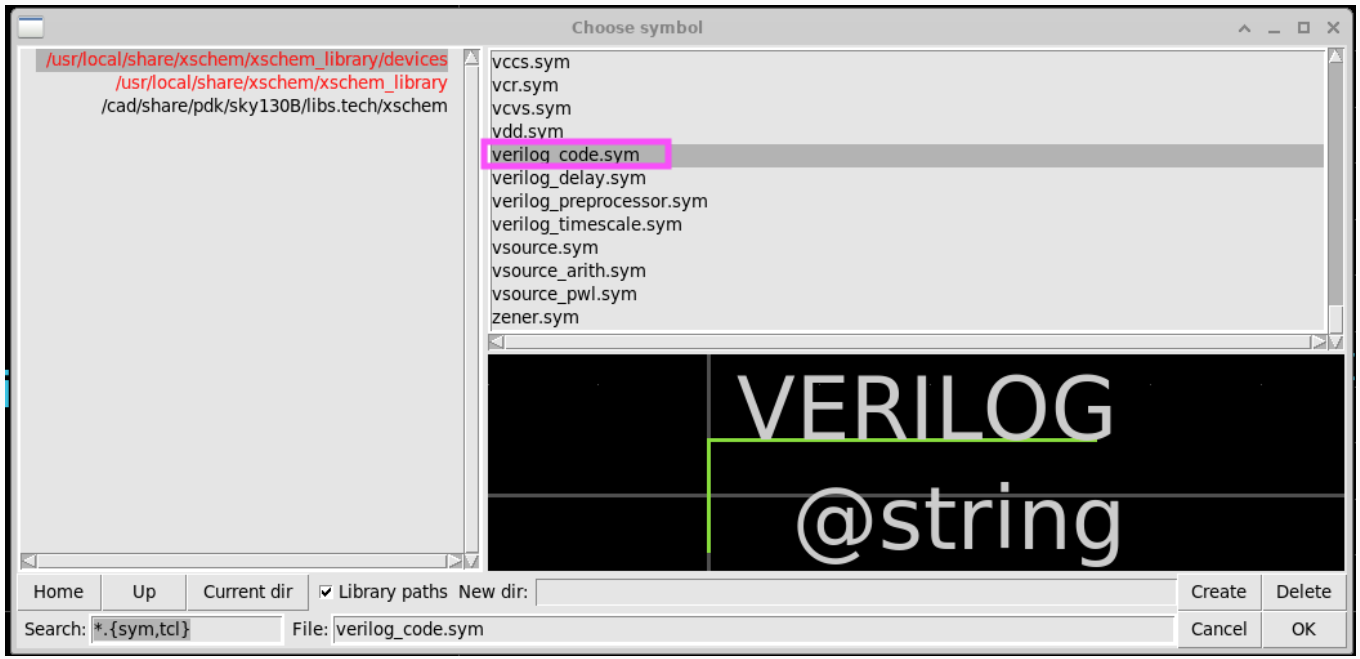
EE5311: Digital IC Design

Tutorial 7

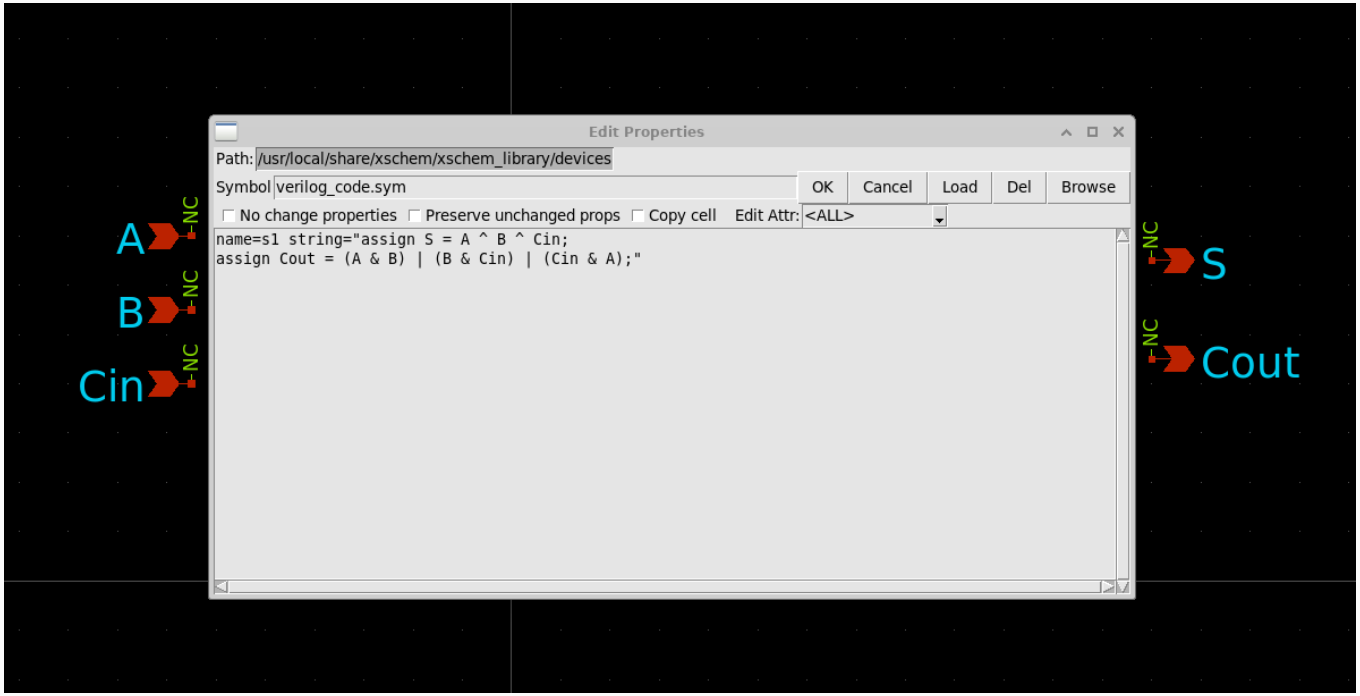
Experiment 7.1

Create a schematic for the full adder verilog module using the `verilog_code` symbol:



Experiment 7.1 - full adder module

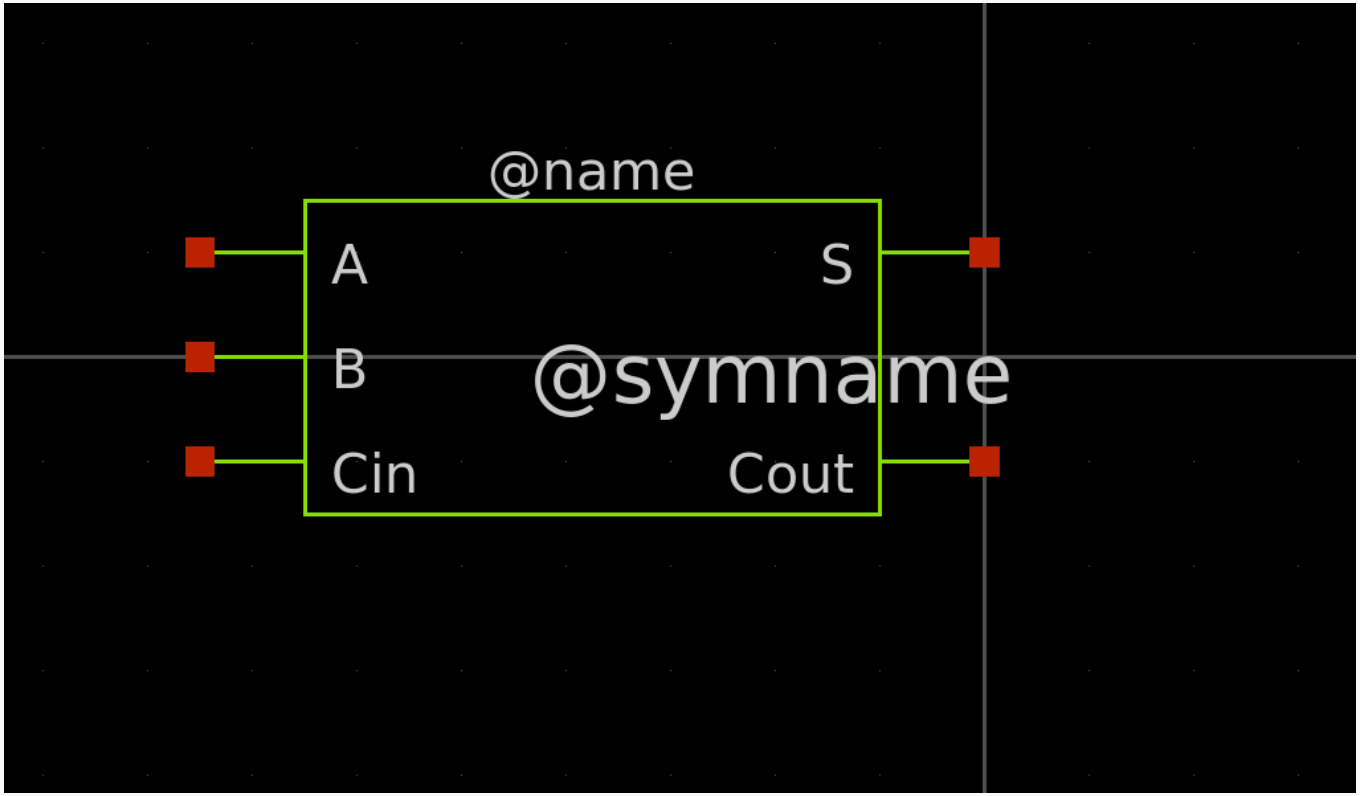
- Populate the verilog code for the full adder:



- Add the input and output ports with the names used in the code
- Connect the ports to `noconn` block to prevent `xschem` from displaying undriven net error

Experiment 7.1 - symbol

- Create a symbol for the full adder block:

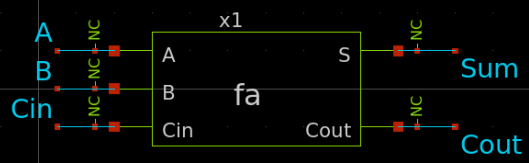


Experiment 7.1 - testbench

- Create a testbench for the full adder as:

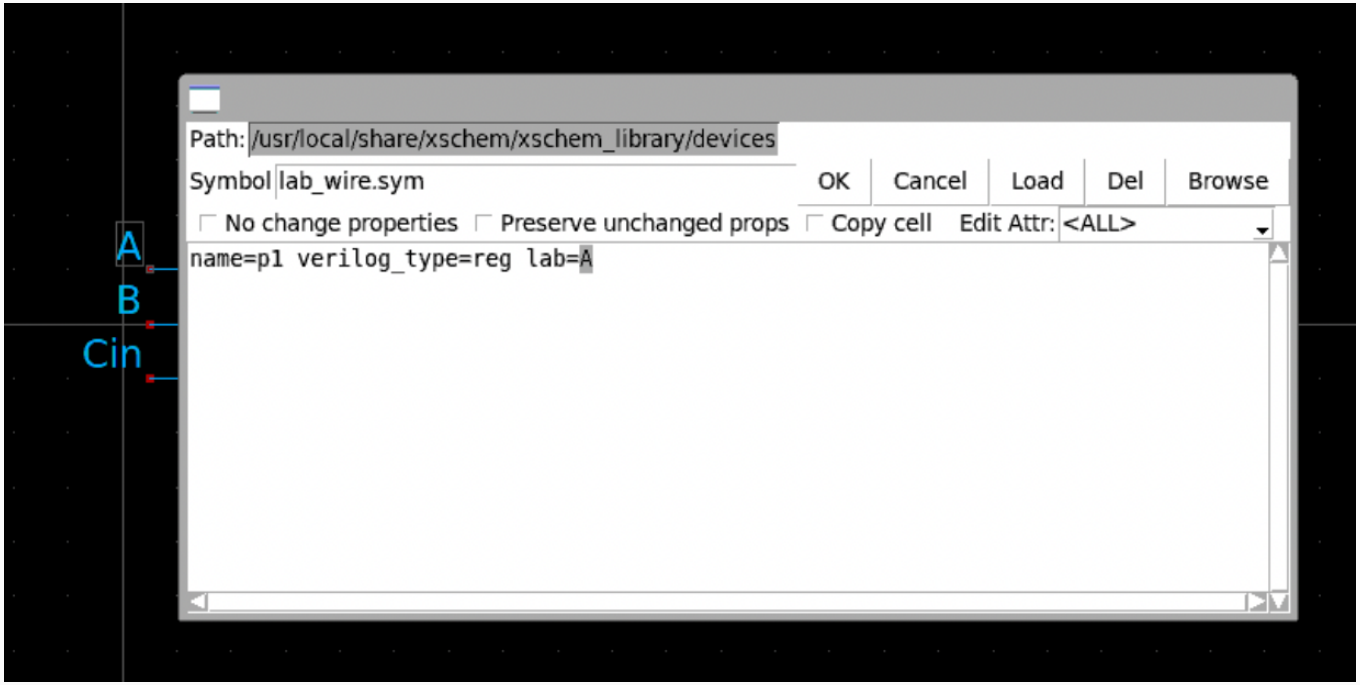
```
VERILOG
  initial begin
    $dumpfile("dumpfile.vcd");
    $dumpvars(0, A, B, Cin, Sum, Cout);
    A = 0;
    B = 0;
    Cin = 0;
  end

  integer x;
  always begin
  for (x = 1; x <= 7; x = x + 1) begin
    #10
    A = x[2];
    B = x[1];
    Cin = x[0];
    end
    #10
    $finish;
  end
```



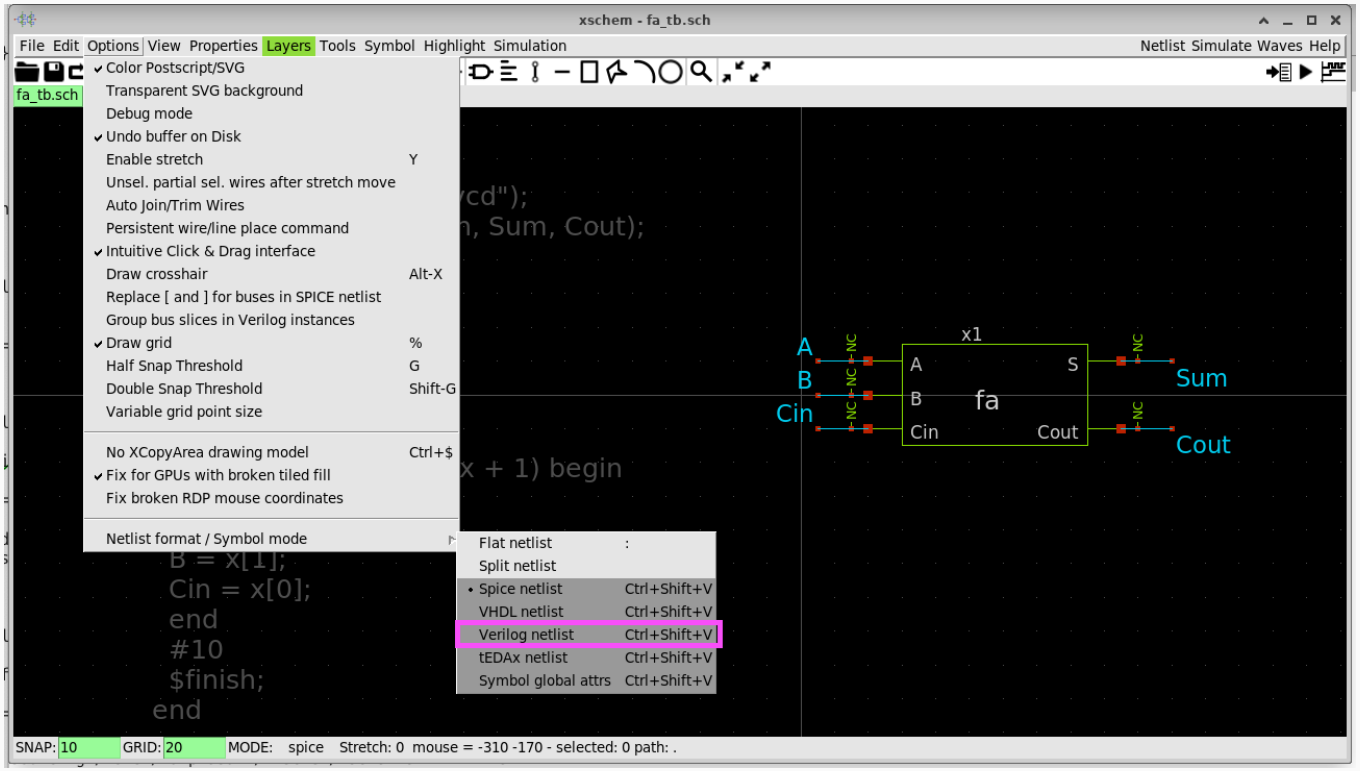
Experiment 7.1 - pin type

- Change the `verilog_type` all input pins to `reg`. In this example change the type of `A`, `B`, and `Cin` as shown below:



Experiment 7.1 - netlist mode

- Change the netlist mode to verilog as shown below:



- Netlist and Simulate
- Open the waveform in the external viewer `gtkwave`