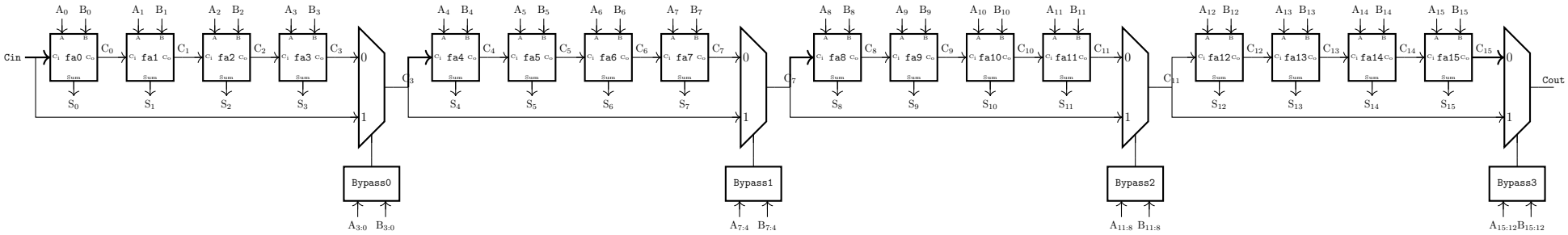
EC 5311 Digital IC Design: Assignment 8
False path in carry bypass adder

1. Implement the below carry-bypass adder in verilog:



2. Add a clock input and register the inputs/outputs of the above bypass adder.
3. Synthesize the adder using Yosys with the Sky130 PDK.
4. Perform STA, report the critical path and its slack.
5. Is the reported critical path right? If it is not, get STA to report the right critical path and its slack?