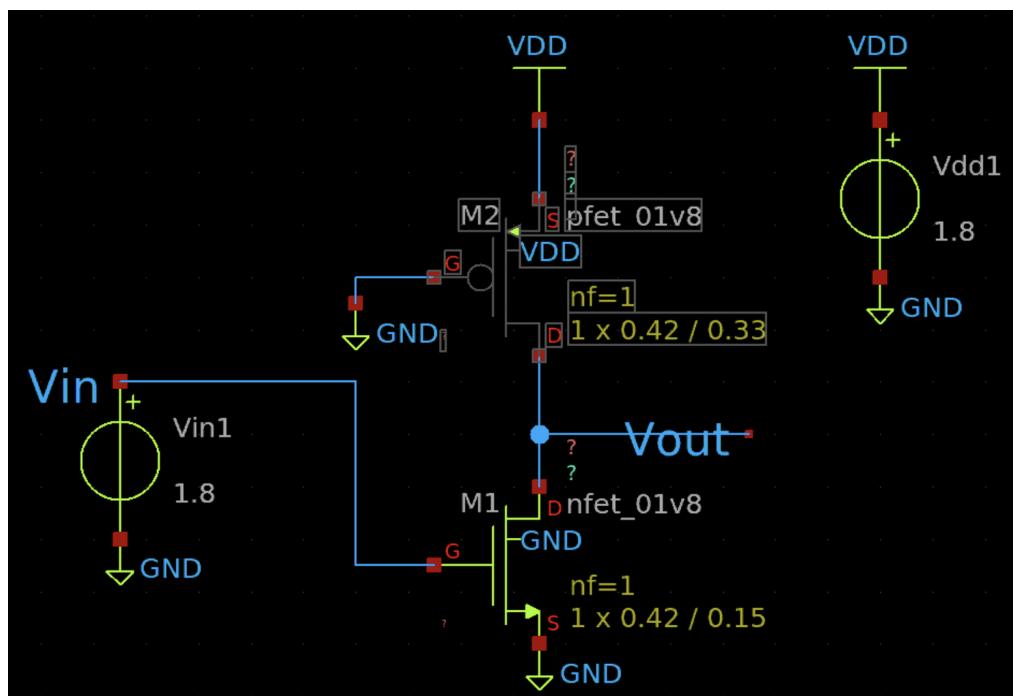


EE5311 Tutorial 2 Report - EE22B070

Himanshu Rajnish Borkar

Question 1.

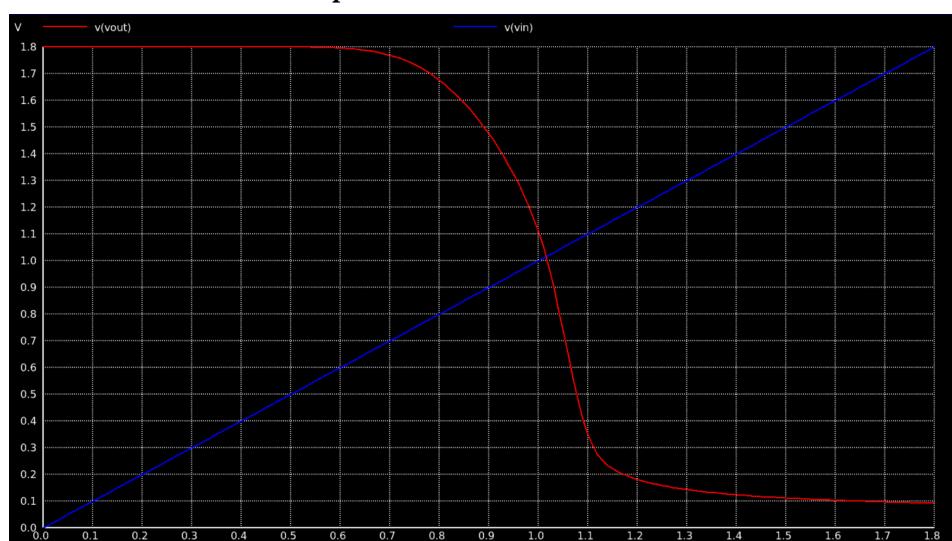
Schematic:



Schematic 1

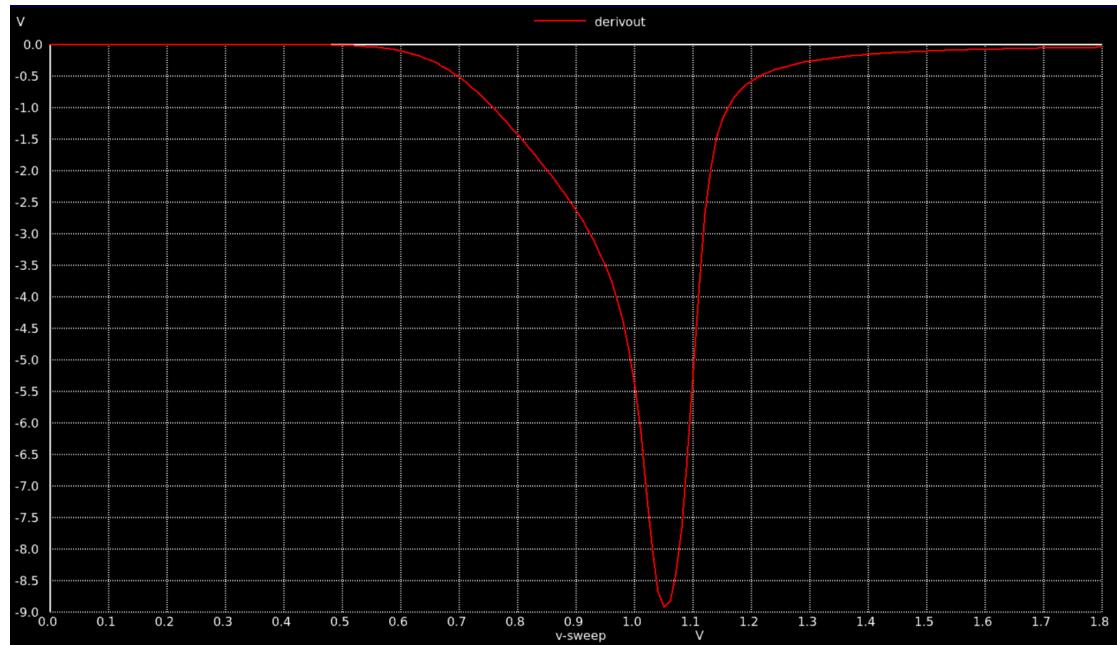
Measurement:

$$L_p = 0.32 \text{ micrometers}$$



Plot 1: DC Characteristics of the pseudo-CMOS Inverter in Schematic 1, $L_p = 0.32 \mu\text{m}$

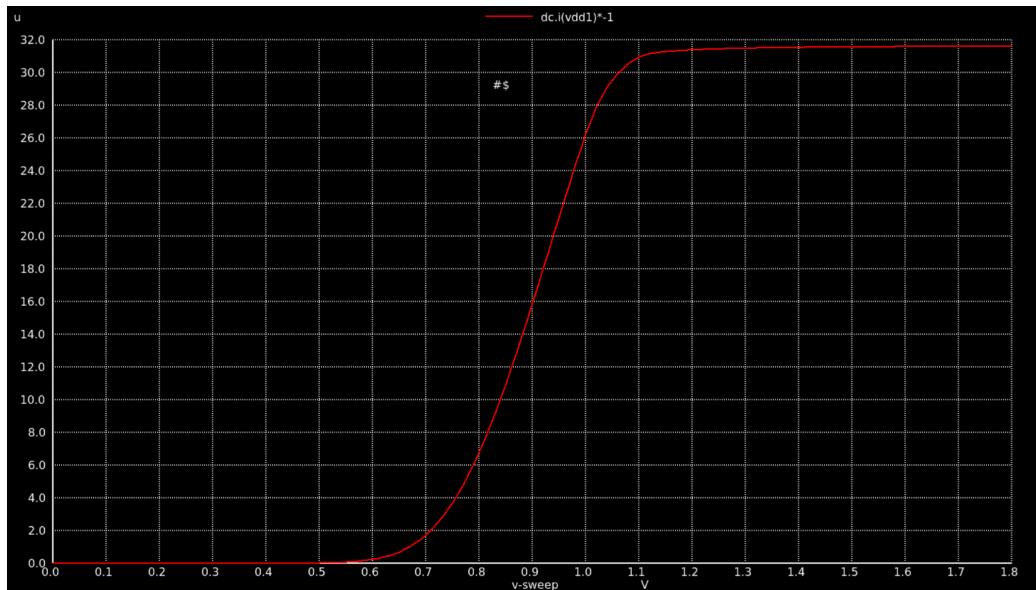
1.(b)



Plot 2: Derivative plot for Schematic 1 inverter.

```
vil      =  /4.5/841/e-01
vih      =  1.158563e+00
vm       =  1.031174e+00
NML: 0.757842 NMH: 0.641437
ngspice 2 -> [REDACTED]
```

1.(c)



```
ngspice 2 ->
x0 = 1.7906, y0 = 3.14912e-05
[REDACTED]
```

Calculations:

$$1(a) V_{\text{inv}(\text{threshold})} = 0.89V$$

|(c) $V_{in} = V_{DD}$

 $\Rightarrow V_{G1} = V_{DD}, V_{SD} = V_{DD} - V_o$
 $\Rightarrow V_{G1} - V_{TN} = V_{DD} - V_o < V_{DD} - V_o$
 Sat \approx

 $\Rightarrow I_{SD, \text{sat}} = V_p \left(\frac{W}{L} \right)_p \left(\frac{E_{CP} L}{E_{CP} L + 1.1} \right) (1.1)^2 (1 \rightarrow V_{DD})$
 $= 36.72 \times \left(\frac{0.4L}{0.568} \right) \left(\frac{0.83}{1.933} \right) (1.21) (1.306)$
 $I_{DS} \approx 28.57 \mu A, I_{DS \text{ sim}} = 81.7 \mu A$

 $P = V_{DD} I_{SD} = 81.37 \mu W$
 $P_{\text{sim}} = 57.06 \mu W$

1(c)

pMOS Size calc.

1 (o)

$$\boxed{V_{OL} = 0.1 \text{ V}} \Rightarrow V_{GS} = V_{DD} \\ V_{DS} = 0.1$$

\Rightarrow

$$V_{in} \propto V_{DD} \Rightarrow V_{in} = V_{DD} - V_{DS}$$

$$\Rightarrow V_{SG} = V_{DD} - 0 = V_{DD} = 1.8 \text{ V}$$

$$V_{SD} = V_{DD} - 0.1 = 1.7$$

$$I_{DS,lin} = k_n \left(\frac{E_{Cn} L}{E_{Cn} L + V_{GS} - V_{TP}} \right) \left[2(V_{GS} - V_{TP}) V_{DS} + V_{DS}^2 \right] (1 + \alpha V_{DS}) \quad | \quad V_{SG} - V_{TP} = 1.8 - 0.7 = 0.9 \text{ V}$$

$$| \quad V_{SG} - V_{TP} < V_{SP}$$

∴ sat region

$$= 164.2 \left(\frac{0.96}{0.96 + 1.8 - 0.7} \right) \left(2(1.8 - 0.7) 0.1 + (0.1)^2 \right) (1.016)$$

$$\approx 11.37$$

$$I_{SD,sat} = k_p \int \left(\frac{E_{Cp} L}{E_{Cp} L + V_{SG} - V_{TP}} \right) (V_{SG} - V_{TP})^2 (1 + \alpha V_{DS})$$

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$$I_{SD,sat} = 36.72 \int \left(\frac{0.833}{0.833 + 1.8 - 0.7} \right) (1.8 - 0.7)^2 (1 + 0.16 \times 1.7)$$

$$= 36.72 \int \times 0.431 \times 1.21 \times 1.306$$

$$\approx 25 \text{ f.}$$

$$\therefore \boxed{f = \frac{11.37}{25}}$$

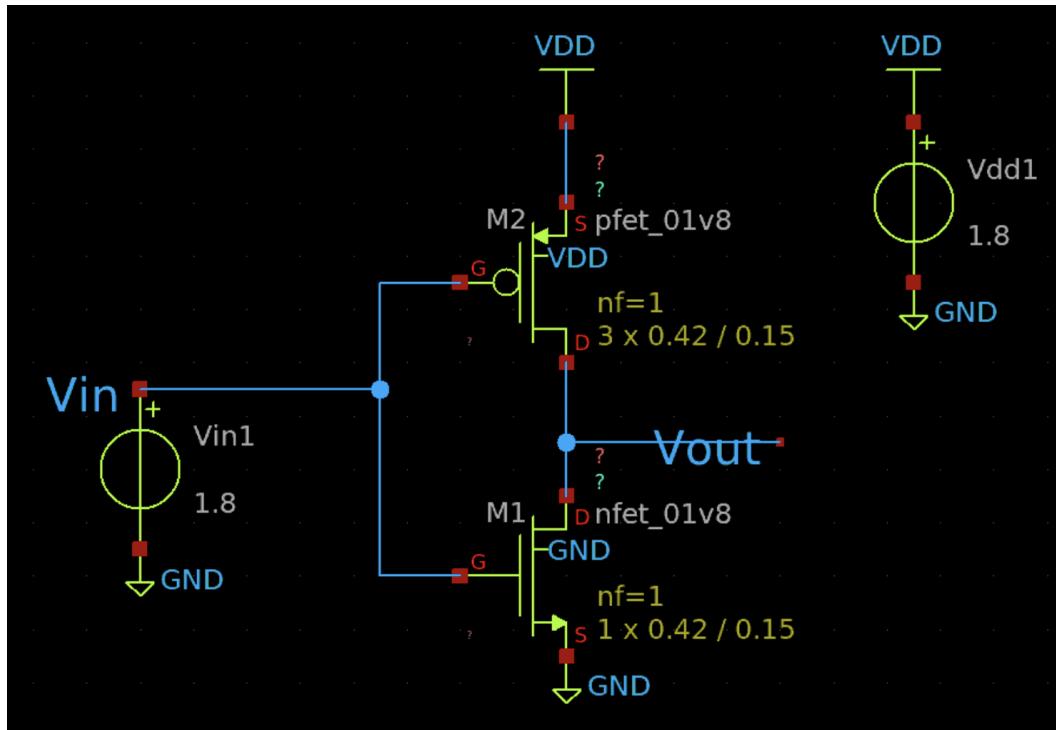
$$\therefore \left(\frac{W}{L} \right)_p = f \cdot \left(\frac{W}{L} \right)_n$$

$$\therefore \boxed{L_p = \frac{L_n}{f}} \Rightarrow \frac{25}{16.19} \times 0.15$$

$$\boxed{L_p \approx 0.33 \text{ } \mu\text{m}}$$

Question 2.

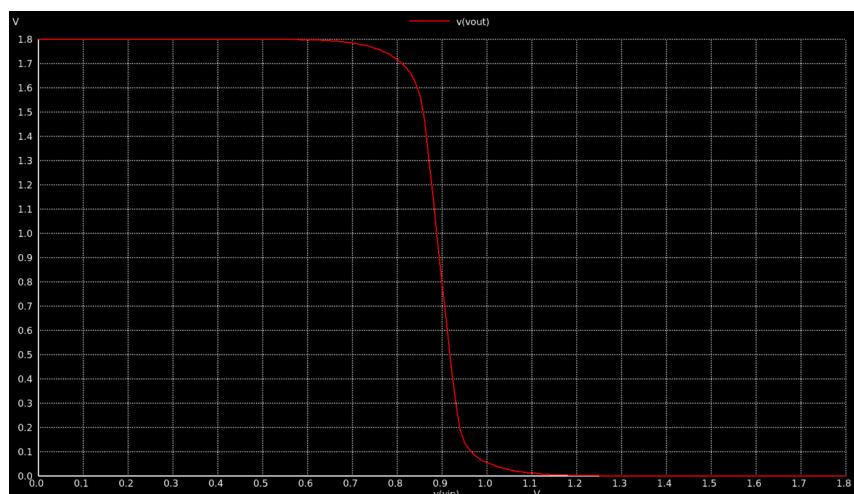
Schematic:



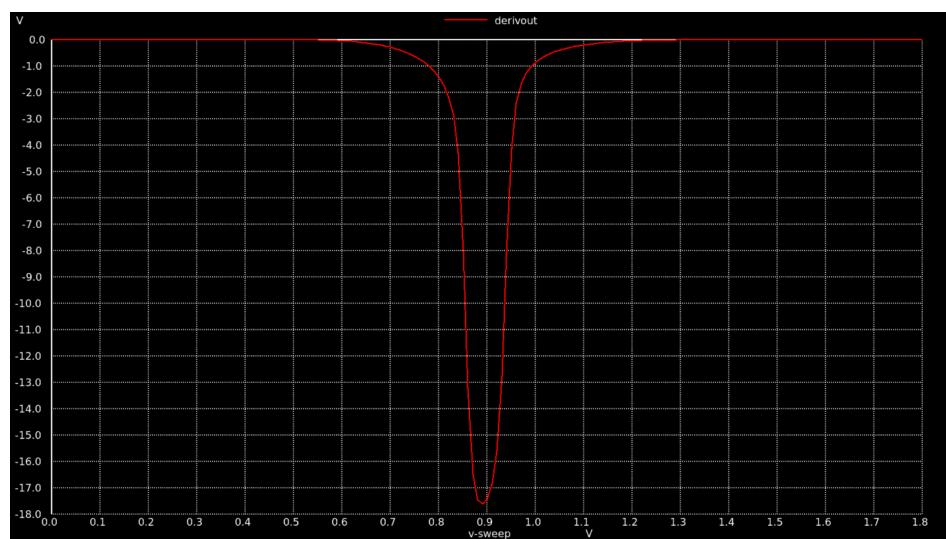
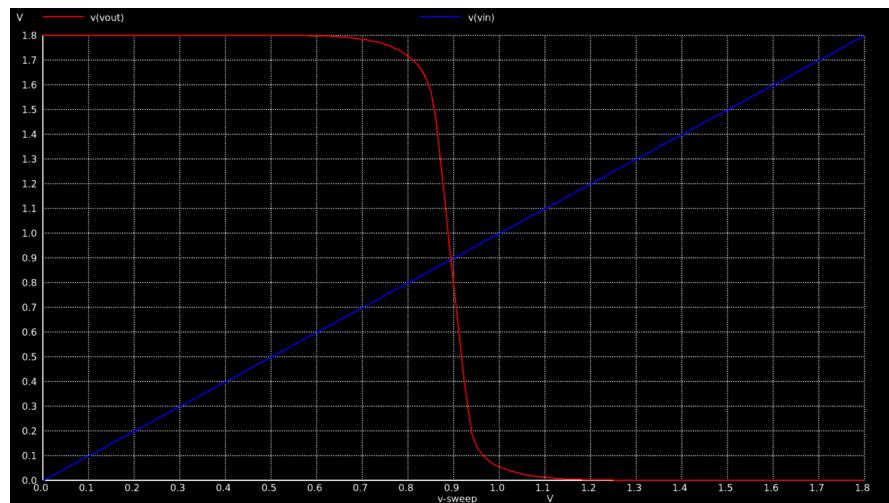
Schematic 2

Measurement:

1(0)



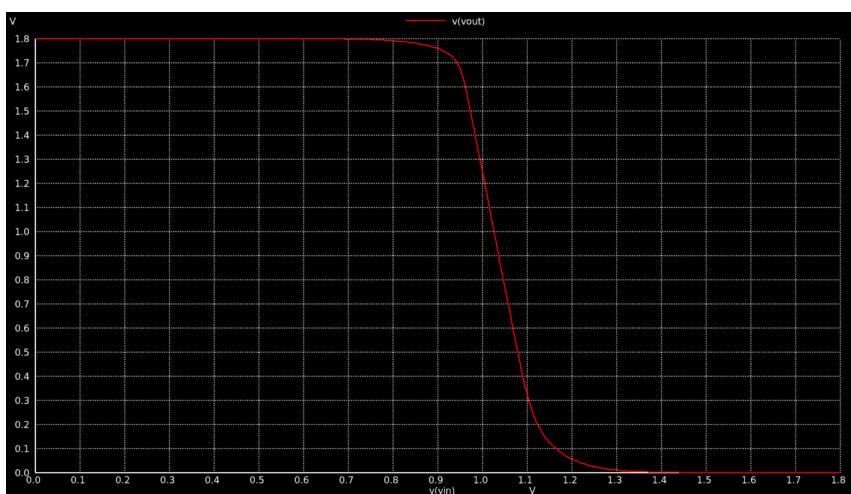
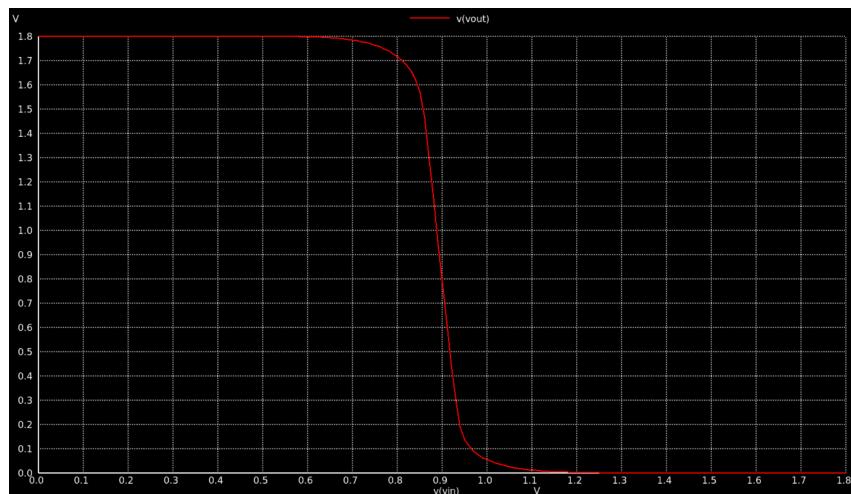
1(a)



```
vil          = 7.795111e-01
vih          = 9.913325e-01
vm          = 8.933287e-01
NML: 0.779511 NMH: 0.808667
ngspice 2 -
x0 = 1.32051, y0 = -6.04545
ngspice 2 -> █
```

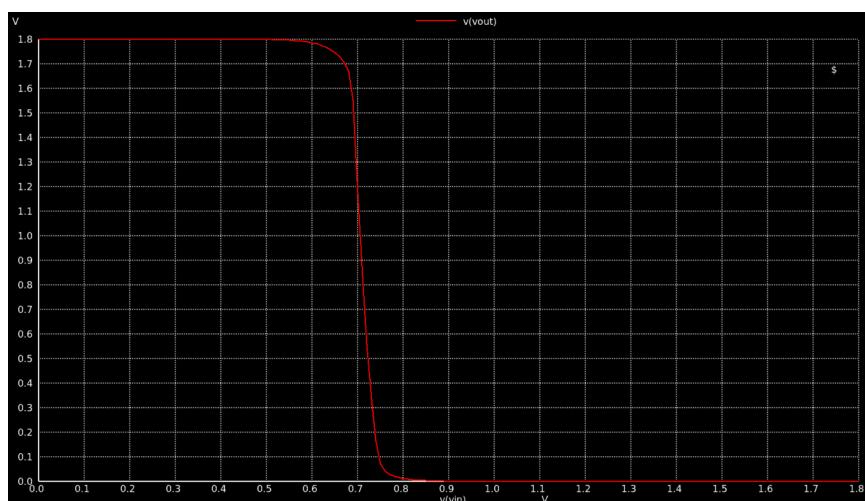
1(b)

For 1x (W/L)

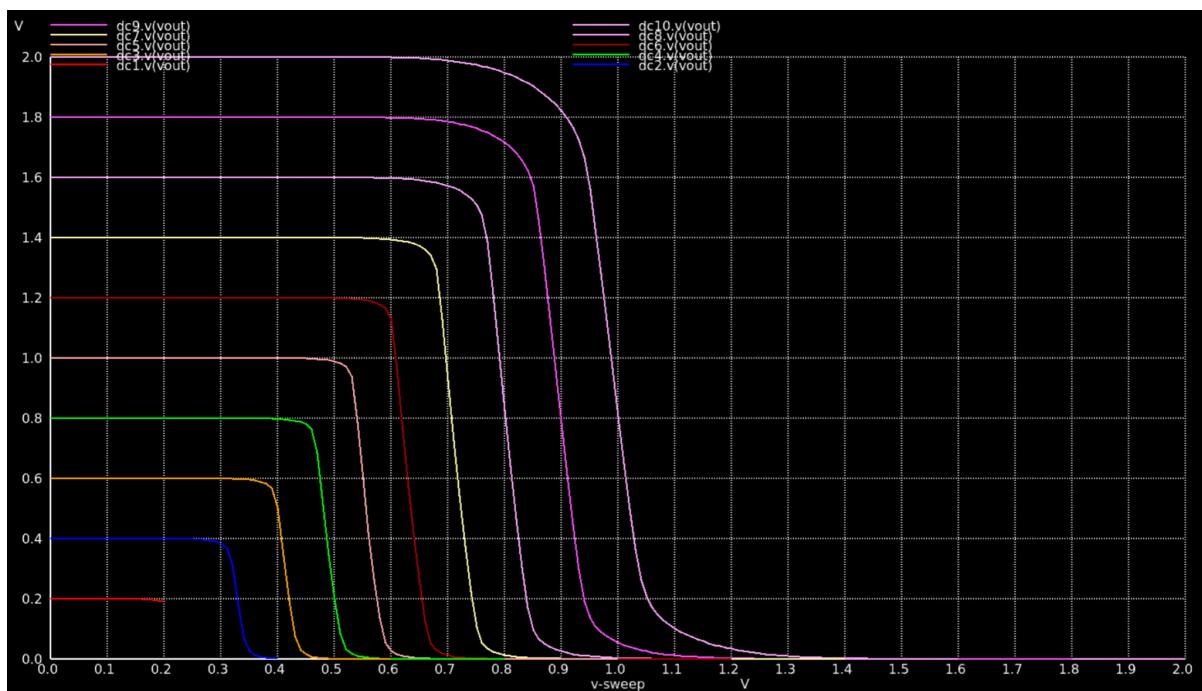


For 10x (W/L)

For 0.1x(W/L)

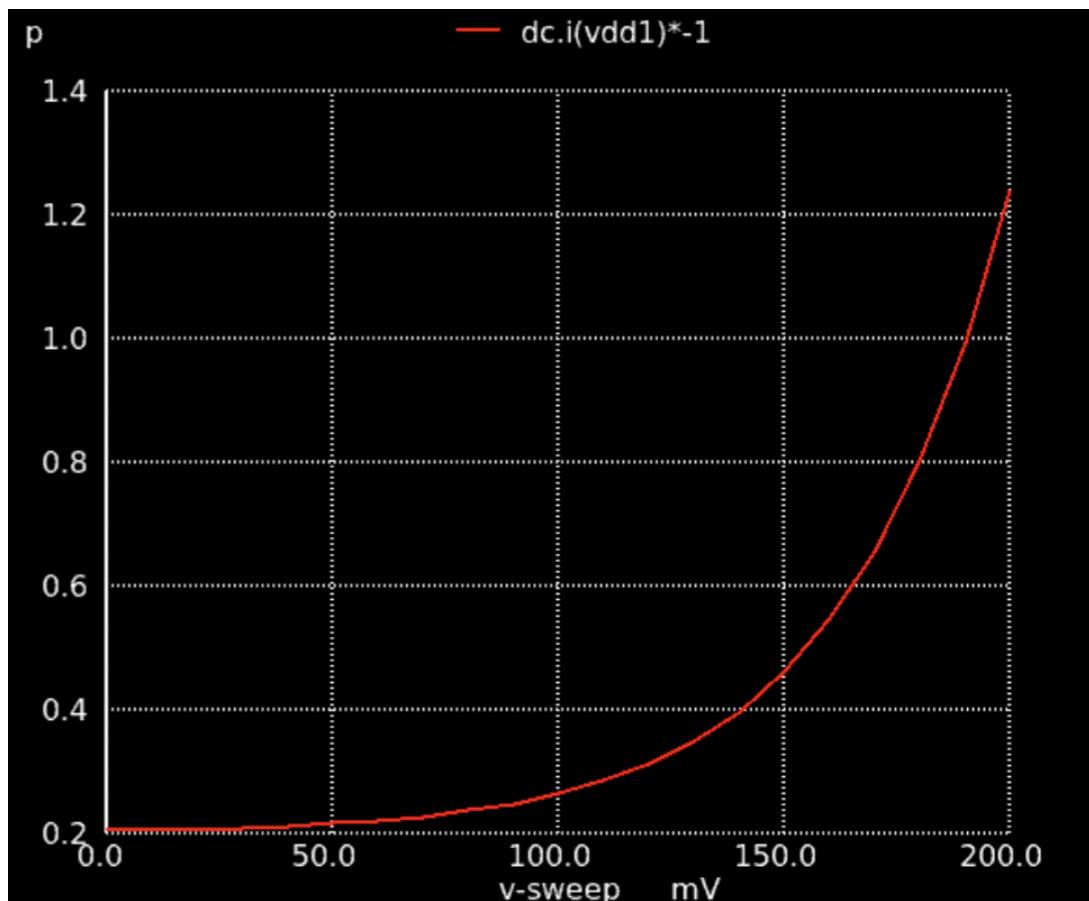


1(c)

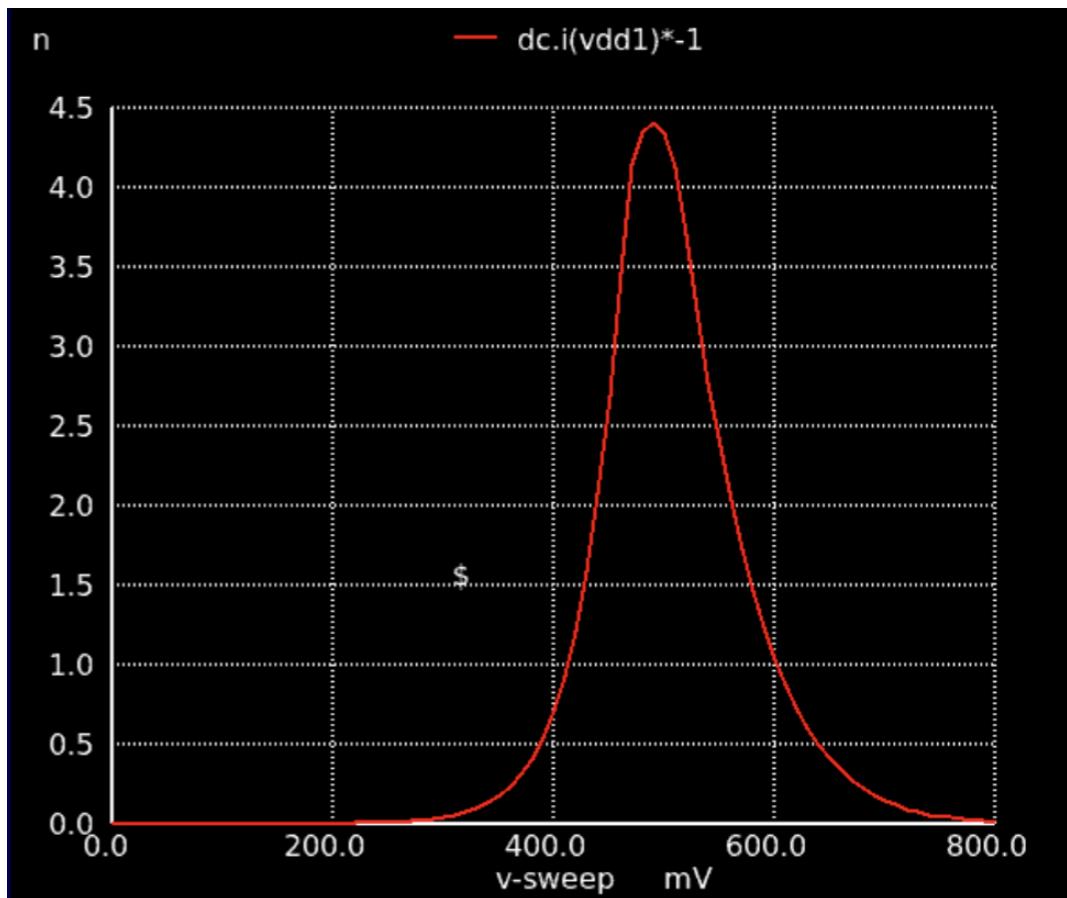


DC Characteristics of various Vdd values.

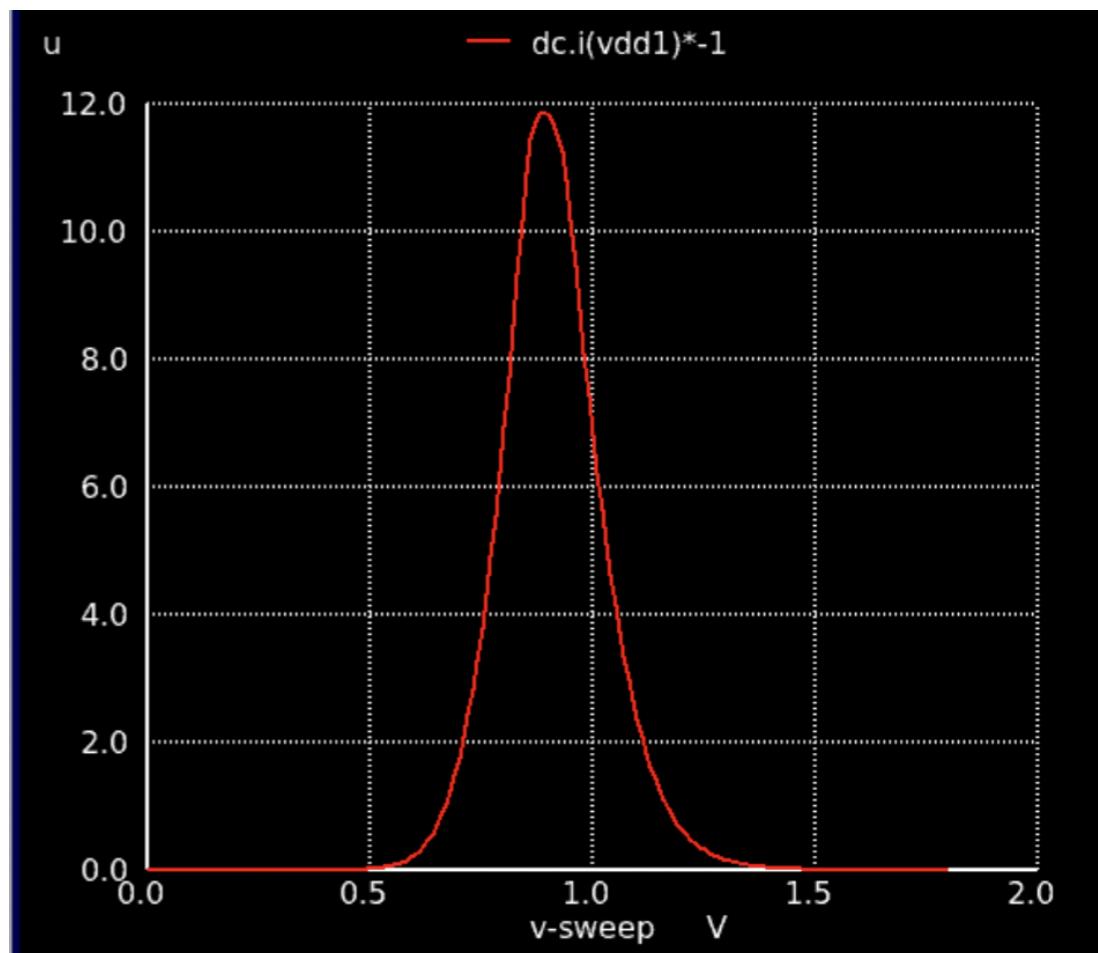
1(d)



For $\text{vdd} = 0.2\text{V}$



For vdd = 0.8V



For vdd = 1.8V

Calculations:

pMOS Sizing

$L_{(o)}$:

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n}{k_p}$$

≈ 3

$$\therefore \left[\frac{(W/L)_p}{(W/L)_n} = 3 \right]$$