EE5311: Digital IC Design

Tutorial 8

OpenLane - Automatic RTL to GDSII flow

- Input files should be in a directory `designs/<design name>`
- Design directory should be organised as:
  1. `src/*.v`: directory containing verilog files
  2. `src/*.sdc`: clock and other timing specification
  3. `config.json`: configuration file to specify user inputs
  4. `pin_order.cfg`: specify which pins of your top module go to which boundary of the floorplan
- An example `adder` is in the directory: `/cad/examples/designs`

OpenLane - SDC specification

- Specify the clock period in the Synopsys Design Constraints (SDC) as:

```
set_units -time ns
create_clock [get_ports <clock port>] -name clock -period <time period>
```

- Example for input port `clk` and period of 5ns:

```
set_units -time ns
create_clock [get_ports clk] -name clock -period 5.0
```

OpenLane - Pin configuration

- Specify the pins on the boundary of floorplan as:

```
#N
<north pins>
#S
<south pins>
#E
<east pins>
#W
<west pins>
```

- Example configuration for an adder with inputs `a`, `b`, `cin`, and `clk` and output `sum`:

```
#N
a.*
#S
b.*
#E
clk
cin
#W
sum.*
```

OpenLane - `config.json`

Specify various user inputs using the `config.json` file. Example for adder:

```
{
    "//": "Basics",
    "DESIGN_NAME": "adder",
    "VERILOG_FILES": "dir::src/*.v",
    "CLOCK_PERIOD": 5,
    "CLOCK_PORT": "clk",
    "PNR_SDC_FILE": "dir::src/adder.sdc",
    "SIGNOFF_SDC_FILE": "dir::src/adder.sdc",
    "//": "Pin Order",
    "FP_PIN_ORDER_CFG": "dir::pin_order.cfg"
}
```

OpenLane - Running the flow

- Run instructions: `openlane.sh <designs directory> <top module>`
- Example:
  1. Copy the `designs` directory to your path:
     `cp -r /cad/examples/designs .`
  2. Run: `openlane.sh designs adder`
  3. Final layout file:
     `designs/adder/runs/auto_pnr/results/signoff/adder.gds`
  4. Post-layout STA report:
     `designs/adder/runs/auto_pnr/logs/signoff/30-rcx_mcsta.nom.log`
  5. Your design meets timing specification if the setup and hold slack are non-negative in the post-layout STA report. e.g.

```
=========================================
report_worst_slack -max (Setup)
=========================================
worst slack 0.10

=========================================
report_worst_slack -min (Hold)
=========================================
worst slack 0.33
```

  6. Outputs of various stages of OpenLane flow are in:
     `designs/adder/runs/auto_pnr/results`