

EE5311 Tutorial 9 Report - EE22B070

Verilog Code:

https://drive.google.com/file/d/1yGhtHqhMH1ooY-RuR3ZniJKetLuyrvLm/view?usp=drive_link

Measurements:

Before false paths:

Delay	Time	Description
0.00	0.00	clock clk (rise edge)
0.00	0.00	clock network delay (ideal)
0.00	0.00	^ _33_/CLK (skyl30_fd_sc_hd_dfxtpt_1)
0.30	0.30	v _33_/Q (skyl30_fd_sc_hd_dfxtpt_1)
0.37	0.67	v x1/x1/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	1.06	v x1/x2/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	1.44	v x1/x3/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.34	1.78	v x1/x4/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.32	2.10	v x1/x17/_4_/X (skyl30_fd_sc_hd_mux2_1)
0.38	2.48	v x1/x5/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	2.87	v x1/x6/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	3.25	v x1/x7/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.34	3.60	v x1/x8/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.32	3.91	v x1/x18/_4_/X (skyl30_fd_sc_hd_mux2_1)
0.38	4.30	v x1/x9/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	4.68	v x1/x10/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	5.06	v x1/x11/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.34	5.41	v x1/x12/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.32	5.73	v x1/x19/_4_/X (skyl30_fd_sc_hd_mux2_1)
0.38	6.11	v x1/x13/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	6.49	v x1/x14/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.38	6.88	v x1/x15/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.34	7.22	v x1/x16/_10_/X (skyl30_fd_sc_hd_maj3_1)
0.27	7.49	v x1/x20/_4_/X (skyl30_fd_sc_hd_mux2_1)
0.00	7.49	v _16_/D (skyl30_fd_sc_hd_dfxtpt_1)
	7.49	data arrival time
3.00	3.00	clock clk (rise edge)
0.00	3.00	clock network delay (ideal)
0.00	3.00	clock reconvergence pessimism
	3.00	^ _16_/CLK (skyl30_fd_sc_hd_dfxtpt_1)
-0.12	2.88	library setup time
	2.88	data required time
	2.88	data required time
	-7.49	data arrival time
	-4.61	slack (VIOLATED)

Time period = 3 - (-4.61) = 7.61ns

Max frequency = 131.40 MHz

After false paths:

```
% set_false_path -through x1/x1/_10_/X
% set_false_path -through x1/x5/_10_/X
% set_false_path -through x1/x9/_10_/X
% set_false_path -through x1/x20/_4_/X
% report_checks -path_delay max
Startpoint: _34_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _15_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
```

Delay	Time	Description
0.00	0.00	clock clk (rise edge)
0.00	0.00	clock network delay (ideal)
0.00	0.00	^ _34_/CLK (sky130_fd_sc_hd_dfxtp_1)
0.30	0.30	v _34_/Q (sky130_fd_sc_hd_dfxtp_1)
0.37	0.67	v x1/x2/_10_/X (sky130_fd_sc_hd_maj3_1)
0.38	1.06	v x1/x3/_10_/X (sky130_fd_sc_hd_maj3_1)
0.34	1.40	v x1/x4/_10_/X (sky130_fd_sc_hd_maj3_1)
0.32	1.72	v x1/x17/_4_/X (sky130_fd_sc_hd_mux2_1)
0.34	2.06	v x1/x18/_4_/X (sky130_fd_sc_hd_mux2_1)
0.34	2.39	v x1/x19/_4_/X (sky130_fd_sc_hd_mux2_1)
0.38	2.78	v x1/x13/_10_/X (sky130_fd_sc_hd_maj3_1)
0.38	3.16	v x1/x14/_10_/X (sky130_fd_sc_hd_maj3_1)
0.38	3.54	v x1/x15/_10_/X (sky130_fd_sc_hd_maj3_1)
0.18	3.72	v x1/x16/_11_/X (sky130_fd_sc_hd_xor3_1)
0.00	3.72	v _15_/D (sky130_fd_sc_hd_dfxtp_1)
	3.72	data arrival time
3.00	3.00	clock clk (rise edge)
0.00	3.00	clock network delay (ideal)
0.00	3.00	clock reconvergence pessimism
	3.00	^ _15_/CLK (sky130_fd_sc_hd_dfxtp_1)
-0.13	2.87	library setup time
	2.87	data required time
	2.87	data required time
	-3.72	data arrival time
	-0.85	slack (VIOLATED)

Time period = $3 - (-0.85) = 3.85\text{ns}$

Max frequency = 259.74 MHz