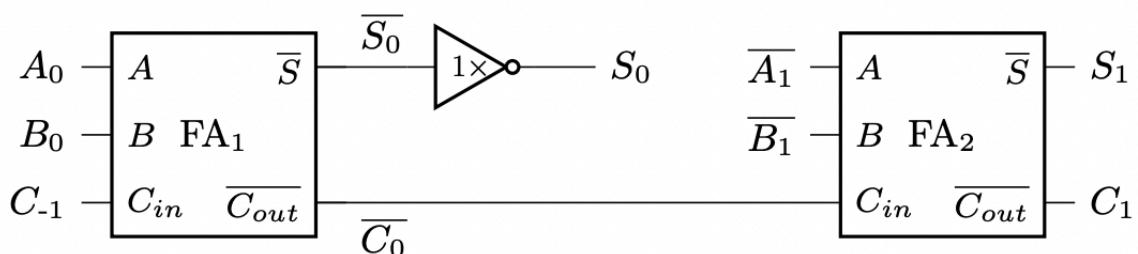


# EE5311 Tutorial 6a Report - EE22B070

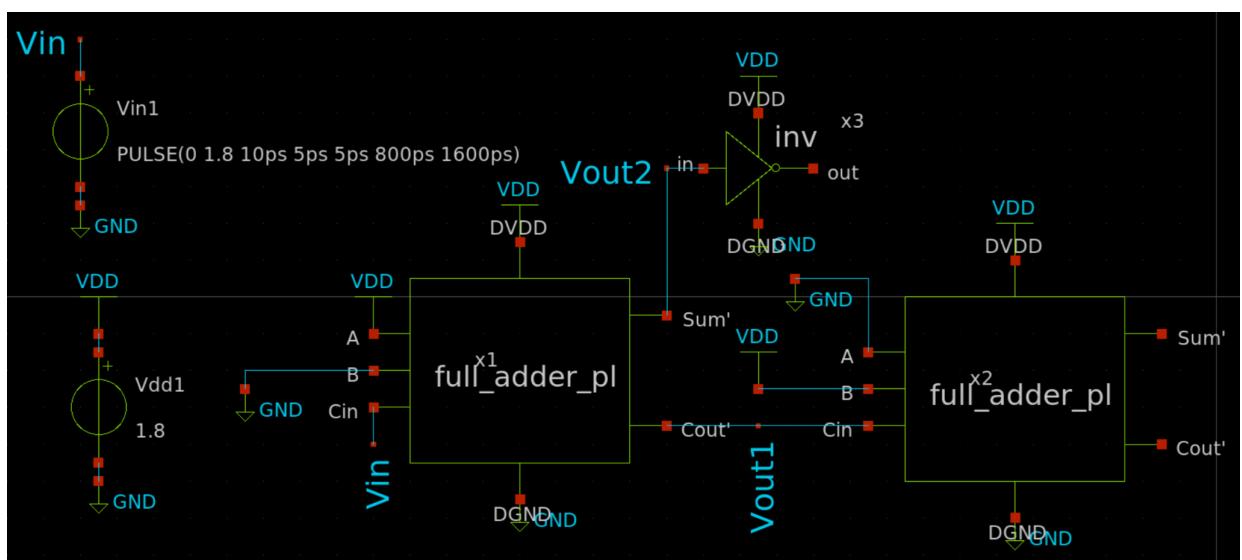
By Himanshu Rajnish Borkar  
3/04/2025

## Question 1: Full Adder

Draw a schematic for the carry and sum logic in a mirror-symmetric full adder, done in class. Size the p/nMOS to minimize the delay from input to output carry, and the stage effort of the carry logic is four when used in a ripple carry adder. Create a symbol for the full adder and connect two full adders as shown below:



## Schematic:

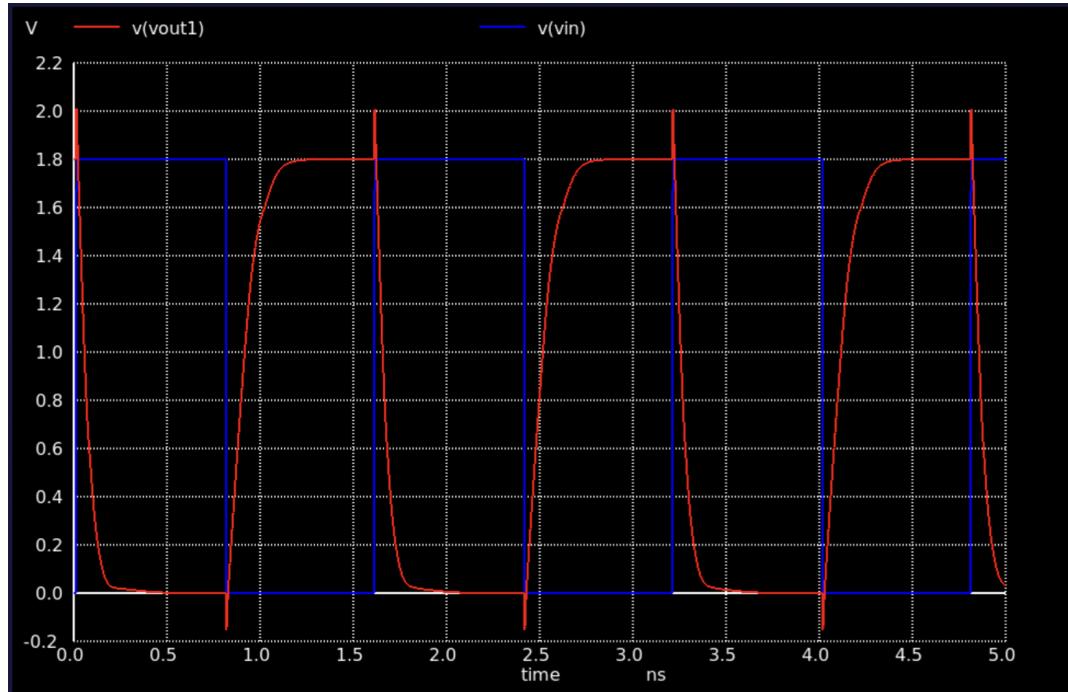


1 (a) Measure the delays: (i) from  $C_{in}$  to  $C_{in}'$ , and (ii) from  $C_{in}$  to  $S_0'$ .

# Measurements:

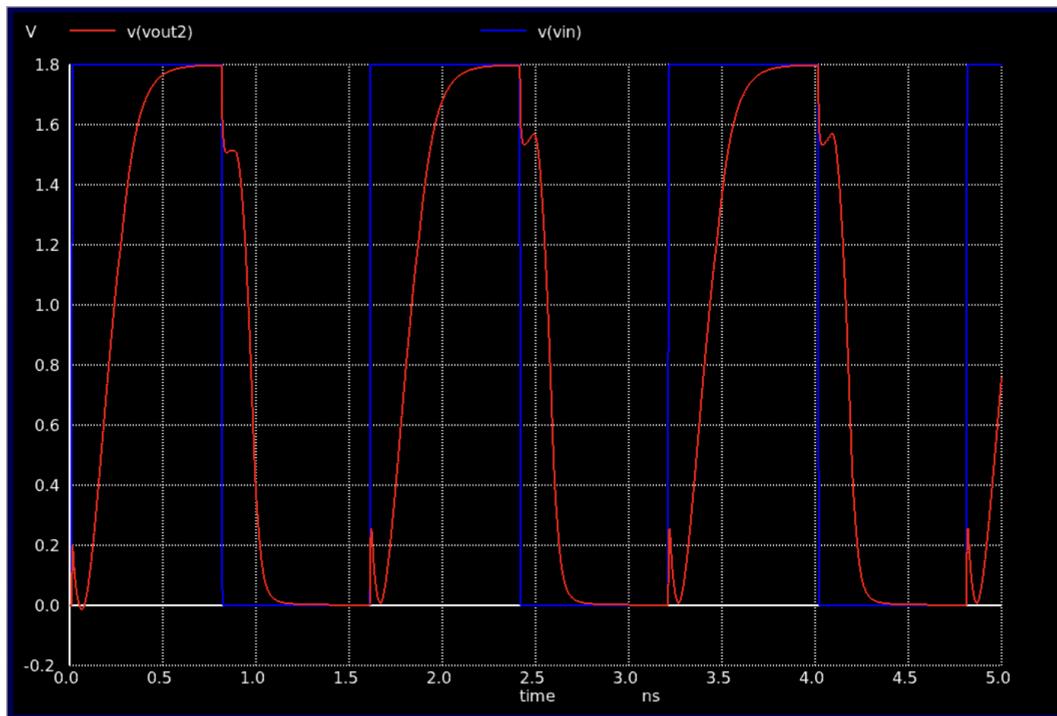
## PRE-LAYOUT

(i)



$C_0$  vs  $V_{in}$  plot

(ii)



$S_0$  vs  $V_{in}$  plot

Here  $C_0^l$  is the carry out from the first Full Adder, and  $S_0^l$  is the sum from the first Full Adder.

### Delays:

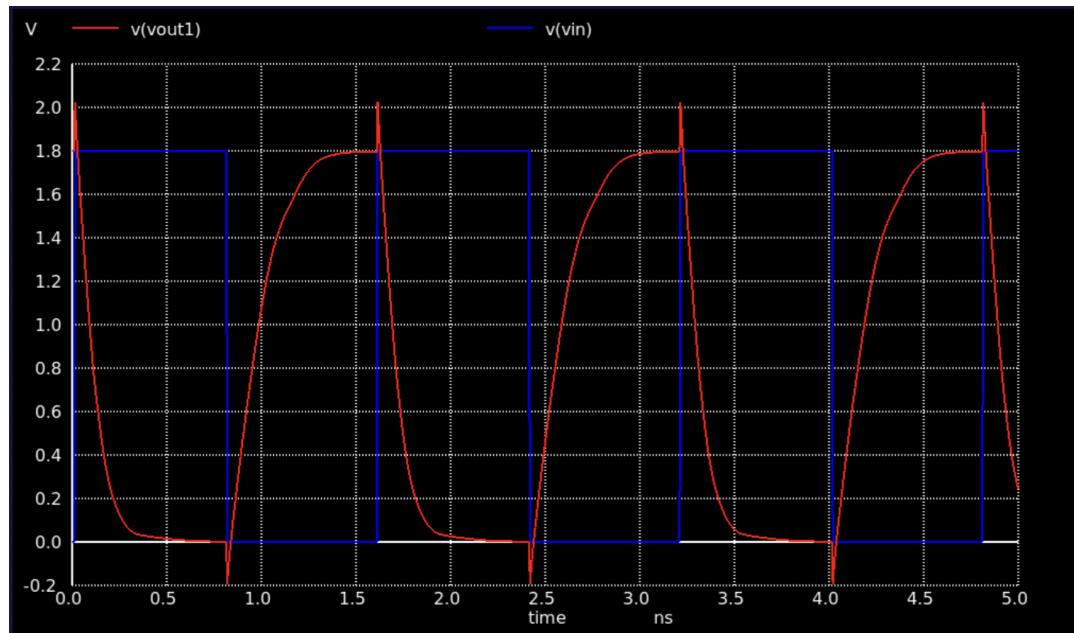
```
thlc      = 5.005178e-11 targ= 6.255178e-11 trig= 1.250000e-11
tlhc      = 9.004704e-11 targ= 9.075470e-10 trig= 8.175000e-10
thls      = 1.487007e-10 targ= 9.662007e-10 trig= 8.175000e-10
tlhs      = 2.128392e-10 targ= 2.253392e-10 trig= 1.250000e-11
C0_delay : 7.00494E-11
S0_delay : 1.8077E-10
```

- $C_0^l$  delay: **70 ps**
- $S_0^l$  delay: **180 ps**

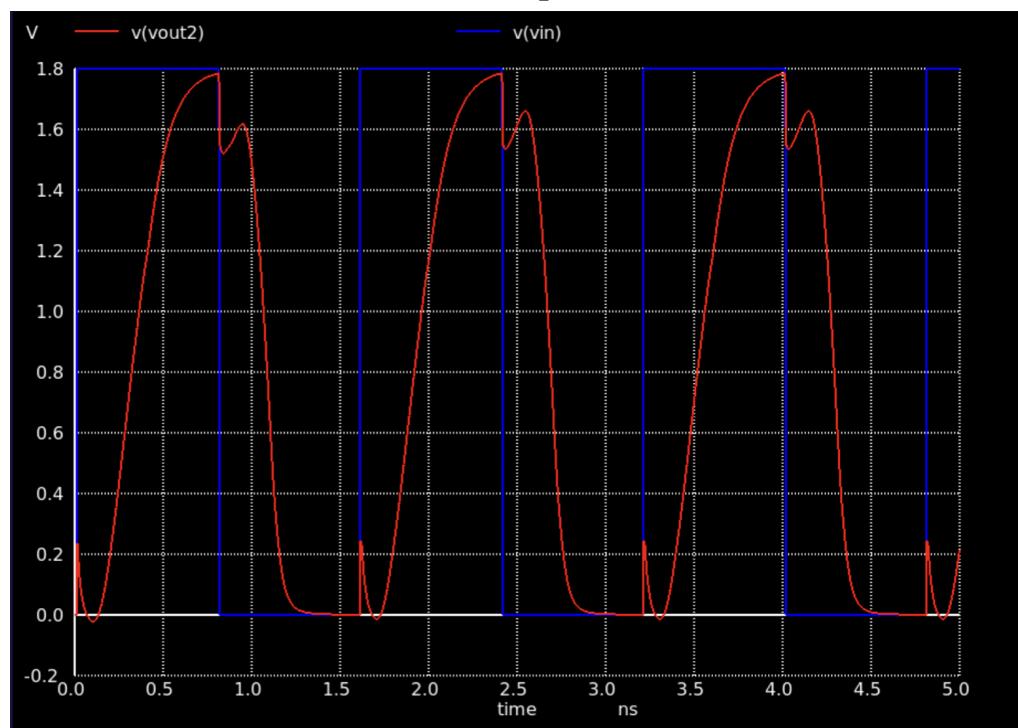
(c) Draw the layout for the full-adder and measure the layout extracted delay and compare it against the pre-layout delay. Use diffusion sharing and num fingers to create a compact layout. The height of the full adder should be the same as the inverter in Assignment 5.

## Measurements:

### POST-LAYOUT



$C_0$  vs  $V_{in}$  plot



$S_0$  vs  $V_{in}$  plot

Here  $C_0^l$  is the carry out from the first Full Adder, and  $S_0^l$  is the sum from the first Full Adder.

### **Delays:**

```

thlc      = 8.913603e-11 targ= 1.016360e-10 trig= 1.250000e-11
tlhc      = 1.515386e-10 targ= 9.690386e-10 trig= 8.175000e-10
thls      = 2.605903e-10 targ= 1.078090e-09 trig= 8.175000e-10
tlhs      = 3.306568e-10 targ= 3.431568e-10 trig= 1.250000e-11
C0_delay : 1.20337E-10
S0_delay : 2.95624E-10

```

- $C_0^l$  delay: **120 ps**
- $S_0^l$  delay: **295 ps**

### **Delay Table:**

	<b>delay(<math>C_0^l</math>)</b>	<b>delay(<math>S_0^l</math>)</b>
<b>Pre-layout</b>	<b>70 ps</b>	<b>180 ps</b>
<b>Post-layout</b>	<b>120 ps</b>	<b>295 ps</b>

### **Sim-Code:**

```

sim

.include inv_extracted.spice
.include full_adder_pl_extracted.spice
.control
tran 0.1p 5n
plot v(Vout1) v(Vin)
plot v(Vout2) v(Vin)
meas tran thlc trig v(Vin) val = 0.9 rise = 1 targ v(Vout1) val = 0.9 fall = 1
meas tran tlhc trig v(Vin) val = 0.9 fall = 1 targ v(Vout1) val = 0.9 rise = 1
meas tran thls trig v(Vin) val = 0.9 fall = 1 targ v(Vout2) val = 0.9 fall = 1
meas tran tlhs trig v(Vin) val = 0.9 rise = 1 targ v(Vout2) val = 0.9 rise = 1

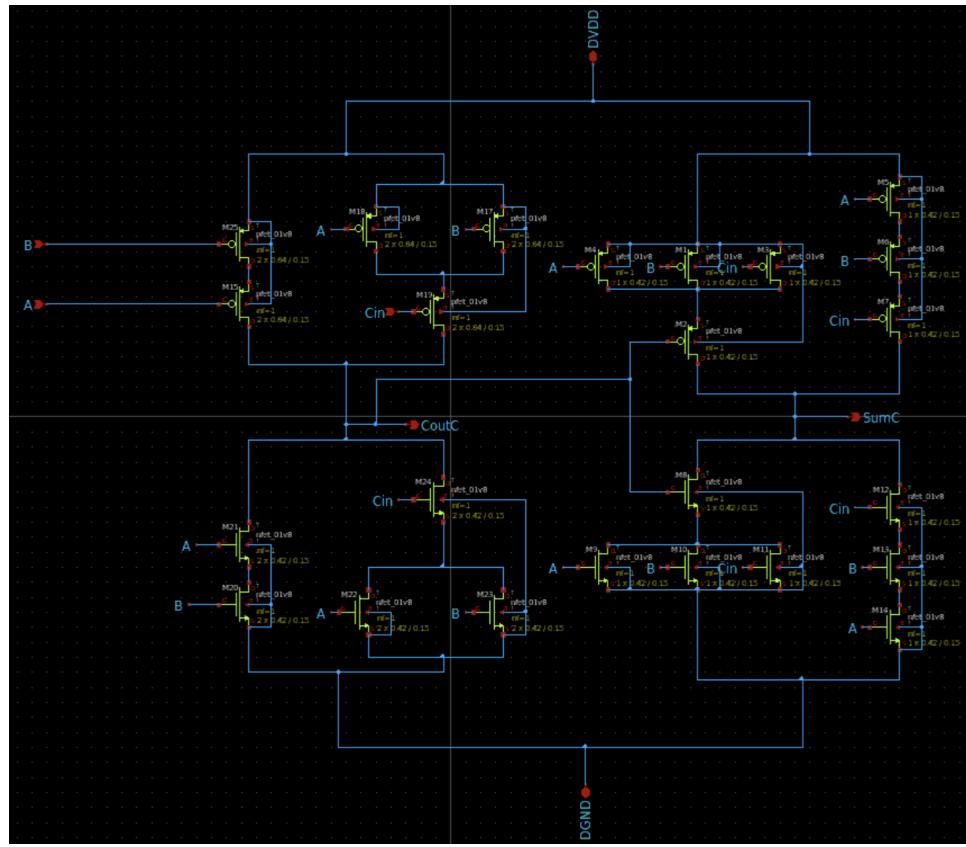
let delayc = ($&thlc + $&tlhc)/2
echo C0_delay : $&delayc

let delays = ($&thls + $&tlhs)/2
echo S0_delay : $&delays

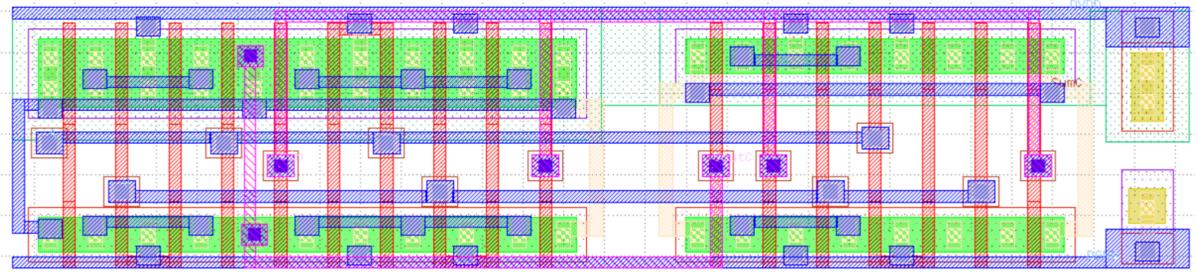
end
.endc

```

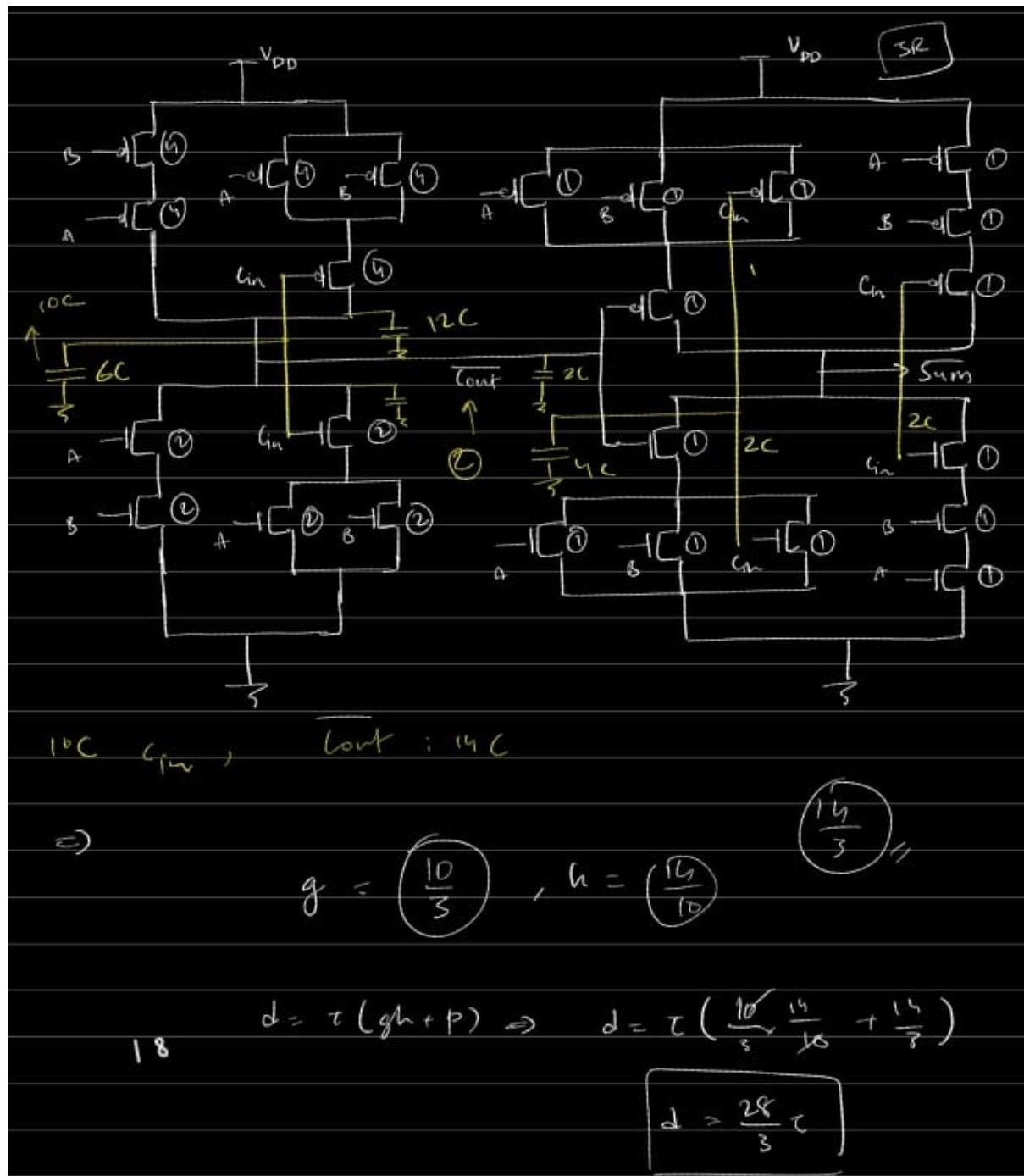
## Full Adder Schematic:



## Full Adder Layout:



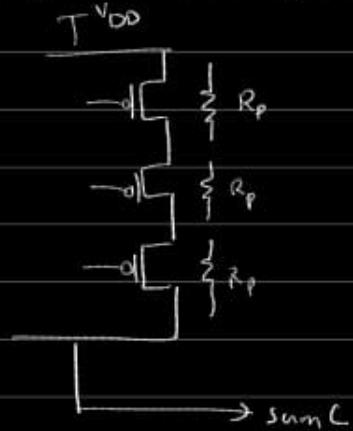
(b) How do the measured delays compare against that estimated using logical and electrical effort?



$$d = \frac{28}{3} \times 10^{-5} \text{ ps}$$

$\therefore [d = 98 \text{ ps}] \rightarrow \text{for } \overline{\text{Cout}}$

and for sum: we consider  $\overline{C_0} \rightarrow \overline{S_0}$  delay.



Now, for ② PMOS  $\left\{ \begin{array}{l} R_{eq} \text{ are same} \rightarrow R \\ \& ① \text{ NMOS} \end{array} \right\}$

① PMOS: Width is decreased

$$\therefore R \rightarrow (2R_0)$$

$$\therefore \text{Now, } d = 0.693 R_{eq} C_{total}$$

$$\underbrace{(C_{self} + C_{load})}_{\Downarrow}$$

$$\left. \begin{array}{l} C_{self} = 4C \\ C_{load} = 3C \end{array} \right\} C_{total} = 7C$$

$R_{eq}$ : the worst case  $R_{eq} = 2R_o$

$$\therefore d = 0.695 \times 2R_o \times T_C \\ = 147 \\ = 147 \text{ ps}$$

$$\therefore d_{\text{total}} = 147 \text{ ps} + 98 \text{ ps} \\ = 245 \text{ ps}$$

$$d_{S_0} = 245 \text{ ps}$$

$$d_{T_0} = 98 \text{ ps}$$