

EE5311 Tutorial 5 Report - EE22B070

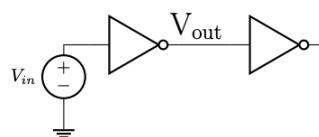
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6/03/2025

Question 1: Inverter

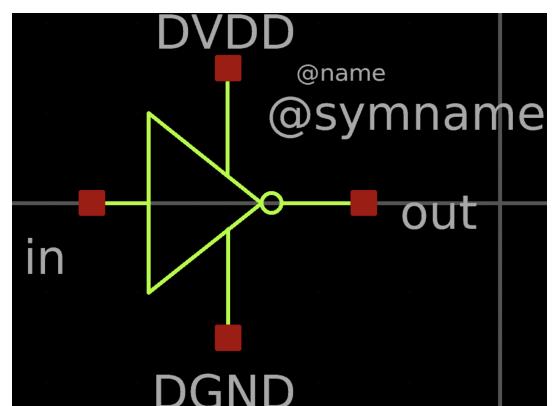
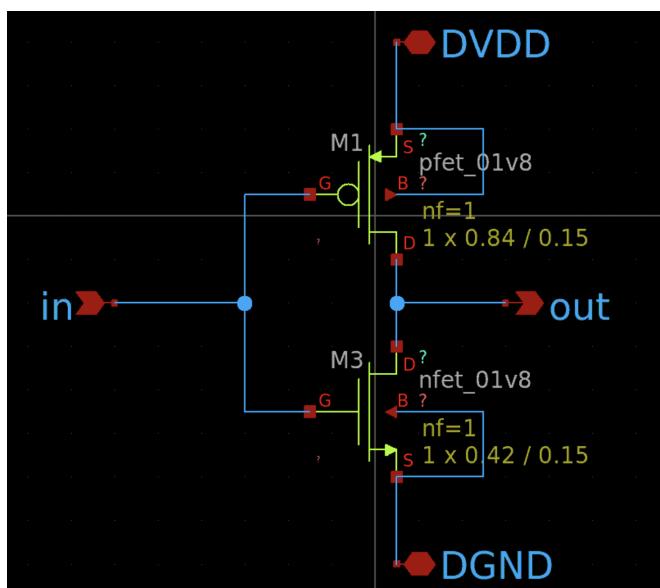
1. Draw a DRC and LVS clean layout of the CMOS inverter with the minimum delay from Assignment 3.

- (a) Extract the parasitic values from the layout and find the delay of the inverter using the circuit:

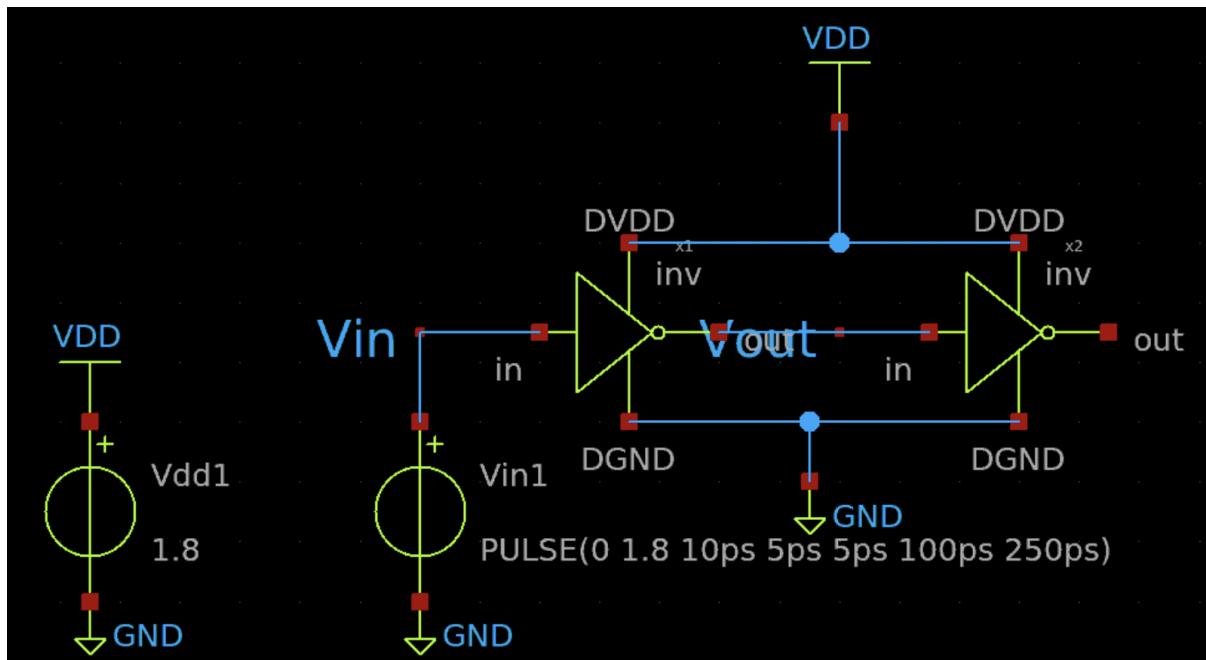


- (b) Measure the delay including the layout parasitic of net V_{out} .

Inverter Schematic:



Circuit Schematic:



Simulation Code:

```
Corner: tt sim
.include inv_extracted.spice
.control
tran 0.01p 250p
plot v(Vout) v(Vin)

meas tran thl trig v(Vin) val = 0.9 rise = 1 targ v(Vout) val = 0.9 fall = 1
meas tran tlh trig v(Vin) val = 0.9 fall = 1 targ v(Vout) val = 0.9 rise = 1

let delay = ($&thl + $&tlh) / 2
echo delay: $&delay
.endc
```

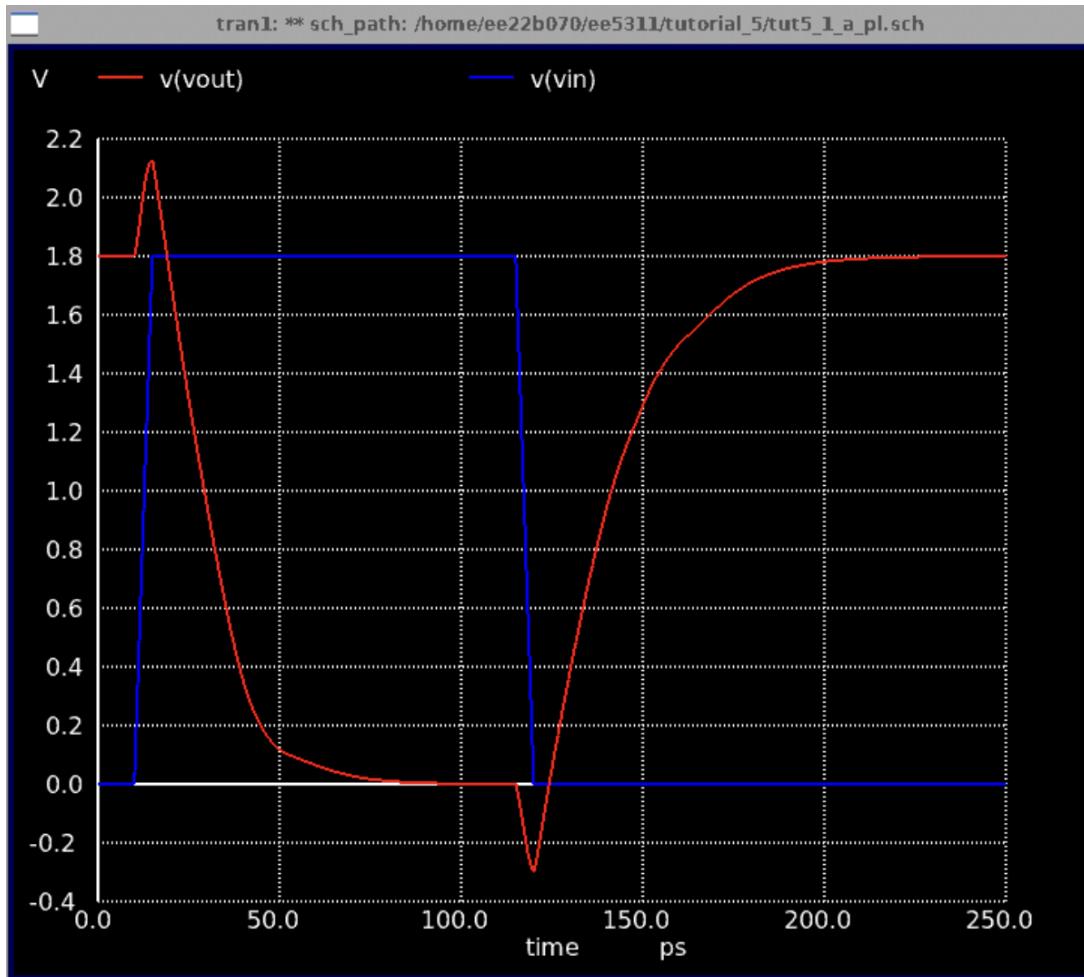
Pre-Layout Measurements:

For these measurements, the ".include inv_extracted.spice" file is commented out

```
thl      = 1.822969e-11 targ= 3.072969e-11 trig= 1.250000e-11
tlh      = 2.167988e-11 targ= 1.391799e-10 trig= 1.175000e-10
delay: 1.99548E-11
ngspice 2 -> ■
```

Delay and rise time/fall time values

The delay for primitive circuit is: **19.954 ps**.



V_{out} and V_{in} transient plot signifying delay

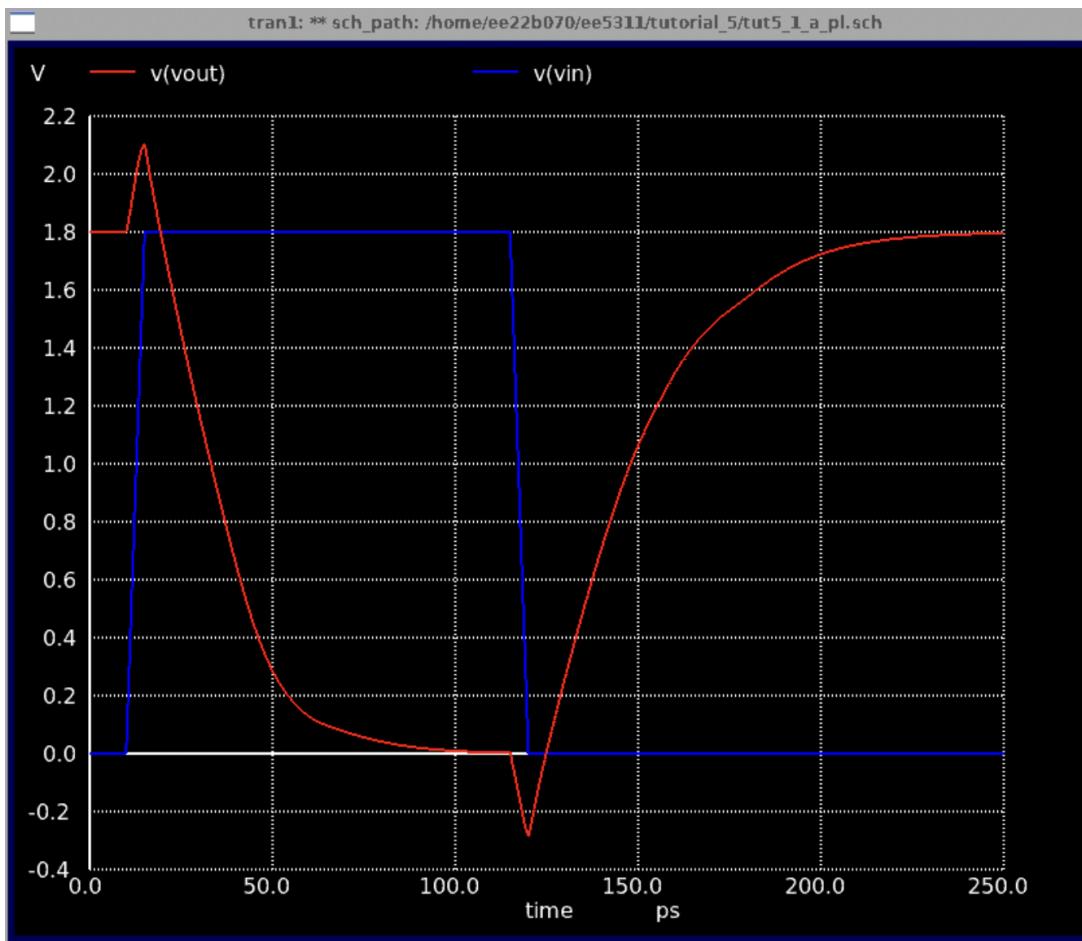
Post-Layout Measurements: (inclusive of layout parasitics)

For these measurements, the ".include inv_extracted.spice" file is included.

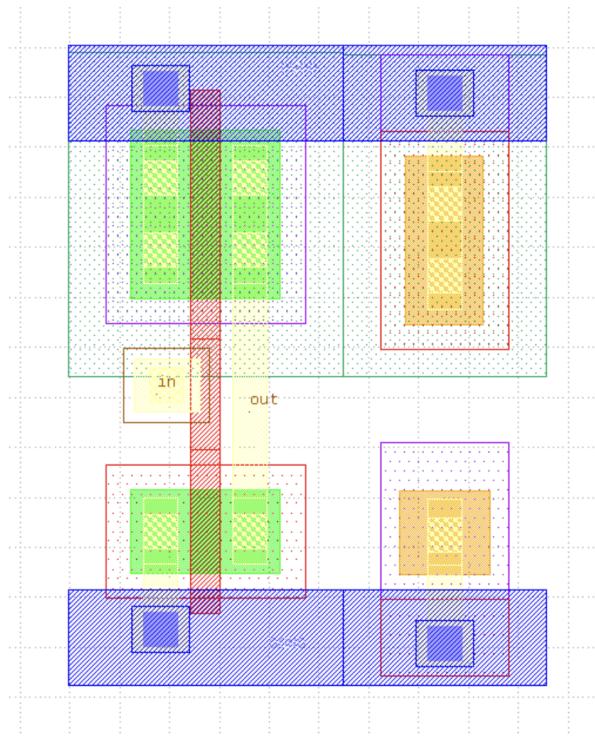
```
thl          = 2.255910e-11 targ= 3.505910e-11 trig= 1.250000e-11
tlh          = 2.749067e-11 targ= 1.449907e-10 trig= 1.175000e-10
delay: 2.50249E-11
ngspice 2 -> ■
```

Delay and rise time/fall time values

The delay for subcircuit circuit is: **25.025 ps**.



V_{out} and V_{in} transient plot signifying delay



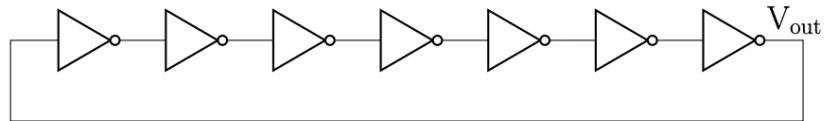
Inverter layout (left - nMOS and pMOS, right - tap)

Layout Parasitics:

```
* NGSPICE file created from inv.ext - technology: sky130A
.subckt inv DVDD in out DGND
X0 out.t1 in.t0 DGND.t1 DGND.t0 sky130_fd_pr_nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.44 w=0.42
l=0.15
X1 out.t0 in.t1 DVDD.t1 DVDD.t0 sky130_fd_pr_pfet_01v8 ad=0.252 pd=2.28 as=0.252 ps=2.28 w=0.84
l=0.15
R0 in.n0 in.t1 246.32
R1 in.n0 in.t0 206.153
R2 in in.n0 154.37
R3 DGND DGND.t0 4634.08
R4 DGND DGND.t1 270.61
R5 out out.t0 418.861
R6 out out.t1 273.034|
R7 DVDD DVDD.t0 949.399
R8 DVDD DVDD.t1 398.005
C0 in DVDD 0.106842f
C1 out in 0.039803f
C2 out DVDD 0.10264f
C3 out DGND 0.127322f
C4 in DGND 0.231484f
C5 DVDD DGND 0.77367f
.ends
```

Question 2: Ring Oscillator

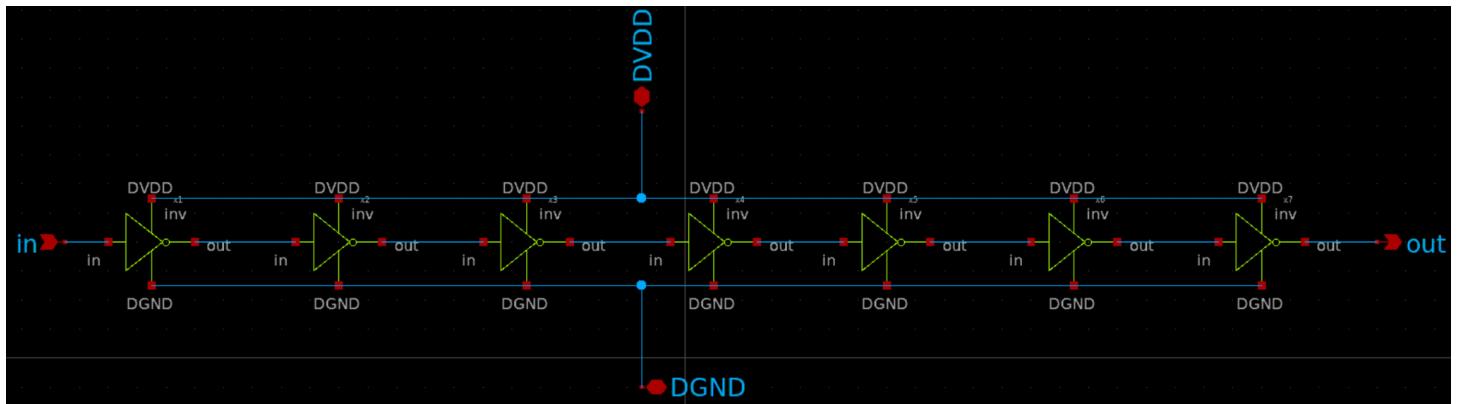
2. Using the inverter layout above, draw the layout of a seven stage ring oscillator shown below.



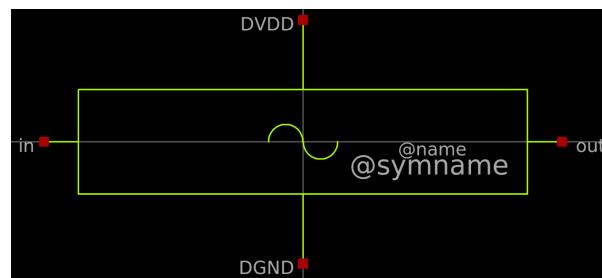
To ensure oscillation in the transient simulation, set the node $V_{out} = 0V$ initially using: .ic v(Vout)=0

- Measure the oscillating frequency for $V_{DD} = 1.8V$ with the layout parasitics.
- Plot the oscillating frequency and time period as a function of V_{DD} for $V_{DD} = 1V$ to $1.8V$ in steps of $0.1V$.
- Compare the frequencies against pre-layout simulation in Assignment 4.

Oscillator Schematic:

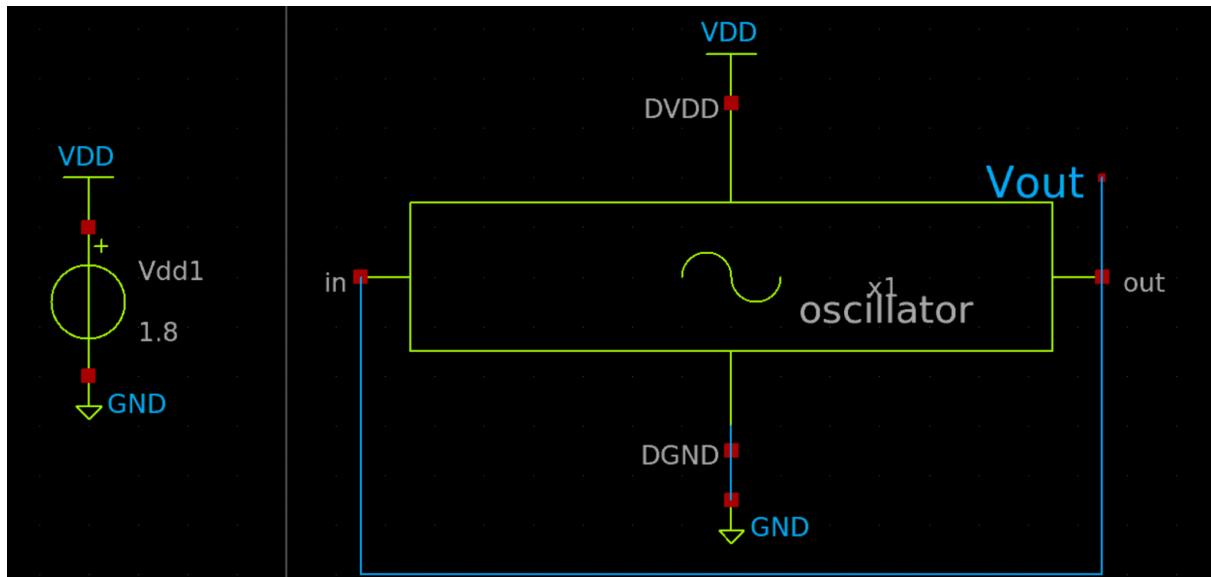


Schematic



Symbol

Circuit Schematic:



Simulation Code:

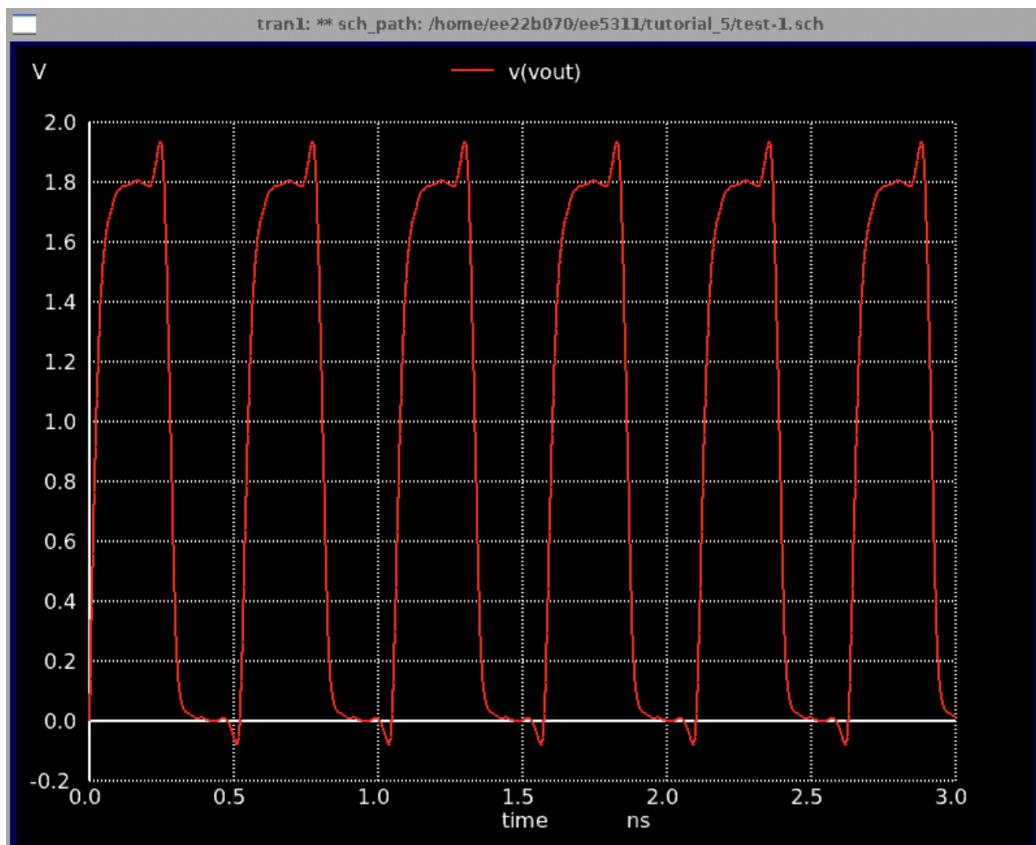
```
Corner: tt
sim
*.include oscillator_extracted.spice
.ic v(Vout) = 0
.control
tran 1p 3n
plot v(Vout)
meas tran t trig V(Vout) val = 0.9 rise = 3 targ V(Vout) val = 0.9 rise = 4
let freq = 1/t
echo Frequency: $&freq Hz
.endc
```

1(a) Post-Layout Measurements:

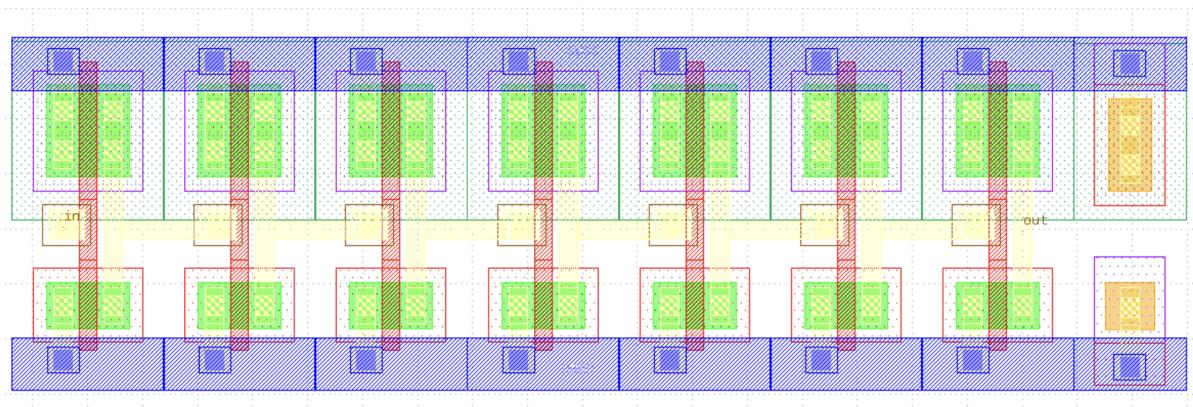
For these measurements, the “.include oscillator_extracted.spice” file is commented out.

```
t          = 5.270397e-10 targ= 1.600536e-09 trig= 1.073496e-09
Frequency: 1.89739E+09 Hz
ngspice 2 -> ■
```

The frequency for post-layout oscillator circuit for $V_{DD} = 1.8 \text{ V}$ is: **1.89 GHz**



V_{out} transient plot to find frequency



Oscillator layout (left - 7 nMOS and 7 pMOS, right - tap)

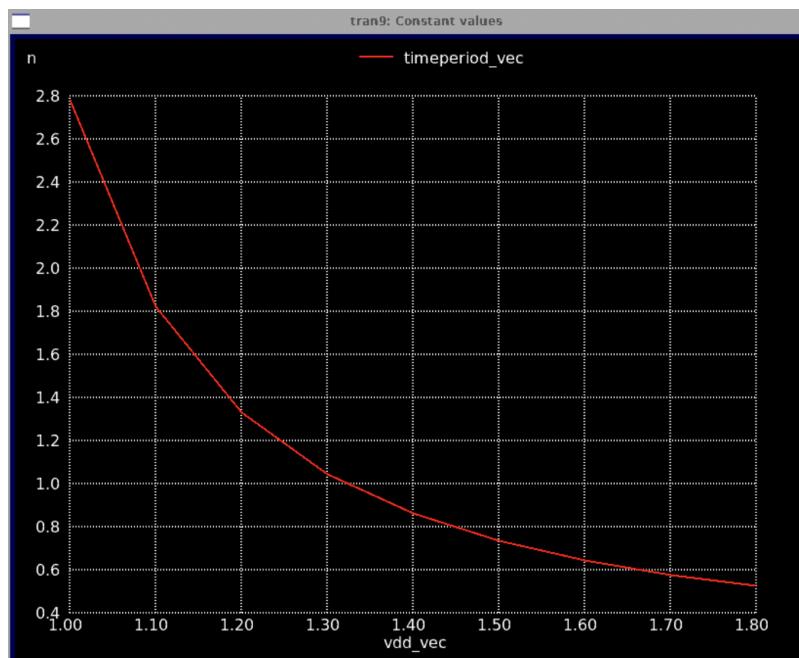
1(b) Simulation Code:

```
sim
.include oscillator_extracted.spice
.param VDDval = 1.8
.ic V(Vout) = 0
.control
let index = 0
let N = 9
let freq_vec = vector(N)
let vdd_vec = vector(N)

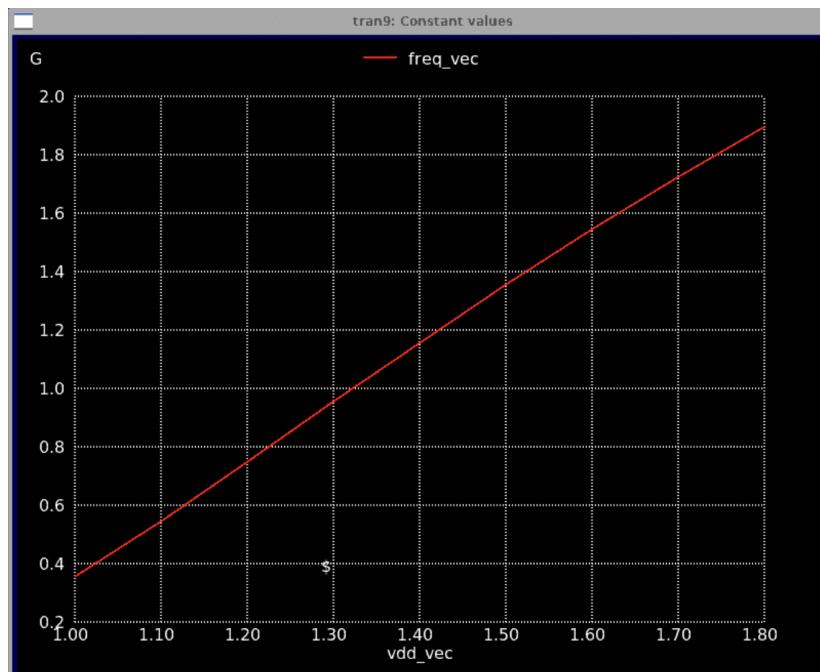
let timeperiod_vec = vector(N)
while index < N
    let vdd = 1.0 + (index * 0.1)
    let vdd_vec[index] = vdd
    let vby2 = vdd/2
    alterparam VDDval = $&vdd
    reset
    tran 1p 10n
    meas tran t trig V(Vout) val = vby2 rise = 3 targ V(Vout) val = vby2 rise = 4
    let freq = 1/t
    let timeperiod_vec[index] = $&t
    let freq_vec[index] = $&freq
    let index = index + 1
    echo Frequency: $&freq Hz
end
print vdd_vec freq_vec
plot freq_vec vs vdd_vec
plot timeperiod_vec vs vdd_vec
.endc
```

Schematic is the same as the 1(a) case

Measurements:



Time Period vs V_{DD} plot post layout



Frequency vs V_{DD} plot post layout

1(c) Pre-layout vs Post-layout:

Pre-layout frequencies:

Index	vdd_vec	freq_vec
0	1.000000e+00	3.766180e+08
1	1.100000e+00	5.707420e+08
2	1.200000e+00	7.743350e+08
3	1.300000e+00	9.790170e+08
4	1.400000e+00	1.179930e+09
5	1.500000e+00	1.374110e+09
6	1.600000e+00	1.559690e+09
7	1.700000e+00	1.735530e+09
8	1.800000e+00	1.901010e+09

ngspice 2 -> █

Post-layout frequencies:

Index	vdd_vec	freq_vec
0	1.000000e+00	3.592830e+08
1	1.100000e+00	5.490790e+08
2	1.200000e+00	7.509990e+08
3	1.300000e+00	9.562550e+08
4	1.400000e+00	1.159400e+09
5	1.500000e+00	1.356940e+09
6	1.600000e+00	1.546630e+09
7	1.700000e+00	1.727050e+09
8	1.800000e+00	1.897390e+09

Inference:

The frequencies have reduced in post layout simulation compared to pre-layout simulation due to the parasitics added from the additional resistance and capacitance of the layout elements.