EC 5311 Digital IC Design: Assignment 7
Adder trees - schematic and simulation

1. Create a schematic for the full adder implemented in verilog. Create a corresponding symbol and a testbench that tests it for all possible input combinations.
2. Use the full adder to construct a 16-bit ripple carry adder and create a testbench to tests it for 20 random inputs.
3. Draw schematic and testbenches for the following 16-bit tree adders using Propagate/Generate modules:
   (a) Brent-Kung adder
   (b) Kogge-Stone adder
   (c) Sklansky adder