

EE6332 - ENDSEM PROJECT — Gate Sizing using Geometric Programming and Branch and Bound

Himanshu Rajnish Borkar - EE22B070

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1 Introduction

Gate sizing is a critical optimization problem in digital circuit design, aiming to meet performance specifications such as delay while minimizing area or power. Due to the combinatorial nature of selecting discrete gate sizes, the problem is generally hard. This report presents a two-phase approach:

- **Phase 1:** Solve the relaxed problem using Geometric Programming (GP) to obtain a continuous solution.
- **Phase 2:** Use a Branch and Bound (BnB) algorithm to convert the continuous solution into a feasible discrete one.

2 Phase 1: Continuous Relaxation with Geometric Programming

In the first phase, we model the gate sizing problem as a geometric program:

- **Variables:** Gate sizes x_i and arrival times A_i
- **Objective:** Minimize total gate area $\sum x_i$
- **Constraints:** Timing constraints between gates and an upper bound on total delay:

$$T_{\text{wall}} \leq T_{\text{spec}} = 1.3 \cdot T_{\text{wall_solved}}$$

The solution yields optimal (but fractional) gate sizes and timing information. These values serve as a lower bound and a guide for the next phase.

Plots and Visualizations

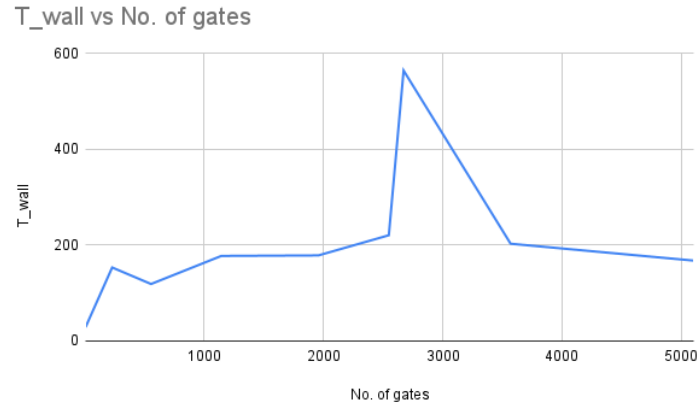
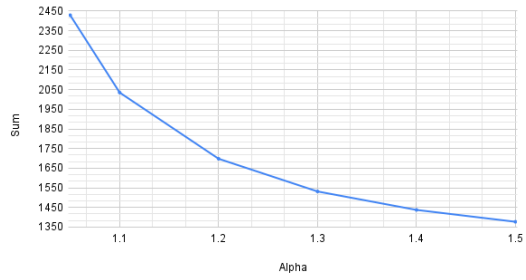


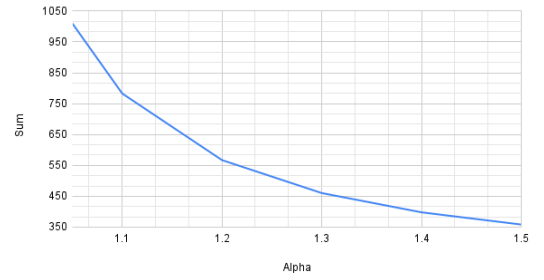
Figure 1: T_{wall} vs Number of Gates

C1908; $T_{\text{wall}} = 177.6$



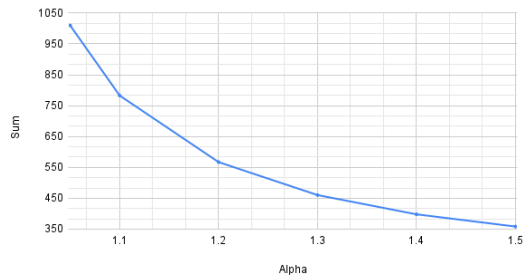
(a) A_{min} vs T_{spec} (c1908)

C17; $T_{\text{wall}} = 28.8$



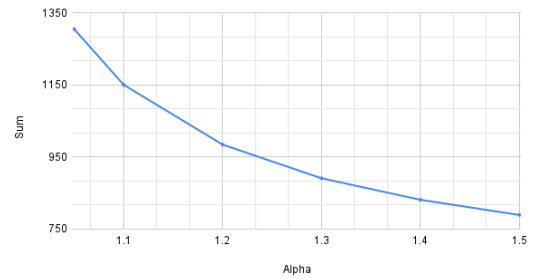
(b) A_{min} vs T_{spec} (c17)

C432; $T_{\text{wall}} = 153.4$



(c) A_{min} vs T_{spec} (c432)

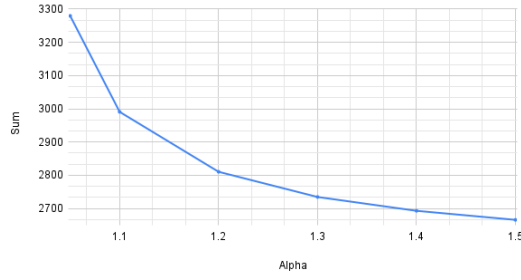
C880; $T_{\text{wall}} = 118.9$



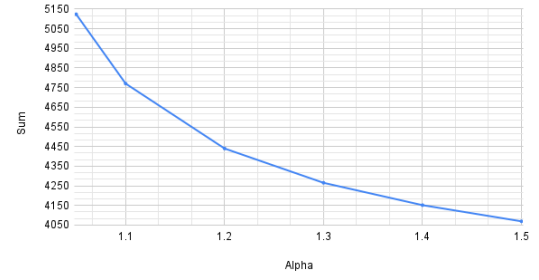
(d) A_{min} vs T_{spec} (c880)

Figure 2: A_{min} vs T_{spec}

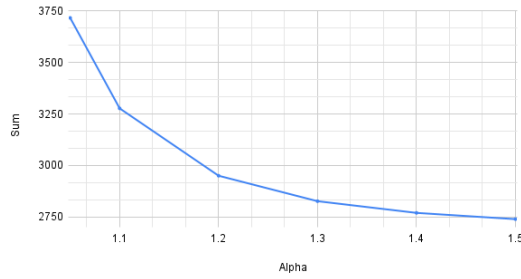
C3540; Twall = 220.7

(a) A_{\min} vs T_{spec} (c3540)

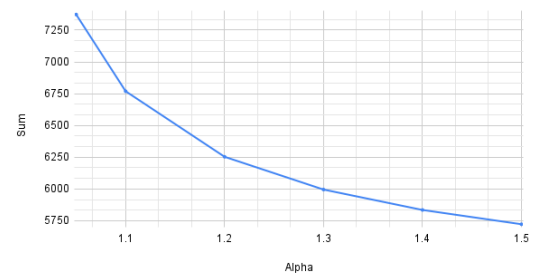
C5315; Twall = 203.1

(b) A_{\min} vs T_{spec} (c5315)

C6288; Twall = 564.6

(c) A_{\min} vs T_{spec} (c6288)

C7552; Twall = 167.9

(d) A_{\min} vs T_{spec} (c7552)Figure 3: A_{\min} vs T_{spec}

Column 1	▼	#	Twall	▼	#	1.05	▼	#	1.1	▼	#	1.2	▼	#	1.3	▼	#	1.4	▼	#	1.5	▼
c432			153.4			1009.9			782.8			567.1			460.3			397.9			358.3	
c17			28.8			199.1			182.7			156.3			136.1			120.2			107.4	
c880			118.9			1305.5			1150.8			984.8			891.2			831.4			789.3	
c1908			177.6			2429.1			2035.2			1698			1531.5			1437.5			1377.1	
c3540			220.7			3279.6			2990.7			2810.4			2734.6			2693			2665.8	
c5315			203.1			5123.7			4770.5			4440			4265.3			4151.6			4069.3	
c6288			564.6			3716.9			3277.1			2949.7			2825.9			2769.1			2738.7	
c7552			167.9			7373			6769.1			6253.3			5995.4			5834.9			5722.6	

Figure 4: Dataset

Analysis Questions

Q1. Look at the critical path and analyze the gate sizes on the critical path. What do you observe on noncritical paths?

Ans: The critical path contains the gates with larger sizes to reduce the delay as much as possible, whereas the non-critical paths have smaller gate sizes in order to reduce the total area and save power.

Q2. Analyze the effect of discretizing the continuous solution. Can you think of how you can identify a discrete solution is likely to satisfy the timing constraint?

Ans: One way to discretize the solution is to choose a more relaxed T_{spec} , such as $1.35 \times T_{\text{wall}}$ instead of $1.3 \times T_{\text{wall}}$, and then round the continuous solution up to the

ceiling value to obtain a discrete solution. In this way, even with the relaxed T_{spec} , there is no timing violation.

Q3. If you were a standard cell designer and you had to identify the drive strength of various gates (INV, NAND2-4, NOR2-4), what would you decide?

Ans: We consider each gate, for example the NAND2 gate and plot a histogram of the sizes used in the circuit. This distribution typically resembles a bell-curve, and the most frequent size is chosen as the standard discrete drive strength.

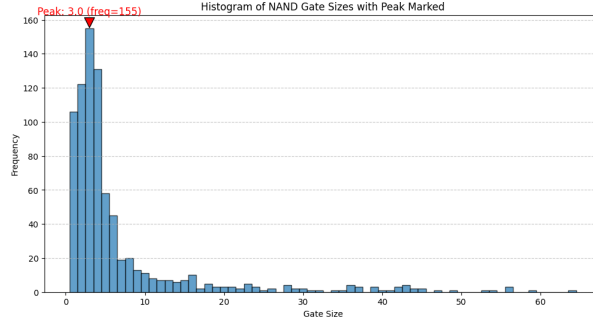


Figure 5: Histogram of gate sizes for NAND2 gates

3 Phase 2: Discrete Optimization with Branch and Bound

While the continuous solution from Phase 1 is optimal in theory, practical constraints require gate sizes to be discrete. To address this, we use a Branch and Bound (BnB) algorithm tailored to the problem structure.

3.1 Key Concepts

- 1. Initial Setup:** Use the solution from Phase 1 to initialize the BnB search and set area bounds.
- 2. Branching Rule:** Select the variable (gate size) with the largest fractional part and highest priority to branch on.
- 3. Bounding:** If a solution exceeds the known best area or violates feasibility, prune that branch.
- 4. Termination:** Stop when a valid integer solution is found within bounds or when a time/resource limit is reached.

3.2 Branch and Bound Python Code

```

1 def branch_and_bound(constraints_input):
2     num_vars = N
3     best_solution = [np.inf] * num_vars
4     best_area = np.inf
5     fewest_fractions = np.inf
6     best_partial_solution = [np.inf] * num_vars
7     best_partial_constraints = []
8
9     timeout = min(100 * num_vars, 1800)
10    start_time = time.time()
11
12    def recurse(current_constraints, last_fraction_count=np.inf):
13        nonlocal best_solution, best_area, fewest_fractions
14        nonlocal best_partial_solution, best_partial_constraints
15
16        if time.time() - start_time > timeout:
17            return
18
19        try:
20            candidate, area = solve_model(current_constraints)
21        except (PrimalInfeasible, UnknownInfeasible, Infeasible,
22                subprocess.CalledProcessError, Exception):
23            return
24
25        if area > best_area or area > 1.4 * initial_area:
26            return
27
28        fraction_count = sum(
29            abs(round(candidate[i]) - candidate[i]) > tolerance
30            for i in range(num_vars)
31        )
32        print(fraction_count, area)
33
34        if fraction_count < fewest_fractions:
35            fewest_fractions = fraction_count
36            best_partial_solution = candidate.copy()
37            best_partial_constraints = current_constraints.copy()
38
39        if is_integer_vector(candidate, num_vars):
40            if area < best_area:
41                best_solution = candidate
42                best_area = area
43                return
44
45        target_index = None
46        max_fraction = -1
47        for i in range(num_vars):
48            frac_part = abs(round(candidate[i]) - candidate[i])
49            if frac_part > tolerance and round(candidate[i], 1):
                if critical_flag[i] and frac_part > max_fraction:

```

```

50         max_fraction = frac_part
51         target_index = i
52
53     if target_index is None:
54         for i in range(num_vars):
55             frac_part = abs(round(candidate[i]) - candidate[i
56             ])
57             if frac_part > tolerance and frac_part >
58                 max_fraction and round(candidate[i], 1):
59                 max_fraction = frac_part
60                 target_index = i
61
62     if target_index is None:
63         return
64
65     low_val = int(np.floor(candidate[target_index]))
66     high_val = int(np.ceil(candidate[target_index]))
67
68     left_constraints = current_constraints.copy()
69     left_constraints.append(x[target_index] <= low_val)
70     recurse(left_constraints, fraction_count)
71
72     right_constraints = current_constraints.copy()
73     right_constraints.append(x[target_index] >= high_val)
74     recurse(right_constraints, fraction_count)
75
76     recurse(constraints_input)
77
78     return best_solution, best_area, best_partial_solution,
79         best_partial_constraints

```

Listing 1: Branch and Bound Implementation

3.3 Final Output

After the BnB algorithm terminates, the final output includes:

- Best integer solution found (gate sizes x_i)
- Total area of the solution
- Optionally, a rounded version of the best partial (fractional) solution

4 Conclusion

The two-phase gate sizing approach combines the efficiency of Geometric Programming with the rigor of Branch and Bound to provide discrete, high-quality solutions that meet timing constraints. This strategy effectively balances optimality with feasibility in practical digital design workflows.