EE6332 Midsem Jan-May 2025

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Q1.
Assume x = {x_1, x_2, ….. x_N} are free variables such that $x_i > 0$ for all i. Let $g_k(x)$ be monomials and $f_j(x)$ be posynomials. Argue why the following are true or false:

(i) $g_k(.)/f_j(.) \geq 1$ is a valid constraint in a Geometric Program.
(ii) $(\sum_{j=1}^{M} f_j(.))^n$ is a posynomial where n is a positive integer
(iii) $c + f_j(.)$ is a posynomial for $c \in R$

Q2.
Consider a circuit with N inputs and M outputs. Now, we make partitions M_1 and M_2 in the outputs such that $M_1 + M_2 = M$. We consider 3 circuits where:

- Circuit C_1 with N inputs and M_1 outputs.
- Circuit C_2 with N inputs and M_2 outputs.
- Circuit C_3 with N inputs and M outputs.

For the above circuits, the T_{wall} is given by $T_{1\text{-}3}$ respectively and for a given T_{spec}, the A_{min} (area minimum) is given as $A_{1\text{-}3}$. Find the relation between the T_{wall} of each circuit and the A_{min} of each circuit. Also determine a T_{spec}.

Q3.
Consider a path with the following gates: Inverter, NOR2, NAND2, NAND3, NOR3; in that order, output load capacitance C_{LOAD} and maximum input capacitance C_{MAX}. Find the T_{WALL} for the given circuit. Also consider each permutation of the order of placing the given gates in the path, determine the order which gives us minimum and maximum area for the same T_{WALL}. Note that area of the path is given by the sum of the sizes of the gate.

Q4.
Assume that a single NMOS transistor of width W is discharging a capacitor from VDD to 0.5VDD and takes a time τ. Starting from the level-1 SPICE model, show that a two transistor stack of twice the width, under identical conditions, will discharge the capacitor in the same time τ. What assumptions does one have to make for this to be true?