A2. Verilog Parser

Mark as done

Opened: Thursday, 13 March 2025, 12:00 AM
Due: Thursday, 20 March 2025, 11:59 PM

As a lead-up to the project where you have to perform gate sizing for arbitrary combinational circuits, you need a Verilog parser. In this assignment, you are expected to **use ChatGPT** and do the following:-

1. Parse a given structural netlist and load it into a data structure like a Directed Acyclic Graph(DAG)
2. Traverse the graph from the primary inputs to the primary outputs along various paths. Identify the path with the largest logic depth i.e. the number of gates should be the highest in this path.
3. Print for each gate in the circuit the list of fanout gates. For example in c17 you

NAND2_2 - NAND2_3, NAND2_4

Attached are sample Verilog netlists. A couple of important points:-

1. The gates in the circuits are only inverter, NAND, and NOR (2-4 inputs)
2. The format for any gate is of the form: **type** {INST_NAME} ({OUT}, {IN_1}, {IN_2}, ... {IN_N}). For example

nand NAND2_1 (N10, N1, N3);

is a **NAND2** gate with inputs N1 and N3 and output N10.