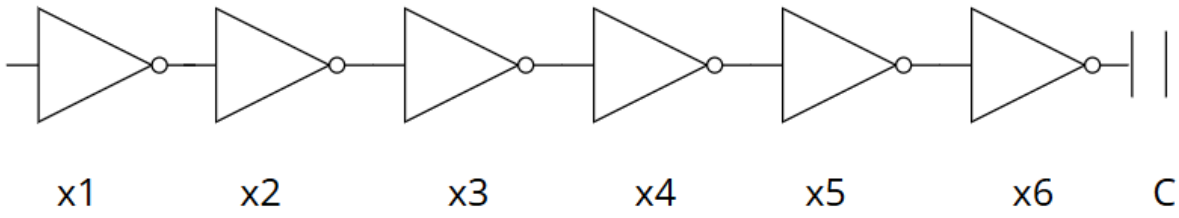
Assignment - 1

Following the MOSEK setup on your python environment, the objective of the assignment is to find the Twall and minimum area (under given timing specifications) of the circuit below



1. Finding T_{wall} of the given circuit:

- Define the total number of gates in the circuit.
- Create Logical Effort and Parasitic Delay Lists
- Setup the Objective and Constraints to Minimize Timing
- Formulate the delay equation using logical effort and parasitic delay.
- Add constraints to ensure gate sizes remain within valid limits.
- Use GPkit to solve the optimization model.
- Extract the optimized gate sizes and report the total delay.

2. Optimize circuit for Minimum Area

- Change the objective function to minimize the total gate area instead of delay.
- Modify constraints to ensure timing meets a given timing specification.
- Solve the new model and report the optimized gate sizes for minimum area.

Assumptions:

- Intrinsic delay of inverter is 5ps
- Maximum gate size of 64x and minimum size of 1x
- Capacitance at the end of the inverter chain (C) is 100 times the unit sized inverter
- Parasitic effort and logical effort values are ideal

Deliverables:

- Report gate sizes for the circuit for optimized timing (Twall)
- Report gate sizes for the area minimised circuit with a timing specification of 1.2 x T_{wall}