

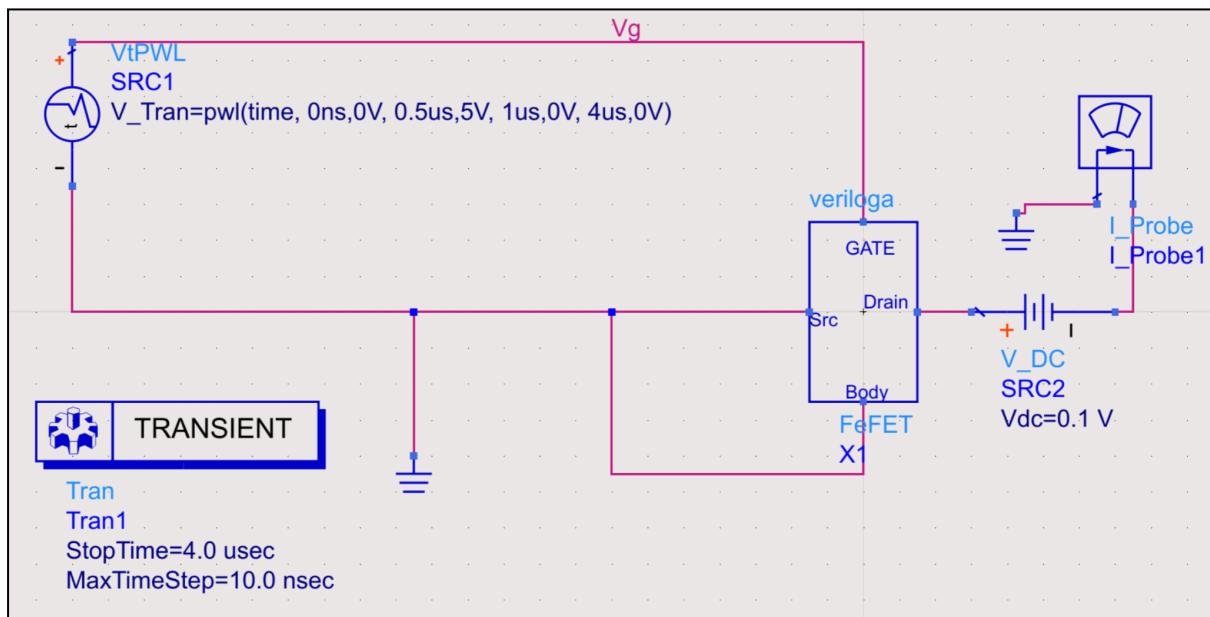
EE6347: Assignment 3 Report

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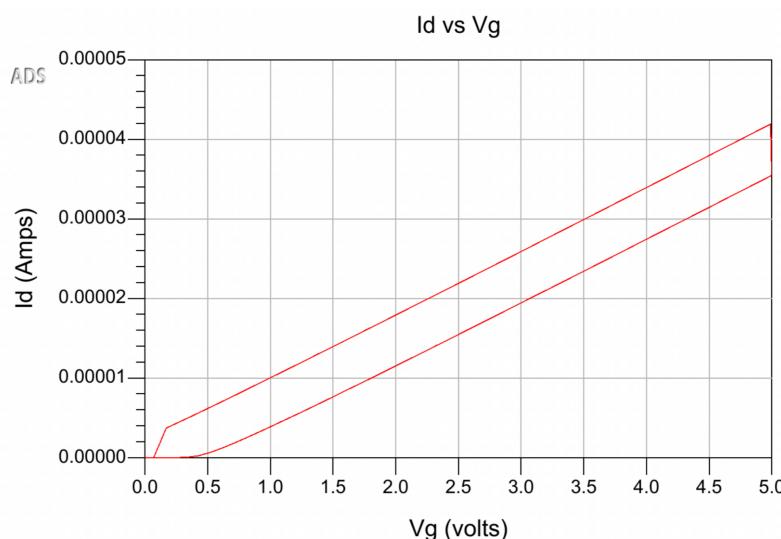
Date: 28.09.2025

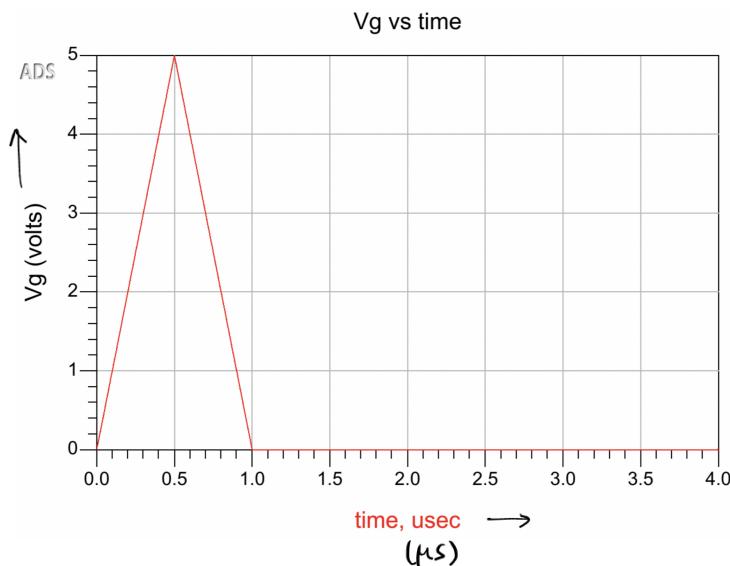
1. Show the I_d - V_g hysteresis of an FeFET using the model file provided. Apply a 5V, 1 μ s triangular pulse at gate, with $V_D = 0.1V$, $V_S = V_B = 0V$.

- (a) Take a screenshot of the schematic showing the biasing and the transient simulation conditions.



- (b) Show the V_g – time and I_d - V_g plots. Clearly label the axes and the show units.





Triangular pulse of 5V for 1μsec

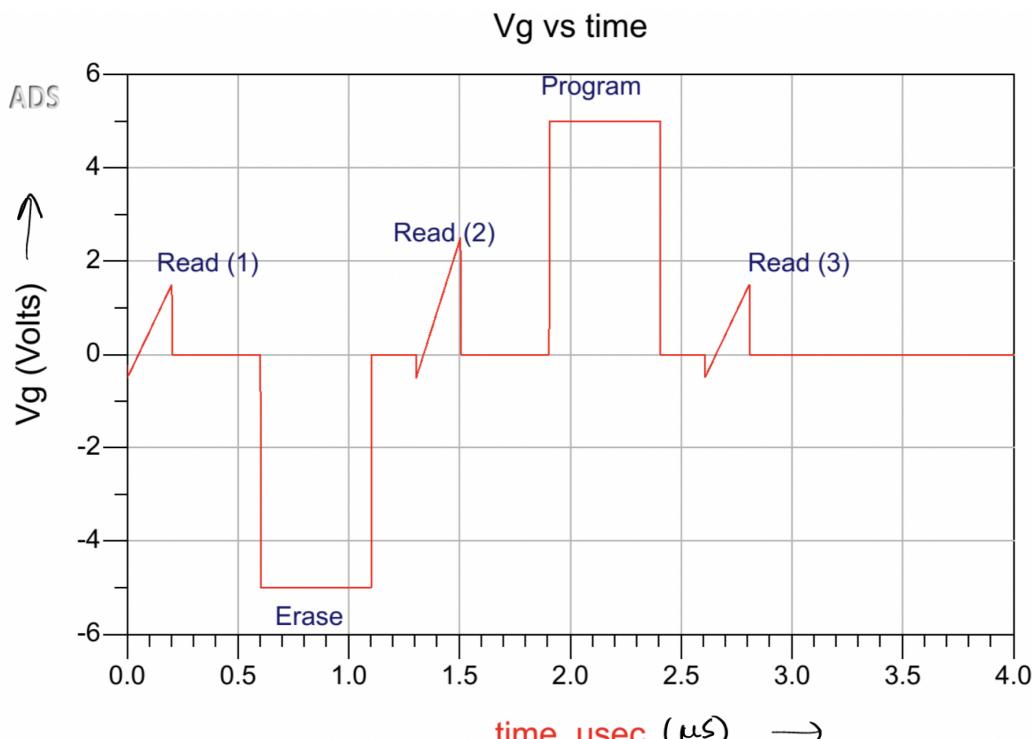
2. Demonstrate Read/Erase/Read/Program/Read operations on a single FeFET cell; in that specific order.

Read: Sweep the gate voltage from -0.5V to 1.5V over 200ns to measure the threshold voltage, keeping $V_D = 0.1V$ and all other terminals grounded ($V_s = V_B = 0V$).

Program: Apply a 5V, 500ns pulse to program the FeFET.

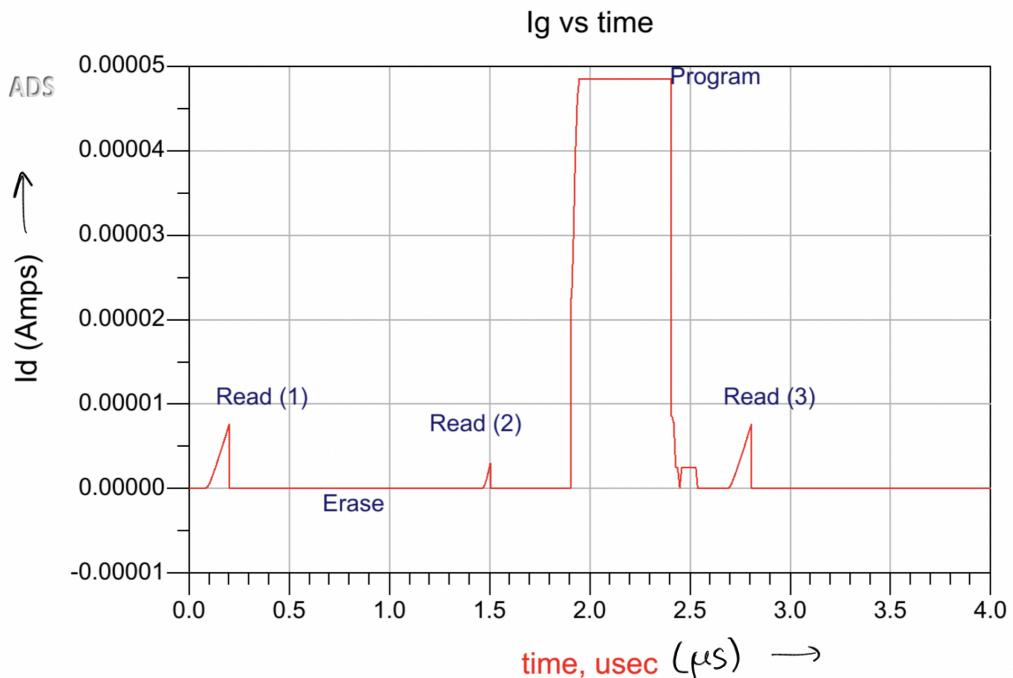
Erase: Apply a -5V, 500ns pulse to erase the FeFET.

(a) Plot Vg-time. Label the axes and show the units.



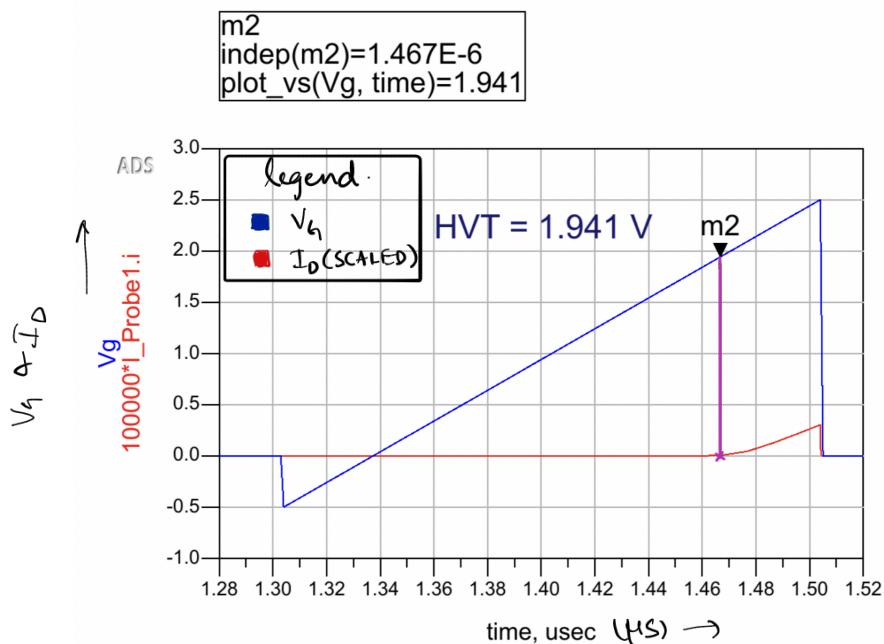
Read/Erase/Read/Program/Erase input to FeFET

(b) Plot I_d -time. Label the axes show the units.

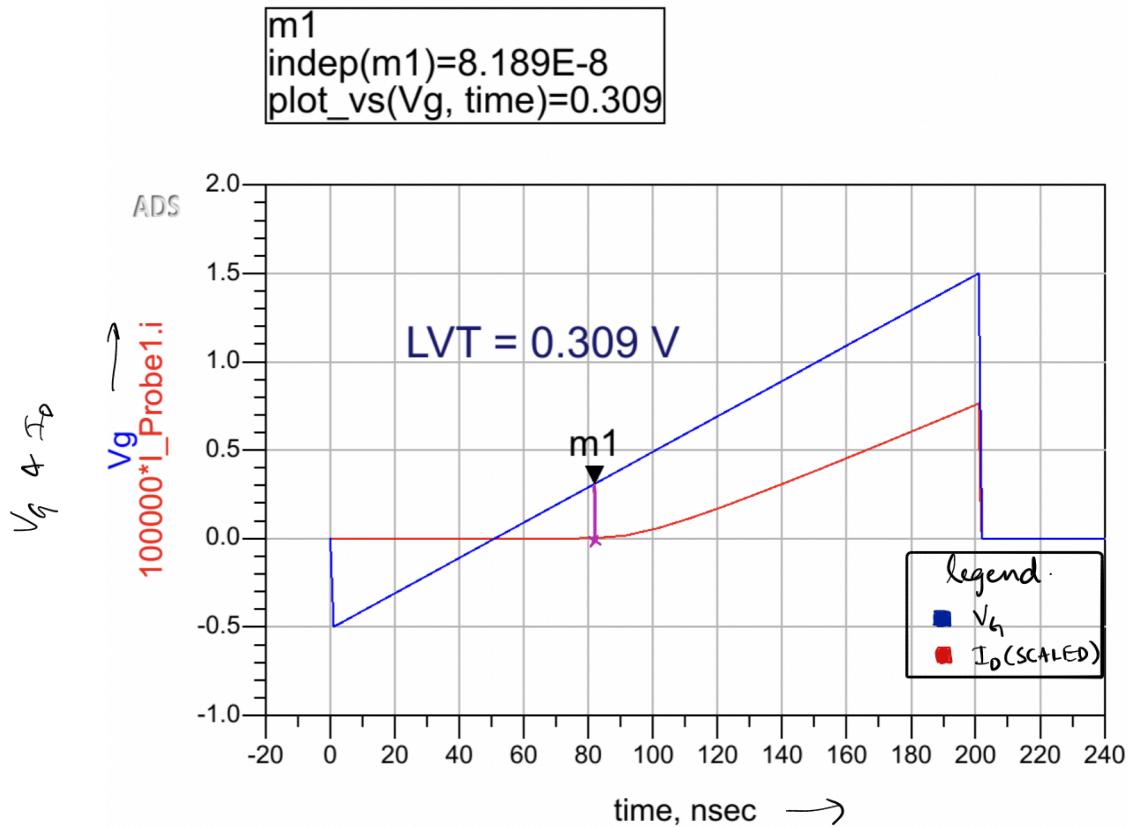


Note that $I_D = 0$ for ERASE, and FeFET has a higher threshold voltage for the read after erase.

(c) Calculate the threshold voltages for the HVT and the LVT states, respectively

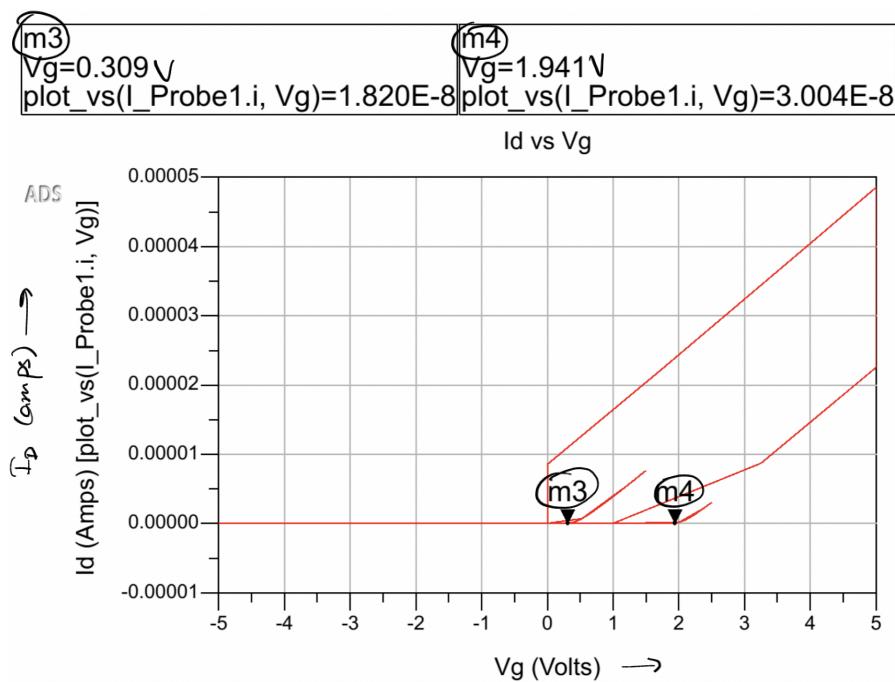


Therefore, from the V_G vs time and scaled I_D vs time we get **HVT = 1.941 V**



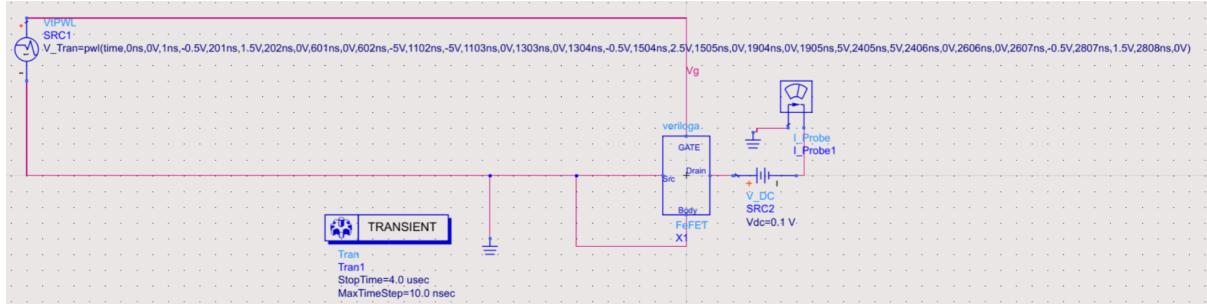
Similarly, from the V_G vs time and scaled I_D vs time we get **LVT = 0.309 V**

We verify this from the I_d vs V_g plot as shown below:



HVT & LVT values

	HVT	LVT
Value:	1.941 V	0.309 V



Schematic for Question 2