

# EE6347: Assignment 2 Report

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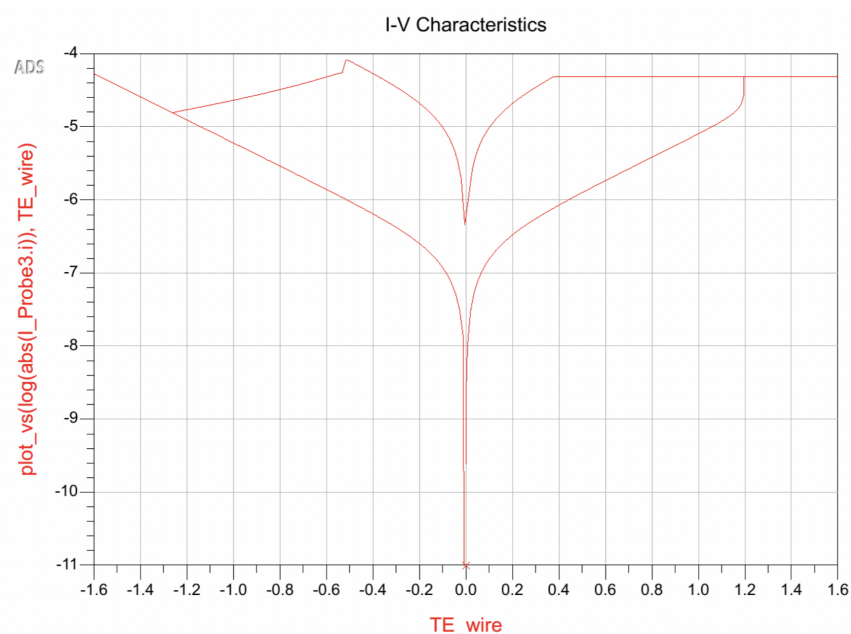
You are given an incomplete Verilog-A code to implement the Stanford model for a RRAM device.

**(a) Your first job is to complete the model. Do so by defining the in/out and other electrical nodes; choosing appropriate values for the parameters (some parameter values are not given); and solving appropriate equations to calculate the current, gap, and the temperature. Upload the completed code as a separate text file.**

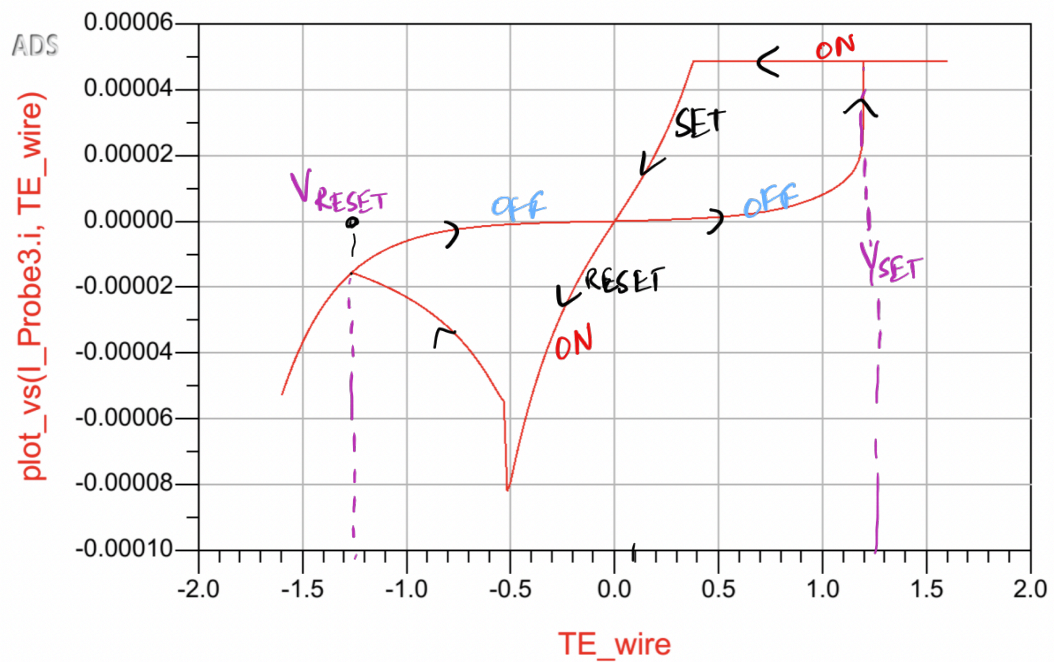
**Answer:** Code is included in the zip file.

**(c) Fit the model you have created using the experimental SET and RESET data provided in two separate csv files. You have to adjust the model parameters to match the model with the experiment. Plot the simulated I-V along with the experimental data in a semi-log plot.**

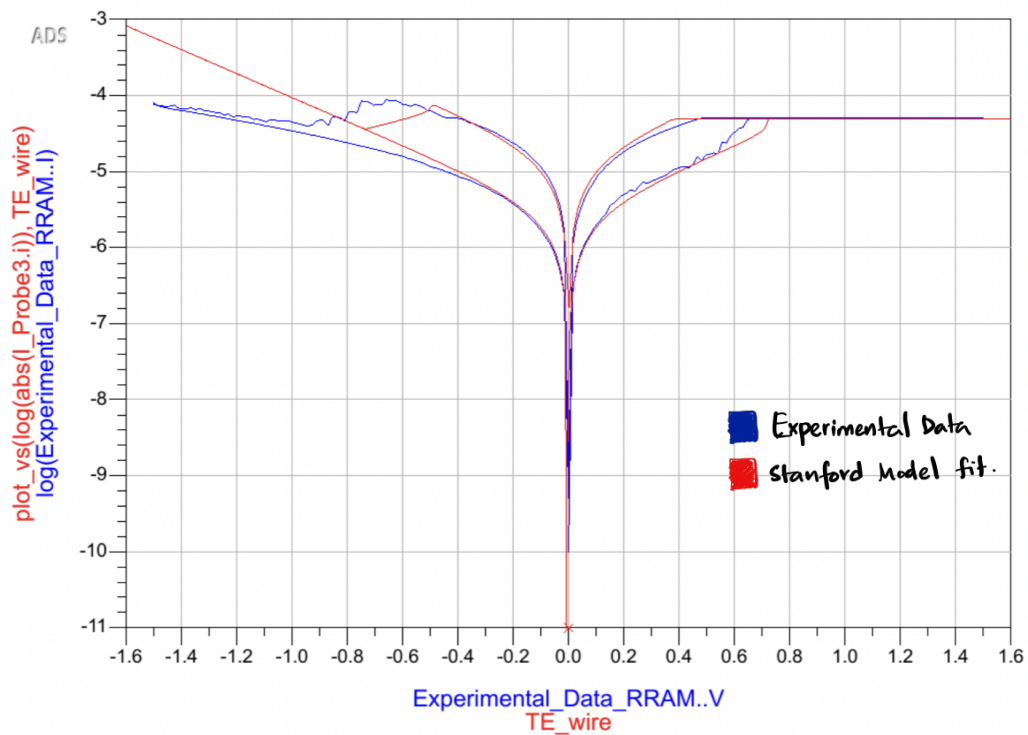
I have preferred to fit the model to the experimental data first and then carry out the tasks in section (b).



Given above is the I-V plot for the parameters given to us in the code.



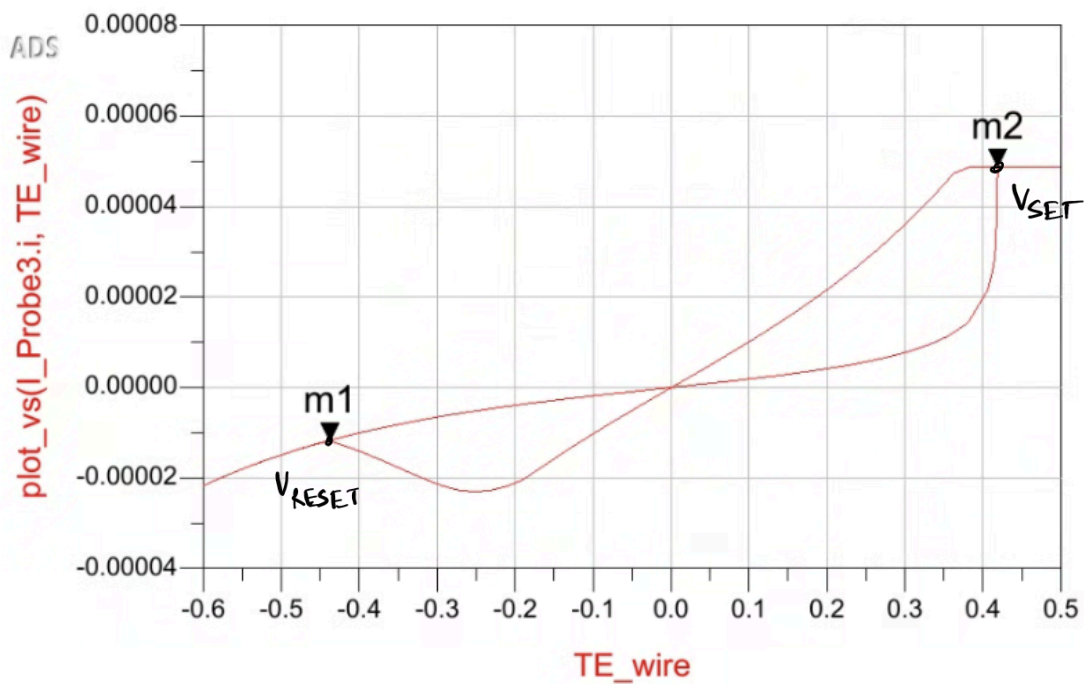
The I-V characteristics are shown above before the model is fitted with the Experimental data



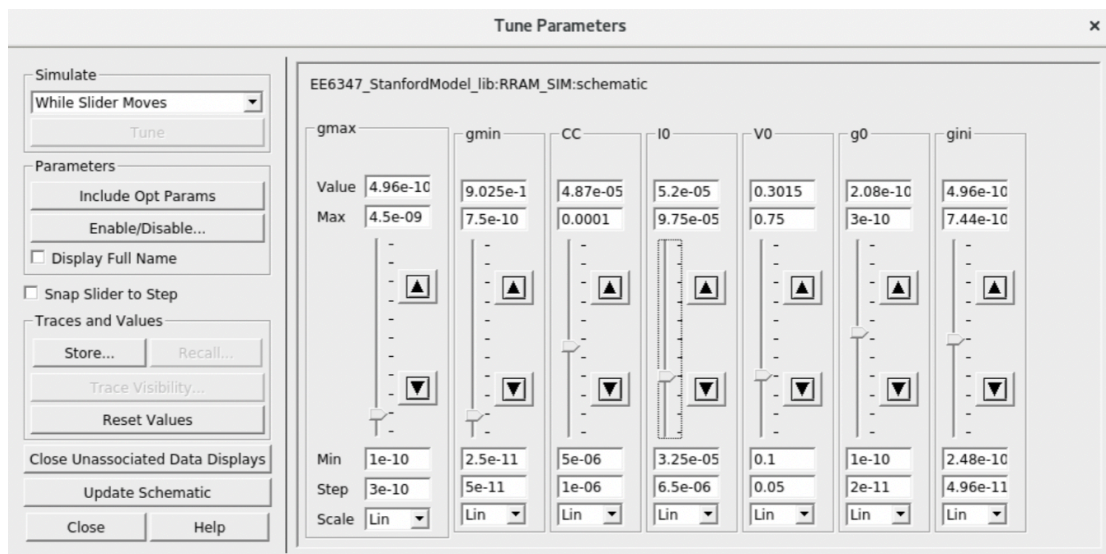
Given above is the I-V Plot of the RRAM with altered params to fit the experimental values

```
m2
TE_wire=0.419V
plot_vs(I_Probe3.i, TE_wire)=4.870E-5
```

```
m1
TE_wire=-0.438 V
plot_vs(I_Probe3.i, TE_wire)=-1.178E-5
```



Given above is the I-V Characteristics AFTER the model is fit with exp. data



Final values of the fitting parameters. (other parameters are available in the code)

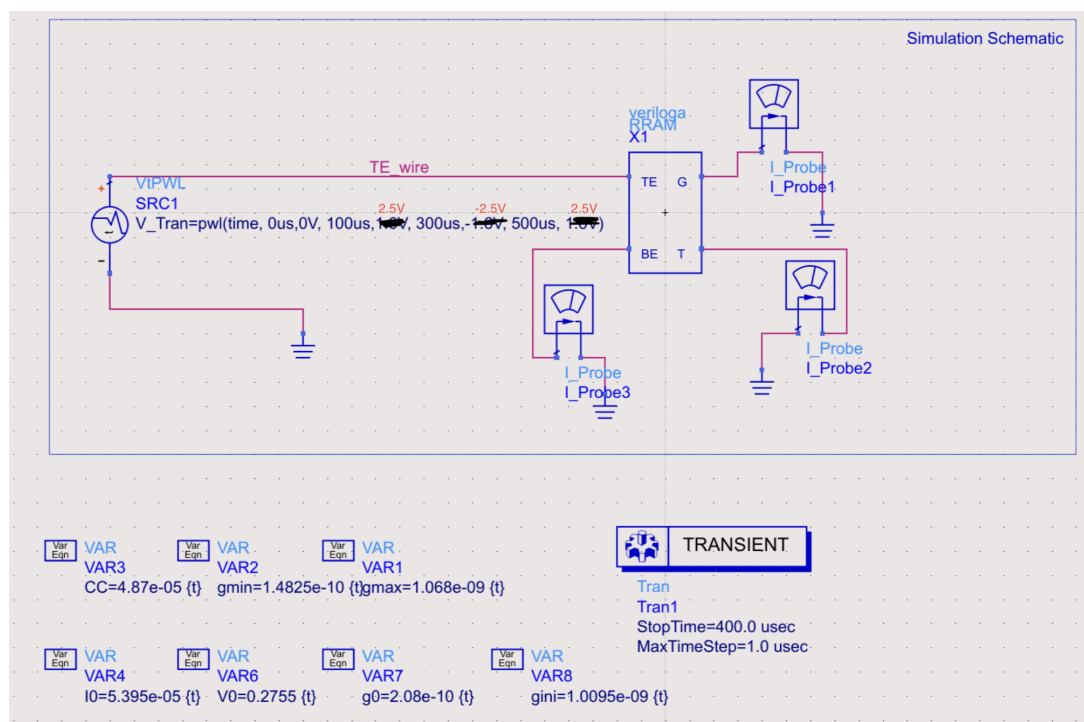
Note that I have set gini to be equal to gmax - the device is in RESET state.

**(b) Now demonstrate bipolar resistive switching using the model you have created.**

*(i) First, create a schematic for running transient simulations on your device. You should also measure the applied voltage (V) and the resulting current (I) in the device. Show the schematic you have created in a separate document file.*

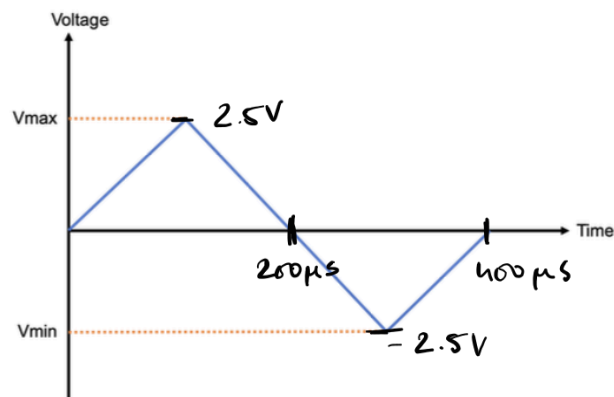
**Answer:**

Schematic:



*(ii) Now, demonstrate SET and RESET operation using a voltage ramp as shown below. Make sure that  $V_{max} \geq V_{SET}$  and  $|V_{min}| \geq |V_{RESET}|$ . Note that you can control  $V_{SET}$  and  $V_{RESET}$  by changing the device parameters. Plot the simulated I-V characteristics of the device in a semi-log plot. Use a ramp rate of 2V/min.*

Answer: The ramp input given is:



We take the amplitude of the waveform to be from +2.5V to -2.5V and the timeperiod of the ramp is 400  $\mu$ sec.

We now consider the  $V_{SET}$  and  $V_{RESET}$  which are given the following values from the I-V Plot of the fitted model:

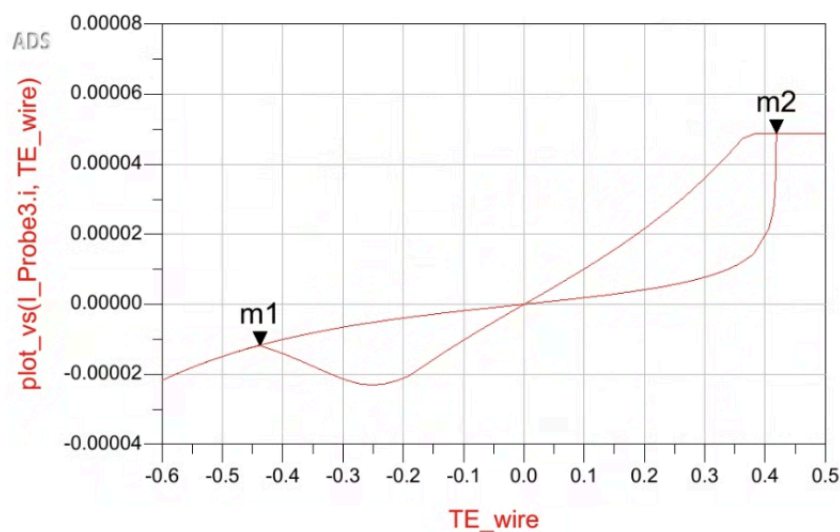
$$V_{SET} = 0.9 \text{ V}$$

$$V_{RESET} = -0.9 \text{ V}$$

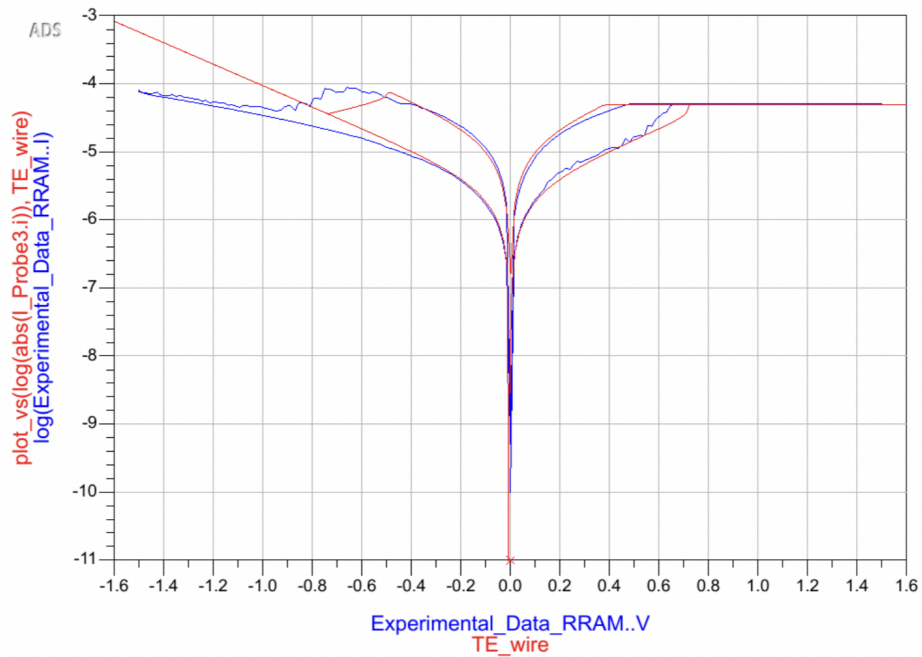
We required a higher value of  $V_{SET}$  and  $V_{RESET}$  to make sure that the device functions appropriately in Program/Erase operations.

```
m2
TE_wire=0.419V
plot_vs(I_Probe3.i, TE_wire)=4.870E-5
```

```
m1
TE_wire=-0.438V
plot_vs(I_Probe3.i, TE_wire)=-1.178E-5
```



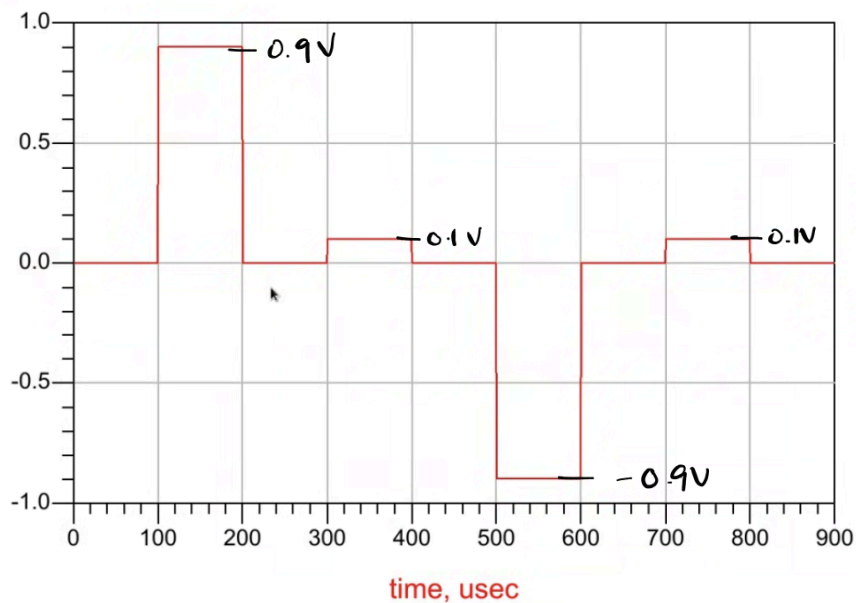
The SET and RESET states are mentioned in the graph given above.



The above graph's Red plot is the I-V Characteristics of the device.

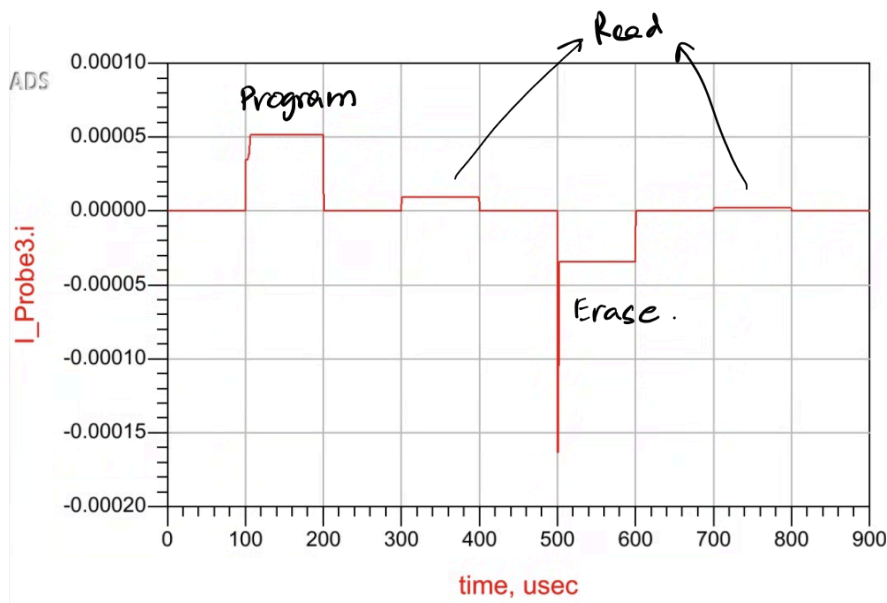
(iii) Next, perform program/erase operation on the memory cell using voltage pulses. Use a write-and-verify scheme as shown below. Use a pulse width of  $100\ \mu\text{s}$  and duty cycle of 50%. Use  $V_{\text{read}} = 0.1\text{V}$ . Use appropriate  $V_{\text{SET}}$  and  $V_{\text{RESET}}$  amplitudes. Calculate the SET and RESET energy.

**Answer:** Input waveform:

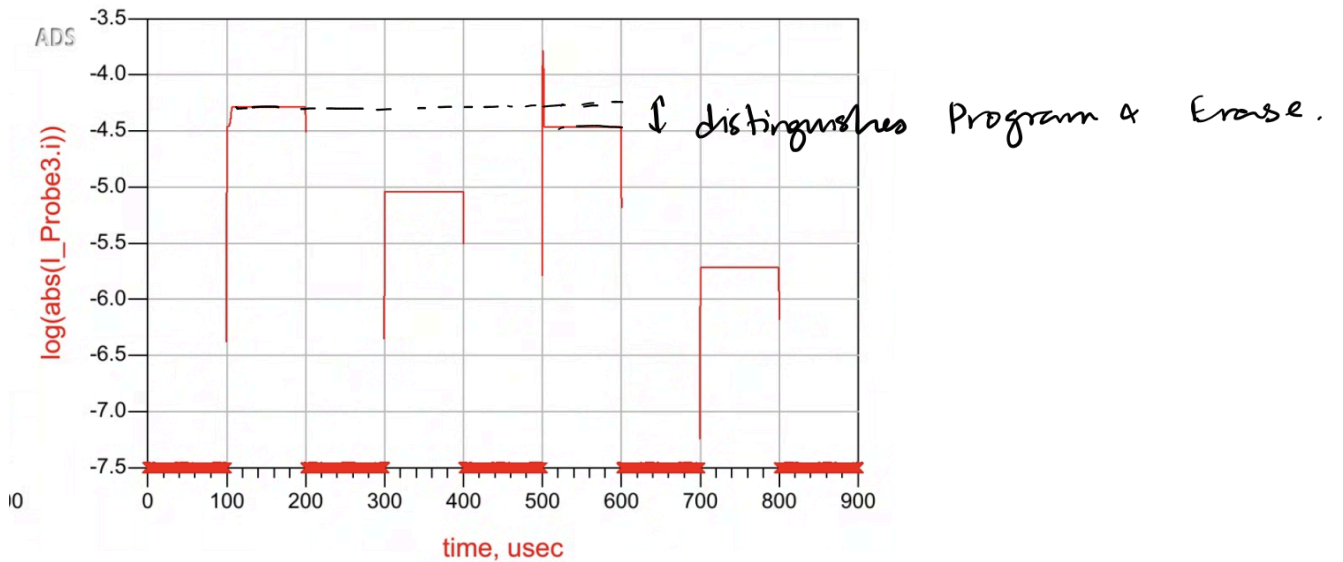




Output current through the device:

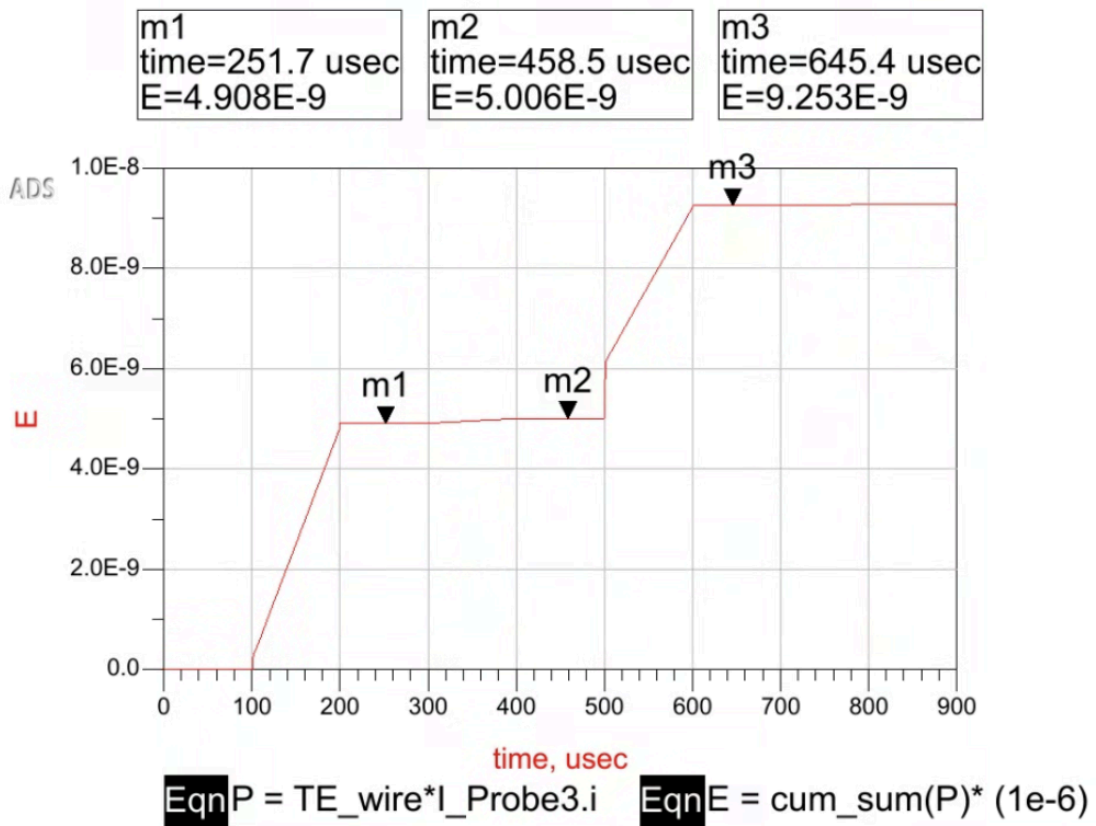


Output semilog variation:



Note: The reason for 2<sup>nd</sup> read having lesser value of current is because the device is in OFF state.

Energy of RESET and SET:



Therefore, the  $E_{SET} = E_{m1} = 4.9 \text{ nJ}$

and,  $E_{RESET} = E_{m3} - E_{m2} = 4.247 \text{ nJ}$