PROJECT REPORT

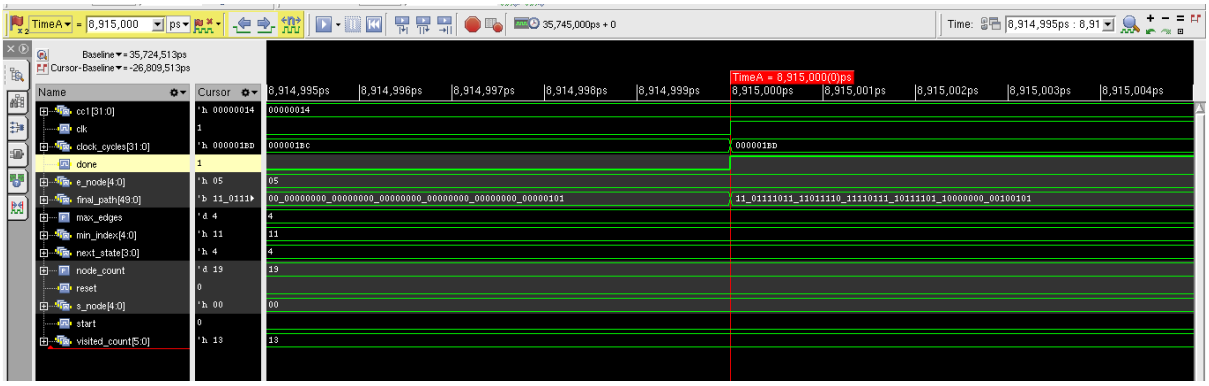
Hardware implementations of Dijkstra's algorithm are popular for applications requiring fast and efficient pathfinding, such as in network routing, autonomous vehicles, and robotics.

Despite the challenges, the parallel processing capabilities of modern hardware accelerators make them well-suited for high-performance adaptations of Dijkstra’s algorithm.

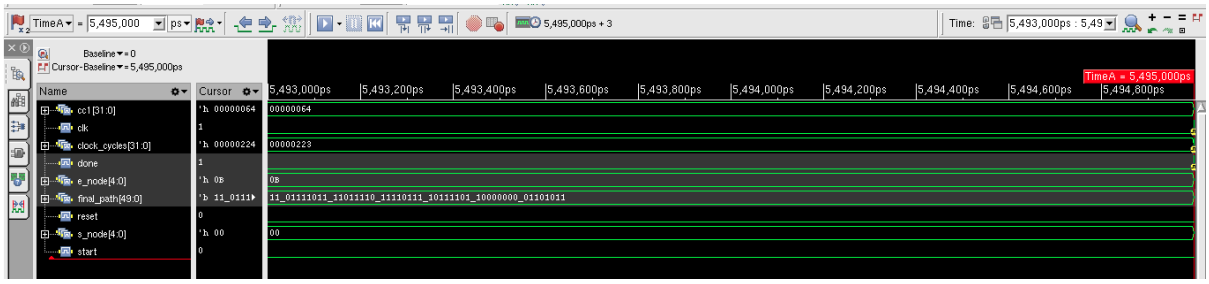
COMPARISONS :

WAVEFORMS

PARALLELISED CODE

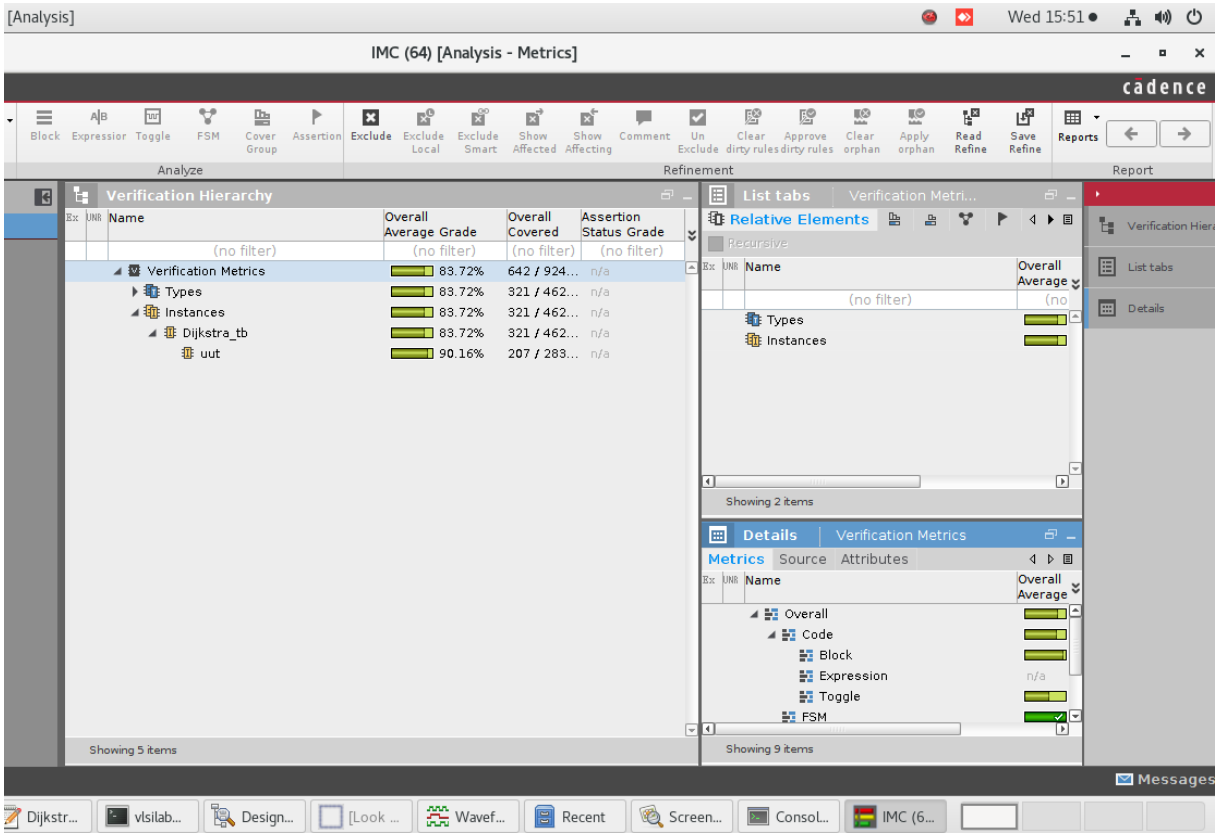


UNPARALLELISED CODE:

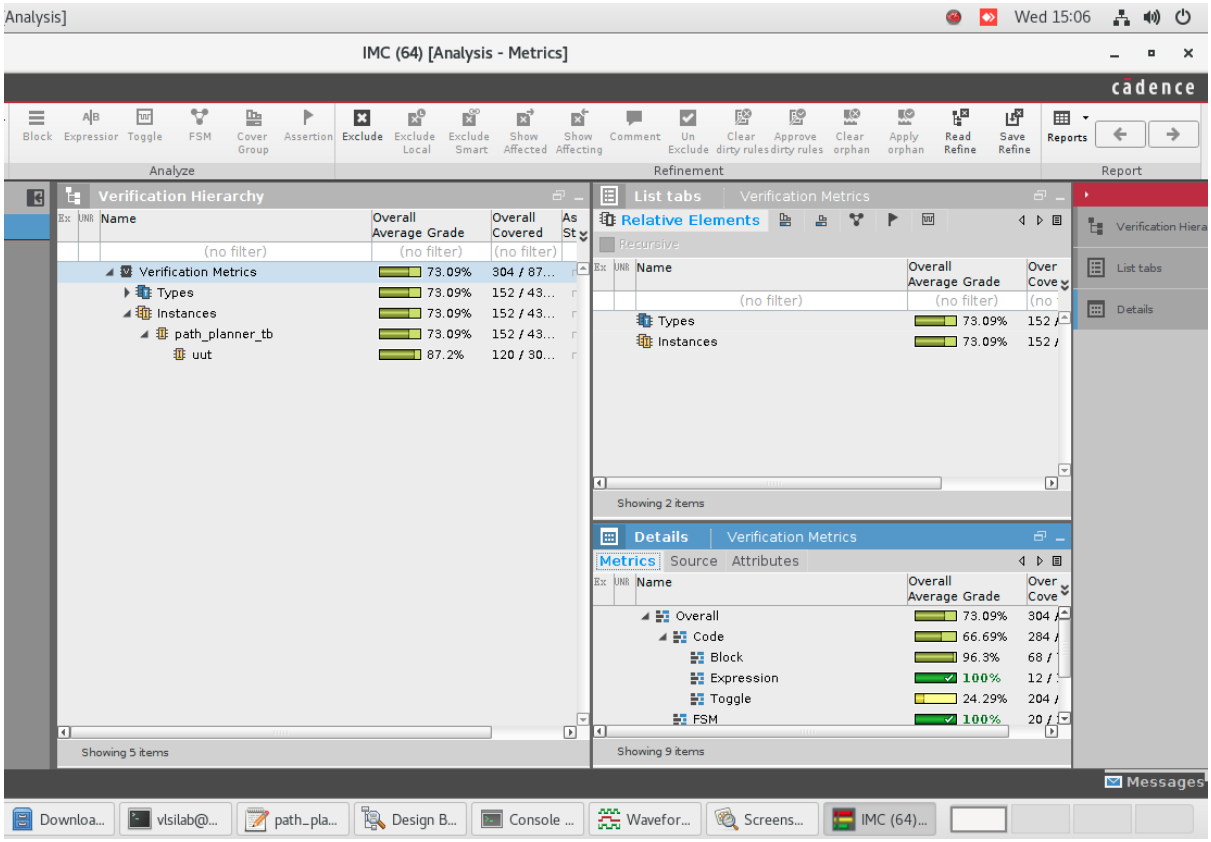


CODE COVERAGE

PARALLELISED CODE :

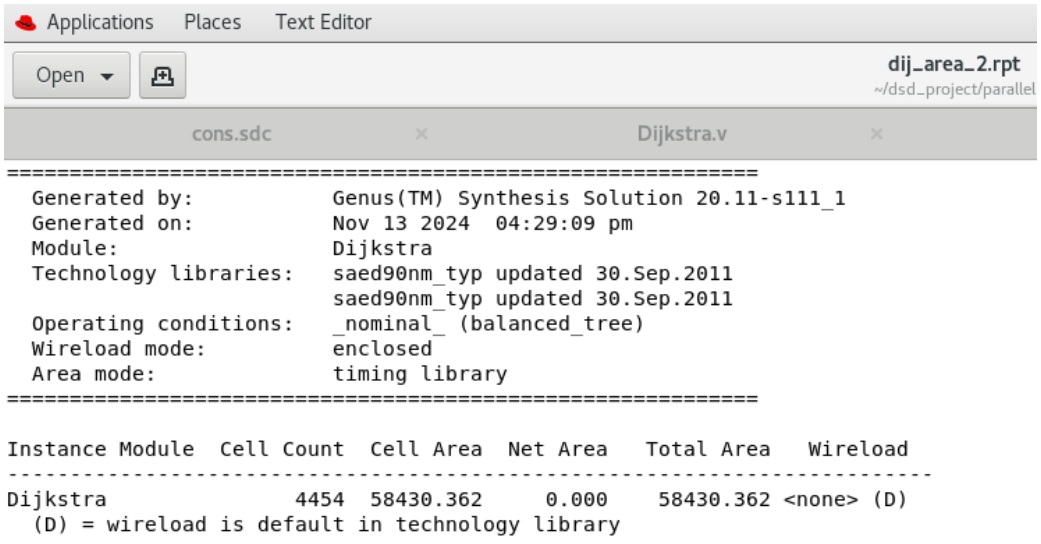


UNPARALLELISED CODE :



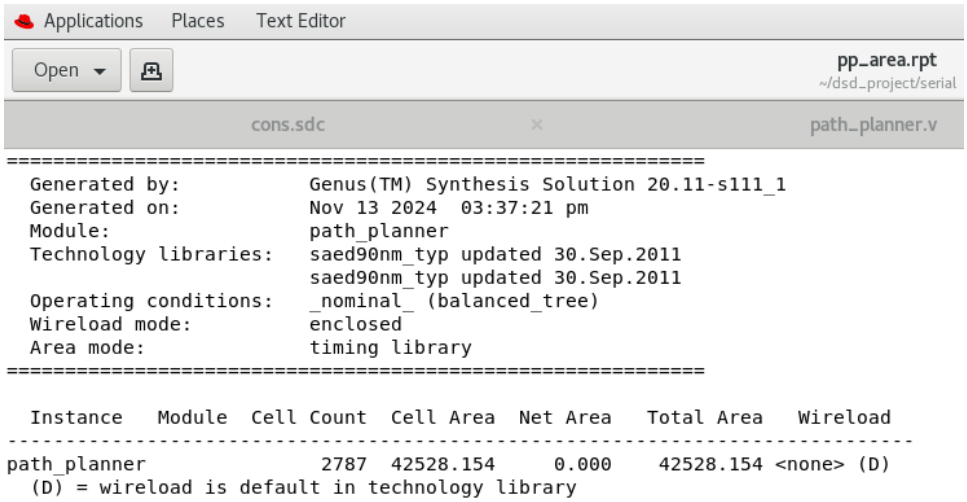
AREA REPORT

PARALLELISED :




```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 13 2024  04:29:09 pm
  Module:                 Dijkstra
  Technology libraries:   saed90nm_typ updated 30.Sep.2011
                          saed90nm_typ updated 30.Sep.2011
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
------------------------------------------------------------------------------
Dijkstra              4454  58430.362     0.000    58430.362 <none> (D)
  (D) = wireload is default in technology library
```

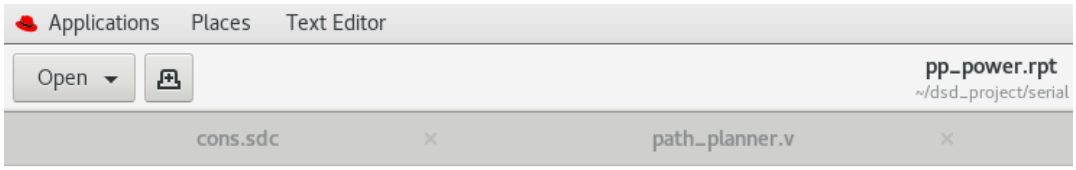
UNPARALLELISED :




```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 13 2024  03:37:21 pm
  Module:                 path_planner
  Technology libraries:   saed90nm_typ updated 30.Sep.2011
                          saed90nm_typ updated 30.Sep.2011
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

  Instance    Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
path_planner               2787  42528.154     0.000    42528.154 <none> (D)
  (D) = wireload is default in technology library
```

POWER REPORT

PARALLELISED :




```
Instance: /path_planner
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage      Internal    Switching         Total    Row%
  ---------------------------------------------------------------------------
       memory     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
     register     1.15040e-04  -1.65591e-04  3.78570e-05  -1.26939e-05  -2.17%
        latch     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
        logic     9.44128e-05   3.20446e-04  1.12732e-04   5.27590e-04  90.04%
         bbox     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
        clock     0.00000e+00   0.00000e+00  7.10496e-05   7.10496e-05  12.13%
          pad     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
           pm     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
  ---------------------------------------------------------------------------
    Subtotal     2.09453e-04   1.54855e-04  2.21638e-04   5.85946e-04 100.00%
  Percentage          35.75%        26.43%       37.83%       100.00% 100.00%
  ---------------------------------------------------------------------------
```

UNPARALLELISED:

Applications Places Text Editor

Open dij_power_2.rpt ~/dsd_project/parallel

cons.sdc × Dijkstra.v × Dijkstra_tb.v ×

```
Instance: /Dijkstra
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage      Internal    Switching         Total    Row%
  ------------------------------------------------------------------------------
       memory     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
     register     1.16493e-04  -2.27274e-04  5.28489e-05  -5.79319e-05  -6.76%
        latch     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
        logic     1.46711e-04   5.04160e-04  1.93350e-04   8.44221e-04  98.49%
         bbox     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
        clock     0.00000e+00   0.00000e+00  7.09056e-05   7.09056e-05   8.27%
          pad     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
           pm     0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     2.63204e-04   2.76886e-04  3.17105e-04   8.57195e-04 100.00%
  Percentage           30.71%        32.30%       36.99%        100.00% 100.00%
  ------------------------------------------------------------------------------
```

TIMING REPORT

PARALLELISED :

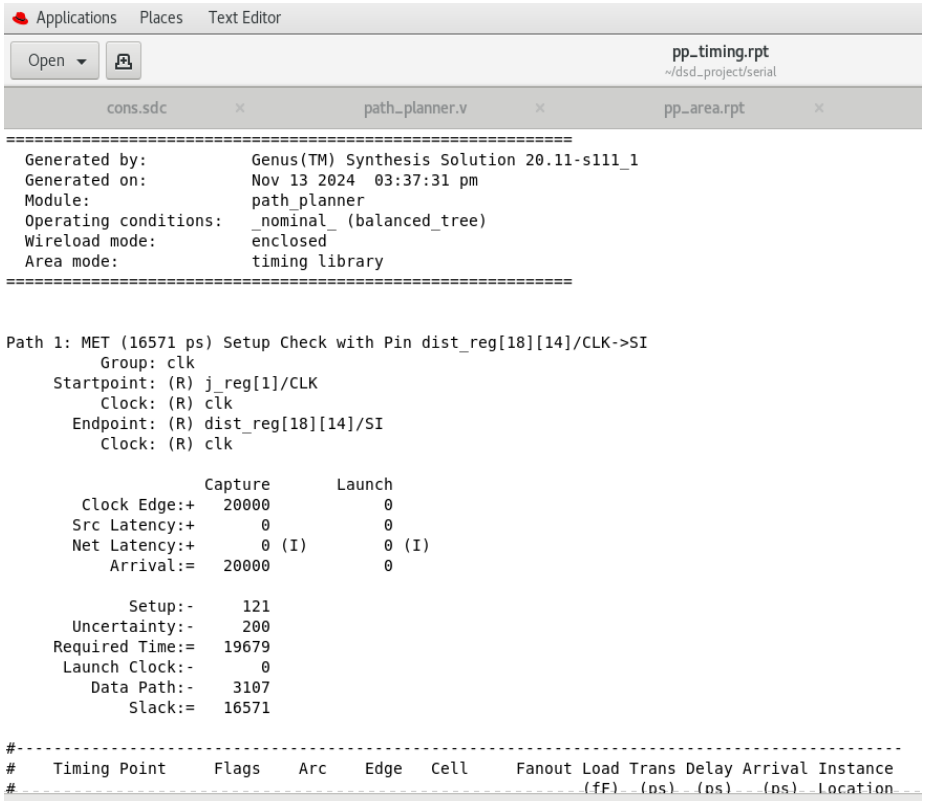
Applications Places Text Editor

Open dij_timing_2.rpt ~/dsd_project/parallel

cons.sdc × Dijkstra.v × Dijkstra_tb.v × dij_area_2.rpt ×

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 13 2024  04:29:19 pm
  Module:                 Dijkstra
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (16411 ps) Setup Check with Pin dist_reg[16][1]/CLK->D
          Group: clk
     Startpoint: (R) j_reg[3]/CLK
          Clock: (R) clk
       Endpoint: (R) dist_reg[16][1]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   20000            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=  20000            0

             Setup:-    107
       Uncertainty:-    200
     Required Time:=  19693
      Launch Clock:-      0
         Data Path:-   3282
             Slack:=  16411

#-------------------------------------------------------------------------------------------
#   Timing Point    Flags    Arc    Edge   Cell     Fanout  Load Trans Delay Arrival Instance
#                                                    (fF)  (ps)  (ps)   (ps)  Location
```

UNPARALLELISED :




```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 13 2024  03:37:31 pm
  Module:                 path_planner
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (16571 ps) Setup Check with Pin dist_reg[18][14]/CLK->SI
          Group: clk
     Startpoint: (R) j_reg[1]/CLK
          Clock: (R) clk
       Endpoint: (R) dist_reg[18][14]/SI
          Clock: (R) clk

                    Capture       Launch
        Clock Edge:+   20000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   20000            0

             Setup:-     121
       Uncertainty:-     200
     Required Time:=   19679
      Launch Clock:-       0
         Data Path:-    3107
             Slack:=   16571

#-------------------------------------------------------------------------------------------------
#    Timing Point     Flags    Arc    Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                       (fF)  (ps)  (ps)   (ps)  Location
```