

# Hackathon KAUST GPU 2020

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KAUST & Saudi Aramco

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  - Overview
  - Compilation and validation
- 2 **Test platforms**
  - Shaheen II (KAUST)
- 3 **Test Case Grid**
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- 5 **Conclusions and next steps**
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hpcscan is a C++ code for benchmarking HPC kernels (mainly for solving PDEs with FDM)

- Simple code structure based on individual test cases
- Easy to add new test cases
- Main class is Grid: multi-dimension (1, 2 & 3D) Cartesian grid
- Hybrid MPI/OpenMP parallelism
- All configuration parameters on command line
- Support single and double precision computation
- Compilation with standard Makefile
- No external libraries
- Follows C++ Google style code

## hpcscan embeds several test cases

### Current version 1.0

- General operations on grids
- Memory operations
- MPI communication
- FD computation
- Basic wave propagator

### Possible additions for future versions

- Operations on matrices full and sparse
- FFT
- IO
- Compression

# Compilation and validation

Compiling hpcscan

go to `./build` and `make` (by default compilation with single precision float)

To compile with double precision float, make `precision=double`

Validating hpcscan

go to `./script` and `sh runValidationTests.sh`

Table: `runValidationTests.sh`<sup>1</sup>

Machine	Compiler	Single prec.	Double prec.
Mars	g++ 9.3.0	764 PASS / 0 FAIL / 0 ERR / 20 WARN	764 PASS / 0 FAIL / 0 ERR / 20 WARN
Shaheen	icpc 19.0.5.281	764 PASS / 0 FAIL / 0 ERR / 20 WARN	764 PASS / 0 FAIL / 0 ERR / 20 WARN

Numbers can differ due to availability of features depending on the platforms

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<sup>1</sup>Updated Nov 25, 2020

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# Test platform - Shaheen II (KAUST)

## Machine Shaheen II / Cray XC40

- Computing nodes Intel Haswell 2.3 Ghz dual socket (16 cores / socket)
- RAM 128 GB with Peak memory BW 136.5 GB/s
- Peak performance Single Prec. 2.36 TFLOP/s / Double Prec. 1.18 TFLOP/s
- Interconnect Cray Aries with Dragonfly topology
  - 60 GB/s optical links between groups
  - 8.5 GB/s copper links between chassis
  - 3.5 GB/s backplane within a chassis
  - 5 GB/s PCIe from node to Aries router





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# Test Case Grid - Description

- Fill grid ( $W = \text{coef}$ )
- L1 error between grid W and R
- Get min. grid W
- Get max. grid W
- Update pressure  $W = 2*U - W + C*L$  (used in propagator)
- Medium Grid size 4 GB (1000 × 1000 × 1000 points)

# Test Case Grid - Results

- CPU (Intel, no way to get AMD) and GPU kernels (V100)

Table: Bandwidth GB/s <sup>2</sup>

Machine	Algo.	Fill	L1 err.	Get max.	Get min.	Update Pres.
Shaheen CPU	Baseline	54	124	126	126	120
Ibex CPU	Baseline	92	217	224	224	198
Ibex GPU1	Cuda	497	274	700/221	700/221	673
Ibex GPU2	OpenAcc	270	-	-	-	-
Ibex GPU3	OpenMP	-	-	-	-	-

Table: Bandwidth GPoints/s

Machine	Algo.	Fill	L1 err.	Get max.	Get min.	Update Pres.
Shaheen CPU	Baseline	13.5	15.5	31.5	31.5	6.0
Ibex CPU	Baseline	23.0	27.1	56.0	56.0	9.9
Ibex GPU1	Cuda	124	34.5	175/55	175/55	33.7
Ibex GPU2	OpenAcc	67	-	-	-	-
Ibex GPU3	OpenMP	-	-	-	-	-

Reproduce results with `./hackathonTestCases/testCase_Grid/`

<sup>2</sup> Updated Dec 1, 2020

## Machine: Shaheen

- L1 Err., Get Min & Max: 125 GB/s close to peak BW (92 % Peak Mem. BW)
- Low perf for Fill: 54-58 GB/s (40-43 % Peak Mem. BW)
- Max Err. 72-91 GB/s (53-67 % Peak Mem. BW)
- Pressure update 6 GPoint/s (120 GB/s, 88 % Peak Mem. BW)

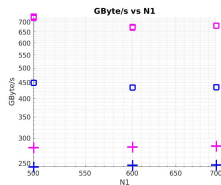
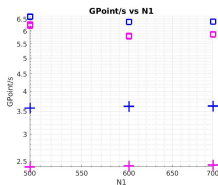
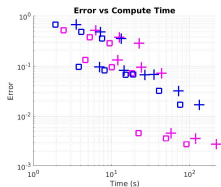
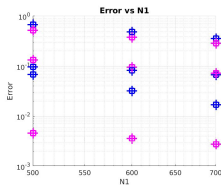
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# Test Case Propa - Description

- Seismic wave propagator
- 2nd order acoustic wave equation
- Time-domain Finite-difference
- Various FD order in space
- 2nd FD order in time
- Various grid size and time steps
- Total 18 configurations
- Comparison against analytical solution (Eigen mode)

# Test Case Propa - Results

- **Machine: shaheen**
- 1 node / 32 threads
- CPU Baseline & cache blocking kernels <sup>3</sup>
- FD: Black O2, Blue O4, Pink O8, Red O12 / Square=CPU CacheBlk, Cross=Baseline

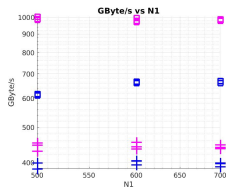
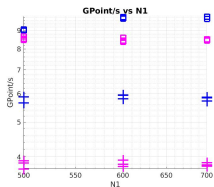
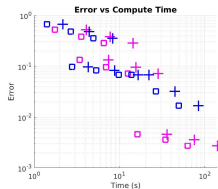
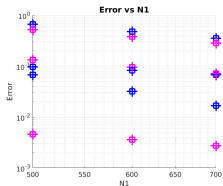


Reproduce results with `./hackathonTestCases/testCase_Propa/runShaheen.sh`

<sup>3</sup> Updated Nov 28, 2020

# Test Case Propa - Results

- **Machine: Ibex Cpu**
- 1 node / 32 threads
- CPU Baseline & cache blocking kernels <sup>4</sup>
- FD: Black O2, Blue O4, Pink O8, Red O12 / Square=CPU CacheBlk, Cross=Baseline



Reproduce results with `./hackathonTestCases/testCase_Propa/runIbexCpu.sh`

<sup>4</sup> Updated Dec 1, 2020

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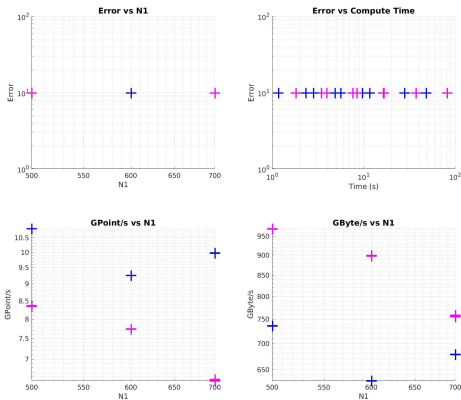
Dec 2020

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# Test Case Propa - Results

- Machine: Ibex Gpu 1 GPU V100
- CUDA kernel <sup>5</sup>
- FD: Black O2, Blue O4, Pink O8, Red O12 / Cross=CUDA
- Results not validated (Error NaN)

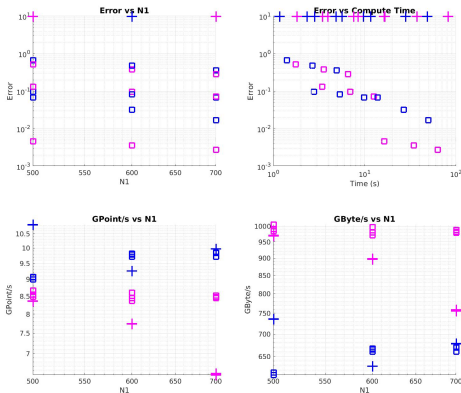


Reproduce results with `./hackathonTestCases/testCase_Propa/runIbexGpuCuda.sh`

<sup>5</sup> Updated Dec 2, 2020

# Test Case Propa - Results

- Machine: Ibex Gpu 1 GPU V100 and CPU Skylake 32 cores
- CUDA kernel <sup>6</sup>
- FD: Black O2, Blue O4, Pink O8, Red O12 / Cross=CUDA
- Results not validated (Error NaN)



Reproduce results with `./hackathonTestCases/testCase_Propa/runIbexCpuGpuCuda.sh`

<sup>6</sup> Updated Dec 2, 2020

Table: Best total time for 18 configurations <sup>7</sup>

Machine	Algo.	Time (s)	Speedup
Shaheen CPU	Baseline	826	0.5
Shaheen CPU	CacheBlk	388	1.0
Ibex CPU	Baseline	524	0.7
Ibex CPU	CacheBlk	265	1.5
Ibex GPU1	Cuda	291	1.3
Ibex GPU2	OpenACC	XXX	Y.Y
Ibex GPU3	OpenMP	XXX	Y.Y

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<sup>7</sup>Updated Dec 1, 2020

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# Conclusions and next steps

TO DO

# Content

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# Acknowledgements

- KAUST ECRC and KSL for access and support on Shaheen II & Ibex