Report Generated From Altium Designer

Name	Priority	Enabled	Type	Category	Scope	Attributes
ANT_clearence_polygon	1	True	Clearance	Electrical	InNet('nRF_GPS_LNA') or InNet('LTE_ANT') or InNet('NetIC901_11') orInNet('GPS_ANTENNA_nRF') orInNet('GPS_ANTENNA_EXT') - All	Generic clearance = 0.125mm, and 6 value(s) for objects
AssemblyTestpoint	1	True	Assembly Testpoint Style	Testpoint	All	Under Comp - Allow Sides - Top, Bottom Pref Size = 1.524mm Pref Hole Size = 0.813mm Using Grid = Yes Grid = 0.025mm Grid Tolerance = 0mm
AssemblyTestPointUsage	1	True	Assembly Testpoint Usage	Testpoint	All	Testpoint - One Required Multiple - Not Allowed
ComponentClearance	1	True	Component Clearance	Placement	All - All	Horizontal Clearance = 0.254mm Vertical Clearance = 0.254mm
DiffPairsRouting	1	True	Differential Pairs Routing	Routing	All	Pref Gap = 0.193mm Min Gap = 0.19mm Max Gap = 0.254mmPref Width = 0.165mm Min Width = 0.165mm Max Width = 0.165mm
FabricationTestpoint	1	True	Fabrication Testpoint Style	Testpoint	All	Under Comp - Allow Sides - Top, Bottom Pref Size = 1.524mm Pref Hole Size = 0.813mm Using Grid = Yes Grid = 0.025mm Grid Tolerance = 0mm
FabricationTestPointUsage	1	True	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required Multiple - Not Allowed
Fanout_BGA	1	True	Fanout Control	Routing	IsBGA	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
GND_STAR	1	False	Routing Topology	Routing	InNet('GND')	Topology - Starburst
Height	1	True	Height	Placement	All	Pref Height = 12.7mm Min Height = 0mm Max Height = 25.4mm
HoleSize	1	True	Hole Size	Manufacturing	All	Min = 0.2mm Max = 2.54mm
HoleToHoleClearance	1	True	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 0.279mm
LayerPairs	1	True	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
MinimumAnnularRing	1	True	Minimum Annular Ring	Manufacturing	All	Min = 0.15mm
MinimumSolderMaskSliver	1	True	Minimum Solder Mask Sliver	Manufacturing	All - All	Minimum Solder Mask Sliver = 0.254mm
NetAntennae	1	True	Net Antennae	Manufacturing	All	Net Antennae Tolerance = 0mm
netties rule	1	True	Short-Circuit	Electrical	HasFootprint('NETTIE_FP') - All	Short Circuit - Allowed
PasteMaskExpansion	1	True	Paste Mask Expansion	Mask	All	Expansion = 0mm
PlaneClearance	1	True	Power Plane Clearance	Plane	All	Clearance = 0.508mm
PlaneConnect	1	True	Power Plane Connect Style	Plane	All	Style - Relief Connect Expansion = 0.508mm Width = 0.254mm Gap = 0.254mm # Entries = 4
PolygonConnect_1	1	True	Polygon Connect Style	Plane	isVia and inNet('GND') or isVia and innet('VDD') orIn Component('IC1201') and InNet('GND') - All	Style - Direct Connect
RoutingCorners	1	True	Routing Corners	Routing	All	Style - 45 Degree Min Setback = 2.54mm Max Setback = 2.54mm
RoutingLayers	1	True	Routing Layers	Routing	All	TopLayer - Enabled MidLayer1 - DisabledMidLayer2 - Enabled BottomLayer - Enabled
RoutingPriority	1	True	Routing Priority	Routing	All	Priority = 0
RoutingVias	1	True	Routing Via Style	Routing	All	Pref Size = 0.5mm Pref Hole Size = 0.25mm
SilkToSilkClearance	1	True	Silk To Silk Clearance	Manufacturing	All - All	Silk to Silk Clearance = 0.254mm
SilkToSolderMaskClearance	1	True	Silk To Solder Mask Clearance	Manufacturing	IsPad - All	Silk To Solder Mask Clearance = 0.254mm
SMDNeckDown	1	True	SMD Neck-Down	SMT	All	Percent = 80%
SolderMaskExpansion_VIA	1	True	Solder Mask Expansion	Mask	IsVia	Expansion = 0.102mm
UnpouredPolygon	1	True	Modified Polygon	Electrical	All	Allow modified - No Allow shelved - No
UnRoutedNet	1	True	Un-Routed Net	Electrical	All	(No Attributes)
Width_PWR	1	True	Width	Routing	InNetClass('PWR')	Pref Width = 0.4mm Min Width = 0.15mm Max Width = 0.4mm

Name	Priority	Enabled	Type	Category	Scope	Attributes
Fanout_LCC	2	True	Fanout Control	Routing	IsLCC	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
PolygonConnect	2	True	Polygon Connect Style	Plane	All - All	Style - Relief Connect Width = 0.254mm Angle = 90 # Entries = 4 Air Gap = 0.254mm
RoutingTopology	2	True	Routing Topology	Routing	All	Topology - Shortest
ShortCircuit	2	True	Short-Circuit	Electrical	All - All	Short Circuit - Not Allowed
SolderMaskExpansion	2	True	Solder Mask Expansion	Mask	All	Expansion = 0.102mm
USB_polygon	2	True	Clearance	Electrical	InNamedPolygon('L1-GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('USB0'))	Clearance = 1.397mm
Width_diff	2	True	Width	Routing	(InDifferentialPairClass('All Differential Pairs'))	Pref Width = 0.165mm Min Width = 0.165mm Max Width = 0.165mm
Fanout_SOIC	3	True	Fanout Control	Routing	IsSOIC	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
USB_clearence	3	True	Clearance	Electrical	(InDifferentialPairClass('All Differential Pairs')) - All	Generic clearance = 0.152mm, and 9 value(s) for objects
Width_GPIO_1	3	True	Width	Routing	InNetClass('GPIO') or InNetClass('COEX') or InNetClass('SWD') or InNetClass('UART')	Pref Width = 0.15mm Min Width = 0.15mm Max Width = 0.152mm
Fanout_Small	4	True	Fanout Control	Routing	(CompPinCount < 5)	Style - Auto Direction - Out Then In Via Grid = 0.025mm
nRFfootprint	4	True	Clearance	Electrical	HasFootprint('XCVR_NRF9160-SICA-R7') - All	Clearance = 0.125mm
Width	4	True	Width	Routing	All	Pref Width = 0.15mm Min Width = 0.15mm Max Width = 0.254mm
Fanout_Default	5	True	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
Polygon_Clearence	5	True	Clearance	Electrical	(InNamedPolygon('L1-GND-Polygon')) or(InNamedPolygon('L4-GND-Polygon')) or(InNamedPolygon('L2-GND_polygon')) or(InNamedPolygon('L3-GND-Polygon')) - All	Generic clearance = 0.254mm, and 9 value(s) for objects
Top_layer_Clearance	6	True	Clearance	Electrical	All - OnLayer('Top Layer')	Clearance = 0.125mm
Clearance	7	True	Clearance	Electrical	All - All	Clearance = 0.125mm