Report Generated From Altium Designer

lame	Priority	Enabled	Туре	Category	Scope	Attributes
.NT_clearence_polygon	1	True	Clearance	Electrical	InNet('nRF_GPS_LN A') or InNet('LTE_ANT') or InNet('NetIC901_11') orInNet('GPS_ANTE NNA_nRF') orInNet(' GPS_ANTENNA_EX T') - All	Generic cleara
AssemblyTestpoint	1	True	Assembly Testpoint Style	Testpoint	All	Under Comp - = 0.813mm
ssemblyTestPointUsage	1	True	Assembly Testpoint Usage	Testpoint	All	Testpoint - On
ComponentClearance	1	True	Component Clearance	Placement	All - All	Horizontal Cle
DiffPairsRouting	1	True	Differential Pairs Routing	Routing	All	Pref Gap = 0.1 0.165mm Mi
abricationTestpoint	1	True	Fabrication Testpoint Style	Testpoint	All	Under Comp - = 0.813mm
fabricationTestPointUsage	1	True	Fabrication Testpoint Usage	Testpoint	All	Testpoint - On
anout BGA	1	True	Fanout Control	Routing	IsBGA	Style - Auto
SND STAR	1 1	False	Routing Topology	Routing	InNet('GND')	Topology - Sta
leight IoleSize	<u>1</u> 1	True True	Height Hole Size	Placement Manufacturing	All All	Pref Height = 1 Min = 0.2mm
loleSize loleToHoleClearance	1	True	Hole Size Hole To Hole Clearance	Manufacturing Manufacturing	All - All	Hole To Hole (
ayerPairs	1	True	Layer Pairs	Manufacturing	All	Layer Pairs - E
linimumAnnularRing linimumSolderMaskSliver	1	True True	Minimum Annular Ring Minimum Solder Mask Sliver	Manufacturing	All All - All	Min = 0.15mm Minimum Sold
letAntennae etties rule	<u>1</u>	True True	Net Antennae Short-Circuit	Manufacturing Electrical	All HasFootprint('NETTI E FP') - All	Net Antennae Short Circuit -
asteMaskExpansion	1	True	Paste Mask Expansion		All	Expansion = 0
laneClearance	1	True	Power Plane Clearance	Plane	All	Clearance = 0.
laneConnect	1	True	Power Plane Connect Style		All	Style - Relief 0 0.254mm # I
olygonConnect_1	1	True	Polygon Connect Style	riane	isVia and inNet('GND') or isVia and innet('VDD') orIn Component('IC1201') and InNet('GND') - All	Style - Direct (
loutingCorners	1	True	Routing Corners	Routing	All	Style - 45 Deg
outingLayers	1	True	Routing Layers	Routing	All	TopLayer - En Enabled
outingPriority	1 1	True	Routing Priority	Routing	All	Priority = 0
outingVias ilkToSilkClearance	1	True	Routing Via Style Silk To Silk Clearance	Routing Manufacturing	All - All	Pref Size = 0.5 Silk to Silk Cle
lkToSolderMaskClearance	1	True True	Silk To Silk Clearance Silk To Solder Mask Clearance	Manufacturing	IsPad - All	Silk To Solder
MDNeckDown	1	True	SMD Neck-Down	SMT	All	Percent = 80%
olderMaskExpansion VIA	1	True	Solder Mask Expansion		IsVia	Expansion = 0
npouredPolygon		True	Modified Polygon	Electrical	All	Allow modified
nRoutedNet	1	True	Un-Routed Net	Electrical	All	(No Attributes)
/idth_PWR anout_LCC	2	True True	Width Fanout Control	Routing Routing	InNetClass('PWR') IsLCC	Pref Width = 0 Style - Auto
olygonConnect	2	True	Polygon Connect Style		All - All	Style - Relief 0 0.254mm
outingTopology	2	True	Routing Topology	Routing	All	Topology - Sho
hortCircuit	2	True	Short-Circuit	Electrical	All - All	Short Circuit -
olderMaskExpansion		True	Solder Mask Expansion		All	Expansion = 0
ISB_polygon	2 2	True	Clearance	Electrical	InNamedPolygon('L1- GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U	
_ 70				Routing	GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential	
/idth_diff	2	True True	Clearance	Routing	GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential Pairs'))	:Pref Width = 0
/idth_diff anout SOIC	2	True	Clearance		GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential Pairs')) IsSOIC (InDifferentialPairClas s('All Differential	: Pref Width = 0 Style - Auto
/idth_diff anout SOIC SB_clearence	2 3	True True	Clearance Width Fanout Control	Routing	GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential Pairs')) IsSOIC (InDifferentialPairClas s('All Differential Pairs')) - All InNetClass('GPIO') or InNetClass('GPIO') or InNetClass('SWD') or	Style - Auto Generic cleara
Vidth_diff Sanout SOIC JSB_clearence Vidth_GPIO_1	2 2 3 3 3	True True True True	Width Fanout Control Clearance Width	Routing Routing Electrical Routing	GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential Pairs')) IsSOIC (InDifferentialPairClas s('All Differential Pairs')) - All InNetClass('GPIO') or InNetClass('GVEX') or InNetClass('SWD') or InNetClass('UART')	Style - Auto Generic cleara
Vidth_diff Fanout SOIC JSB_clearence Vidth_GPIO_1 Fanout Small JRFfootprint	2 3 3	True True True True	Width Fanout Control Clearance	Routing Routing Electrical	GND-Polygon') - (IsTrack or IsArc) and (InDifferentialPair('D') orInDifferentialPair('U SB0')) (InDifferentialPairClas s('All Differential Pairs')) IsSOIC (InDifferentialPairClas s('All Differential Pairs')) - All InNetClass('GPIO') or InNetClass('GPIO') or InNetClass('SWD') or	Style - Auto Generic cleara Pref Width = 0

Name	Priority	Enabled	Туре	Category	Scope	Attributes
har to		T	VAC -141-	Destina	- All	D() A/() - H
Width	4	True	Width	Routing	All	Pref Width = 0.15mm
Fanout Default	5	True	Fanout Control	Routing	All	Style - Auto Direction
Polygon_Clearence	5	True	Clearance	Electrical	(InNamedPolygo -GND-Polygon')) NamedPolygon() ND-Polygon')) oi amedPolygon(')) or(medPolygon('L3 -Polygon')) -	'L4-G r(InN 2-GN InNa -GND
Top_layer_Clearance	6	True	Clearance	Electrical	All - OnLaye Layer')	r('Top Clearance = 0 125mm
Clearance	7	True	Clearance	Electrical	All - All	Clearance = 0 125mm