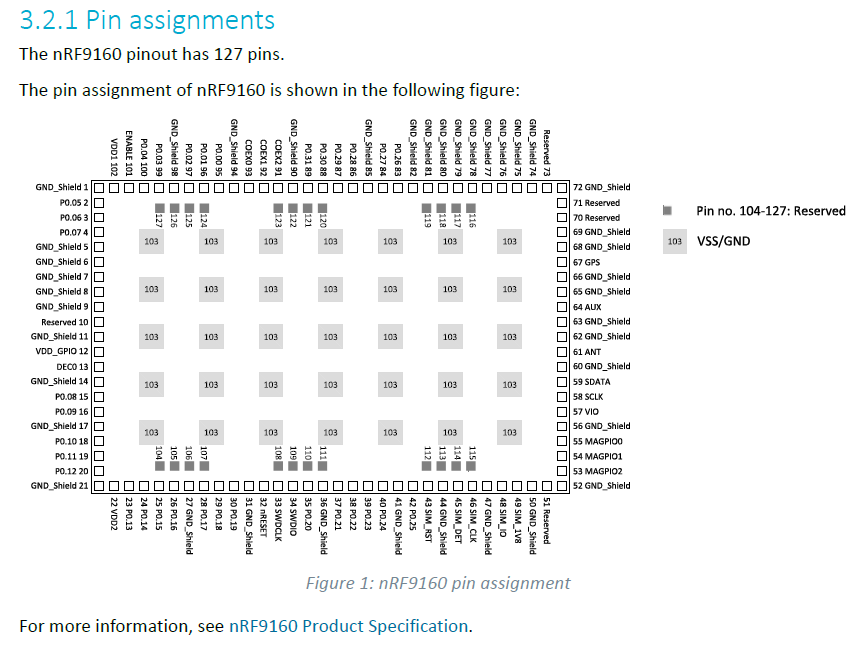
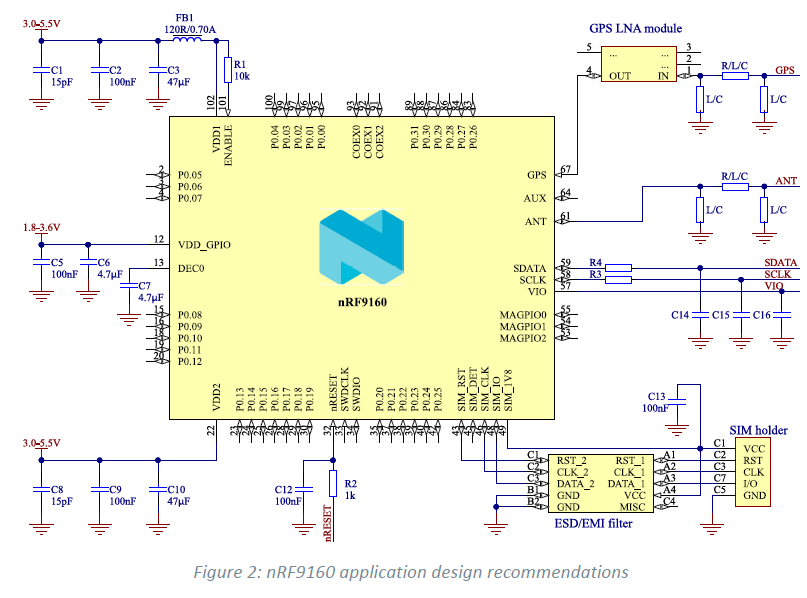
Voltage range : 3-5V. The mode, transceiver requires a minimum of 3.3V  




# Hardware Integration

## VSS

VSS (pin 103). Recommended that the PCBs ground planes around nRF9160 are as intact and as solid as possible. Use as many ground vias as possible between the top metal

layer of the application board and the inner ground layers connected to nRF9160's **VSS** pins. Typically,

metal filled vias provide the best thermal conductivity.

## GND\_shield

The following ground pins are dedicated for the embedded micro shield: 1, 5–9, 11, 14, 17, 21, 27, 31, 36,

41, 44, 47, 50, 52, 56, 60, 62, 63, 65, 66, 68, 69, 72, 74–82, 85, 90, 94, and 98.

Connect **GND\_Shield** electrically strongly to **VSS** (pin 103) and on the application board to the same

ground planes as **VSS**.

## ENABLE

**ENABLE** (pin 101) is a high-impedance control pin for the nRF9160-internal PMU.

It is used to enable and disable nRF9160. Logic high (> 0.8 x VDD1) enables nRF9160. The start delay is in

the range of a few milliseconds from pulling the **ENABLE** pin high. Logic low (< 0.4 V) disables nRF9160

and brings it into extremely low current consumption.

In products where nRF9160 is always enabled, the **ENABLE** pin can be connected to **VDD1** (pin 102) on

the application board with a series resistor. The series resistor minimizes digital noise coupling between

the **VDD1** and **ENABLE** pins. It is recommended to add a decoupling capacitor to the **ENABLE** pin. If

**ENABLE** is connected to **VDD1**, a shared capacitor can be used for the **ENABLE** and **VDD1** pins if the

**VDD1** decoupling capacitor is located close to the **VDD1** and **ENABLE** pins.

# VDD1 and VDD2

To minimize supply voltage ripple and suppress EMI coupling to/

from nRF9160, it is recommended to place low ESR capacitors close to the **VDD1** and **VDD2** pins. Supply

capacitors of low ESR (<0.1 Ω) are recommended.

To improve power delivery, voltage ripple, and EMI performance, it is recommended to have at least

one low ESR supply capacitor **C3** in **VDD1** and **C10** in **VDD2**. Placing ferrite bead FB1 at VDD1 is highly

recommended.

For **VDD\_GPIO**, the minimum recommendation is low ESR supply capacitor **C6**. Filtering for high frequency components can be improved by adding **C5** in the range of 1 nF to 470 nF.

To improve the supply network's EMI performance, a series three terminal filter capacitor can be added

close to the battery. For example, Murata NFM15PC can be used. The filter capacitor attenuates unwanted noise generated at wide frequency range approximately from 10 MHz to 3 GHz.

VDD1 and VDD2 must be connected to the same supplyvoltage