Digital Camera Design

TFE4152: Design of Integrated Circuits
Semester Project

Group 14
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November 18, 2019

Abstract

We live in an analog world. In order to capture a digital snapshot of this world we first have to start in the analog realm. We do this by obtaining an analog representation of the amount of light that hits the camera lens. This analog representation is then amplified and converted into a digital signal so that it can later be processed and viewed.

This report pertains to the design of a four pixel digital camera. The camera is divided into two main parts: analog and digital. Combining these parts allows us to obtain a binary representation of the photons interacting with the photo sensor. It also allows us to control the photo capture.

Contents

1 Introduction

Goal of the project is to design a control and readout circuit for a 2x2 camera sensor according to the specifications in the project description. This task can be splitted into a analog part ("Pixel_electronics") and a digital control block ("RE_Control", Figure 1). In the analog part the basic circuit is already given and only the device parameters are variable and have to be designed according the the requirements. First, those are calculated by hand according to the curriculum of the lecture. To design the "RE_control" first a final state machine is designed and then implemented in verilog. Both parts are then verified by simulating the analog part in AIM-Spice and the digital one using Xilinx Vivado to ensure that the requirements are met.

2 Design

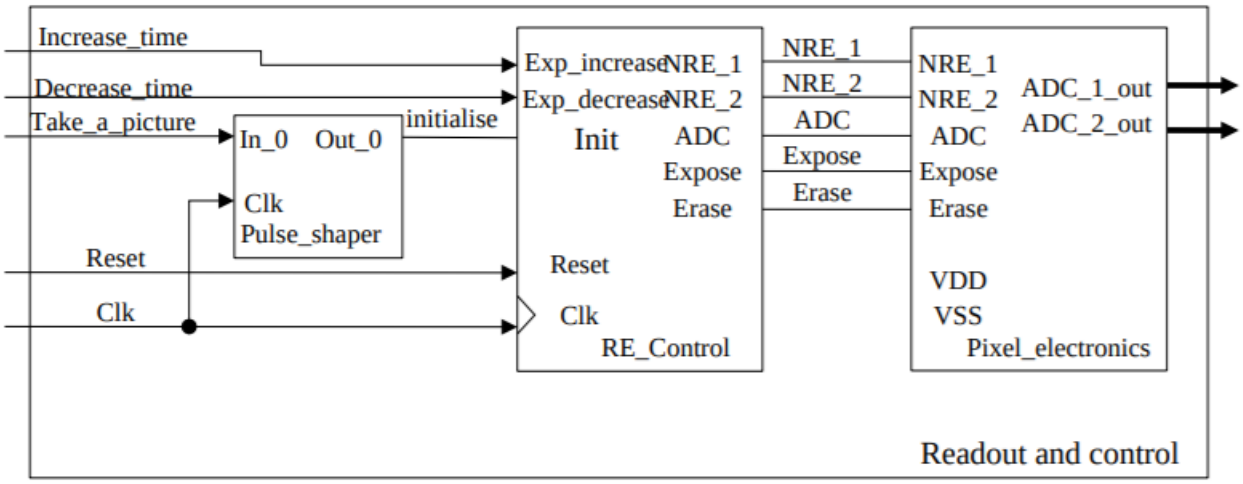


Figure 1: Block diagram for the readout and control circuit.

The readout and control circuit is shown in Figure 1. The inputs of the whole circuit are signals for increasing and decreasing the exposure time, a init-signal that indicates that a picture shall be taken and a reset and clock signal. Outputs are two output signals that connect to the ADCs.

The digital part "RE_Control" takes those inputs, processes them and outputs 5 signals that control the analog part ("Pixel_electronics") of the readout and control circuit. According to the signals of the digital part the analog circuit controls the physical connections and current flows so that all pixels of the camera sensor and their information is outputted at as specified in the project description.

Topic of this chapter is the implementation of those requirements in the analog and digital part of the readout and control circuit.

2.1 Analog

The parts of analog circuit that need to be designed (Figure 2) can be separated in different groups. The diode and current source together form a photo diode that acts as a sensor and "translates" the light intensity into a current. The parameters are already set and given which is why it is not discussed further. The two NMOS transistors M1 and M2 and the PMOS M4 all are controlled by the digital circuit and act as a

switch. The capacitor CS stores the charge that the photo diode outputs during the exposure time. And last the amplifier stage formed by the PMOS transistors M3 and M5 where as M5 acts an active load. The parameters for the capacitor CC1/2 are already specified in the assignment description with $C_{CC1/2} = 3pF$. The different groups are discussed in detail in the following sections.

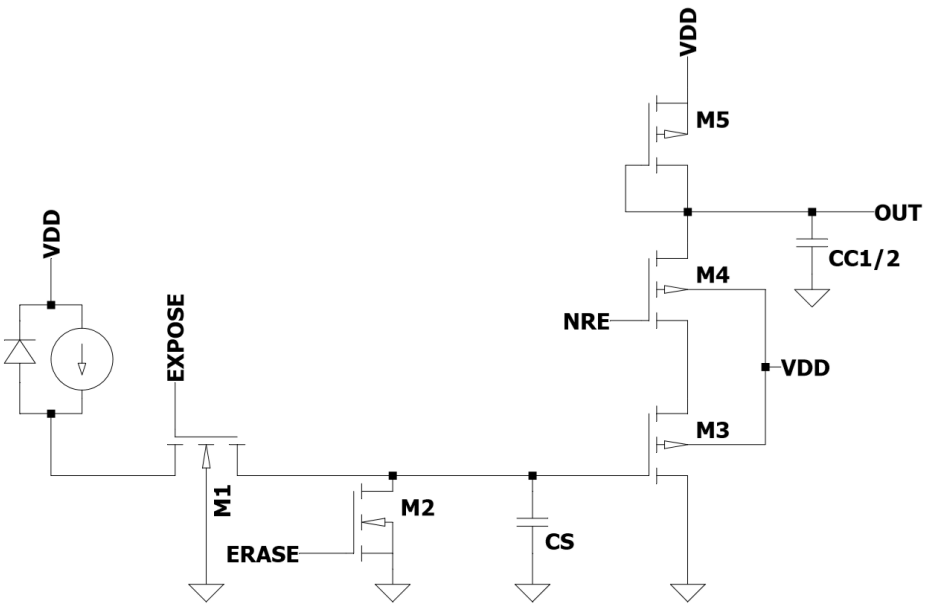


Figure 2: Schematics of analog circuit

2.1.1 Capacitor

The photo current during the exposure time $(2 - 30ms)$ during which the capacitor is charged varies from 50 to 750 pA. The exposure time is adjusted according to the lighting conditions so that the capacitor CS has to store charge of about $Q = 50pA \cdot 30ms = 750pA \cdot 2ms = 1.5pC$.

This is only the case if the camera is set up properly and the four pixels are exposed to similar light conditions. This is why the the capacitor should be sized so the circuit can still work if the charge is only half or double of the previously assumed one.

The transistor M3 has to be in the active region. This means that the source gate voltage V_{SG} has to be at least $|V_{tp}|$. This means that the potential of the gate node must not exceed $V_{DD} - |V_{tp}| = 1.8V - 0.45V = 1.35V$, assuming ideal conditions (V_{DS} of transistors is 0) where the source node could reach the potential of V_{DD}. Adding a safety margin of $0.15V$ the gate voltage of the transistor M3 should not exceed $1.2V$.

With those assumptions we can size the capacitor:

$$Q_{max} = 2 \cdot 1.5pC = 3pC;\ V_{max} = 1.2V$$

$$\Rightarrow \frac{Q_{max}}{V_{max}} = 2.5pF$$

Assuming the default case the voltage is $V_{CS}(Q = 1.5pC) = 0.6V$. This voltage is also assumed when the other components are sized and their parameters calculated.

2.1.2 Control transistors

The transistors M1, M2 and M4 in Figure 2 are controlling the different functions of the analog circuit and are therefore grouped together and named control transistors. They all share the similar design goal which is not to influence the rest of the circuit which means that they should ideally behave like an analog on-off switch.

The transistor M1 conducts current during the exposure phase. The highest current that is outputted from the photo diode is $750pA$. This current has to flow over the transistor and into the capacitor which is why the drain current I_D of the transistor M1 has to be at least as high even at the end of the exposure phase when the capacitor reaches its $V_{max,CS}$ of $1.2V$. At that point the transistor M1 is in active region because $V_{ds} = 0.6V > V_{gs} - V_{tn} = 1.8V - 1.2V - 0.45V = 0.15V$. Another important point is that the (nonlinear) capacitance of the transistor should not influence the rest of the circuit. This means that it should be several orders of magnitudes lower than the one of the capacitor. Because the capacitance of a transistor is proportional to its area, minimal length and with are assumed and then checked if it can conduct the photo current.

$$I_{D,M1}(L = 0.36\mu m, W = 1.08\mu m, V_S = 1.2V) = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}V_{eff}^2[(1 + \frac{\lambda L}{L}(V_{DS} - V_{eff})]$$

$$= \frac{1}{2}\cdot 70\mu AV^{-2}\cdot\frac{1.08\mu m}{0.36\mu m}\cdot(0.6V - 0.45V)^2[1 + \frac{0.08\mu mV^{-1}}{0.36\mu m}(0.6V - 0.6V + 0.45V)] = 2.6\mu A > 750pA$$

The most dominant capacitance of a transistor is the one between the gate and source node, the other ones are neglected for that reason.

$$C_{GS} = \frac{2}{3}WLC_{OX} + WL_{OV}C_{OX} = \frac{2}{3}\cdot 1.08\mu m\cdot 0.36\mu m\cdot 8.5fF/\mu m^2 + 1.08\mu m\cdot 0.35fF/\mu m = 2.58fF$$

$$2.58fF \ll 2.5pf = C_{CS}$$

The capacitance of the transistor M1 is small enough that it can be neglected and should not influence the voltage across the capacitor in a way that is noticeable by the ADC.

The purpose of transistor M2 is to discharge the capacitor during the idle phase so the next picture can be taken. The capacitance is not an issue here since both nodes of the most dominant one (C_{GS}) have no connection to the positive node of the capacitor. The only requirement for that transistor is that it discharges the capacitor before the next photo is taken. To verify that at least the order of magnitude of $\tau = r_{ds}C_{CS}$ is needed. A necessary step for that is to calculate r_{ds}. Because only the order of magnitude is needed V_{CS} is assumed to be $0.6V$ and r_{ds} to be constant throughout the discharge to simplify the calculation. The transistor M2 is in triode region the entire time, because $V_{DS} \leq V_{max,CS} = 1.2V < V_{eff} = 1.8V - 0.45V = 1.35V$.

$$I_{D,M2}(V_{ds} = 0.6V) = \mu_n C_{OX}\frac{W}{L}[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2} =$$

$$= 70\mu AV^{-2}\frac{1.08\mu m}{0.36\mu m}[(1.8V - 0.45V)0.6V - \frac{(0.6V)^2}{2}] = 13mA$$

$$\Rightarrow r_{ds,M2} = \frac{L}{\lambda L I_{D,M2}} = \frac{0.36\mu m}{0.08\mu m/V\cdot 13mA} = 34k\Omega$$

$$\Rightarrow \tau = r_{ds,M2}\cdot C_{CS} = 34k\Omega\cdot 2.5pF = 85ns \ll T_{CLK} = 1ms$$

This result shows that τ is much smaller compared to the cycle time of the clock. The difference is about 4

orders of magnitude so even with the above made assumptions the capacitor should hold only a charge very close to zero that does not affect the function of the circuit.

Transistor M4 should connect the OUT-signal to the ADC but should not affect the amplifier. This means that its r_{ds} must be small compared to transistor M3 so it can be neglected when designing the common source amplifier in the next section. This can be achieved by increasing the width to the maximum of $5.04\mu m$ and make the length as small as possible ($0.36\mu m$).

As we will see in the simulations in 3.1.1 this assumption does not change the behavior of the amplifier.

2.1.3 Common source amplifier

The two PMOS transistors M3 and M5 together form a common source amplifier where M5 acts as an active load. As noted above, transistor M4 is neglected.

(a) schematics (b) small signal model

Figure 3: common source amplifier

In Figure 3 the schematics with the two transistors M3 and M5 (a) and small signal model of the common source amplifier is shown. To calculate the parameters of the two transistors, the amplifier is considered to be isolated like in Figure 3 without any influence from the other components of the analog circuit.

To calculate the with and length of the two transistors and their relation we start with an equation where we state that the drain current of both transistors is equal. This is obvious when we look at Figure 3(a). Both transistors are in active region, because the gate of M5 is connected with its source and M3 because the capacitor CS was sized so that this is the case.

$$I_{D,M5} = I_{D,M3}$$

$$\frac{1}{2}\mu_n C_{OX}(\frac{W}{L})_{M5}V_{eff,M5}^2[1+\lambda(V_{SD,M5}-V_{eff,M5})] = \frac{1}{2}\mu_n C_{OX}(\frac{W}{L})_{M3}V_{eff,M3}^2[1+\lambda(V_{SD,M3}-V_{eff,M3})]$$

Some voltages can be expressed differently: $V_{SG,M5} = V_{SD,M5}$, $V_{SD,M3} = OUT$ and $V_{SG,M3} = OUT - V_{in}$

$$\Rightarrow \frac{W_{M5}}{L_{M5}}(V_{SD,M5}-|V_{tp}|)^2[1+\frac{\lambda L}{L_{M5}}(|V_{tp}|)] = \frac{W_{M3}}{L_{M3}}(V_{SG,M3}-|V_{tp}|)^2[1+\frac{\lambda L}{L_{M3}}(V_{in}+|V_{tp}|)]$$

In the next step we want $[1 + \frac{\lambda L}{L_{M5}}(|V_{tp}|)]$ and $[1 + \frac{\lambda L}{L_{M5}}(V_{in} + |V_{tp}|)]$ to be equal

$$\Rightarrow \frac{\lambda L}{L_{M5}}(|V_{tp}|) = \frac{\lambda L}{L_{M3}}(V_{in} + |V_{tp}|)$$

$$\Rightarrow L_{M3} = L_{M5}\frac{V_{in} + |V_{tp}|}{|V_{tp}|} = \frac{7}{3}L_{M5}$$

Now that the terms in the squared brackets are equal we can simplify the equation.

$$\frac{W_{M5}}{L_{M5}}(V_{SD,M5} - |V_{tp}|)^2 = \frac{W_{M3}}{L_{M3}}(V_{SG,M3} - |V_{tp}|)^2$$

Using the above mentioned different expressions for $V_{SD,M5}$ and $V_{SG,M3}$ we get:

$$\frac{W_{M5}}{L_{M5}}(VDD - V_{in} - V_{off} - |V_{tp}|)^2 = \frac{W_{M3}}{L_{M3}}(V_{off} - |V_{tp}|)^2$$

Where as $V_{off} = OUT - V_{in}$. This offset voltage between the input and output voltage has to be at least $|V_{tp}|$ because the transistor M3 must be in active region. This voltage cannot be greater than $0.6V$ either, because $V_{max,CS} = 1.2V$ and $V_{max,CS} = 1.2V + V_{off} \leq VDD = 1.8V$. This condition is important in a later step.

In the next step we use the relation $L_{M3} = \frac{7}{3}L_{M5}$:

$$\frac{W_{M5}}{L_{M5}}(VDD - V_{in} - V_{off} - |V_{tp}|)^2 = \frac{3W_{M3}}{7L_{M5}}(V_{off} - |V_{tp}|)^2$$

$$\Rightarrow W_{M5}(VDD - V_{in} - V_{off} - |V_{tp}|)^2 = \frac{3W_{M3}}{7}(V_{off} - |V_{tp}|)^2$$

Assuming $V_{in} = 0.6V$:

$$\Rightarrow W_{M3} = \frac{7}{3} \cdot \frac{(VDD - V_{in} - V_{off} - |V_{tp}|)^2}{(V_{off} - |V_{tp}|)^2} \cdot W_{M5}$$

The specifications limit the size of W and therefore also the maximum ratio of W_{M3} and W_{M5} to $\frac{W_{max}}{W_{min}} = \frac{5.04\mu m}{1.08\mu m} = \frac{14}{3}$

$$\Rightarrow \frac{(VDD - V_{in} - V_{off} - |V_{tp}|)^2}{(V_{off} - |V_{tp}|)^2} \leq \frac{14}{3}$$

This inequality is true for a $V_{off,min}$ of about $0.575V$. For lower V_{off} the ratio is to big and $V_{off,max} = 0.6V$. A higher V_{off} reduces the ratio which leaves more room for later adjustments which is why $V_{off} = 0.6V$ is chosen. The ratio is then as follows:

$$\Rightarrow W_{M3} = \frac{7}{3} \cdot \frac{(1.8V - 0.6V - 0.6V - 0.45V)^2}{(0.6V - 0.45V)^2} \cdot W_{M5} = \frac{7}{3} \cdot W_{M5}$$

The ratio between the gate lengths and the widths of the transistors are the same when $V_{off} = 0.6V$. During the readout phase the capacitor CC has to be discharged. To minimize the time it takes to to that the width of transistor should be maximized and its length minimized. That is why minimal length is chosen for transistor M5 ($L = 0.36\mu m$) and maximal width for transistor M3 ($W = 5.04\mu m$). The other dimensions are as follows:

$$L_{M3} = \frac{7}{3}L_{M5} = 0.84\mu m$$

$$W_{M5} = \frac{3}{7}W_{M5} = 2.16\mu m$$

With the dimensions we can now calculate the drain current through both transistors:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W_{M3}}{L_{M3}}V_{eff,M3}^2[1+\frac{\lambda L}{L_{M3}}(V_{SD,M3}-V_{eff,M3})]$$

$$= \frac{1}{2}\mu_n C_{OX}\frac{5.04\mu m}{0.84\mu m}(V_{off}-|V_{tp}|)^2[1+\frac{0.08\mu m}{0.84\mu m\cdot V}(V_{in}+V_{off}-V_{off}+|V_{tp}|)] = 5.2\mu A$$

With the current we can calculate the resistance $r_{ds,M3}$:

$$r_{ds,M3} = \frac{L}{\lambda L\, I_D} = \frac{0.84\mu m\cdot V}{0.08\mu m\cdot 5.2\mu A} = 2.0M\Omega$$

During the readout phase the capacitor CC1/2 has to be discharged. The maximum time for that is one clock cycle $T_{CLK} = 1ms$. Therefore τ should be at least one order of magnitude lower:

$$\tau_{CC,M3} = r_{ds,M3}\cdot C_{CC1/2} = 2.0M\Omega\cdot 3pF = 6\mu s \ll T_{CLK} = 1ms$$

Now that all parameters are calculated they are summarized for a better overview:

$$C_{CS} = 2.5pF$$

	M1	M2	M3	M4	M5
W [μm]	1.08	1.08	5.04	5.04	2.16
L [μm]	0.36	0.36	0.84	0.36	0.36

2.2 Digital

There are three phases in the process of taking a picture. Those being:

- Idle
- Exposure
- Readout

The idle phase is the default state of the camera system. In this phase an erase signal is held high in order to ensure that the capacitor CS is fully drained before a new picture is taken.

When an initializing pulse is sent into the digital controller the next phase of the picture taking process is initiated. The next phase being the expose phase. The expose phase exposes the camera for for an adjustable amount of time. The erase signal is set to zero when the expose signal is set high.

Once the Exposure phase is finished the process will move on to the readout phase. The readout phase reads out one row of pixels at a time. During the readout phase the NRE signals are lowered one at a time. The ADCs are activated while each of the NRE signals are low.

Once the readout process is finished the system will return to idle. The system will also return to idle whenever a reset signal is sent into the controller.

Since the picture taking process is divided into three distinct phases a finite state machine (FSM) is the most natural way to implement it. The state diagram for the controller is shown in Fig.4.

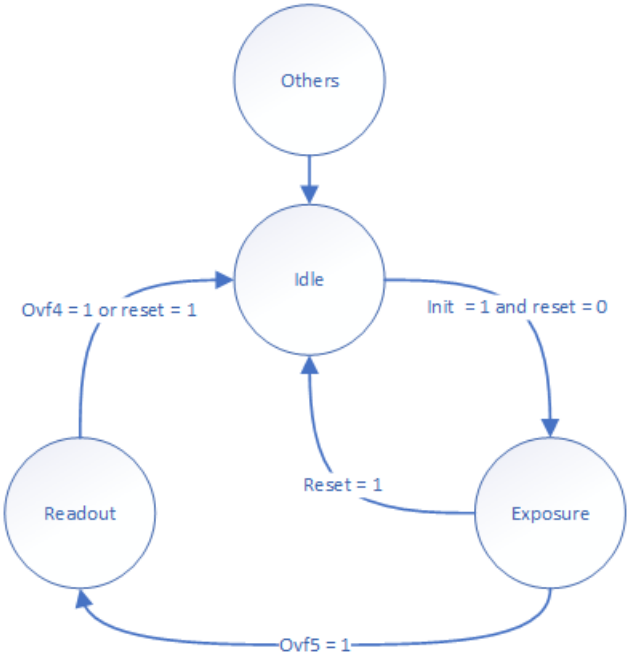


Figure 4: FSM state diagram

In order to move on to the readout state from the exposure state a counter is used to count up the exposure time. Once the counter reaches the exposure time an overflow flag (ovf5) is set to move on to the next state. A counter is also used to exit the readout phase, but this counter has a constant duration. The readout overflow flag is called ovf4.

The wave diagram for the picture taking process is shown in Fig.5. The controller is fully synchronous. New events only occur on the rising edge of the clock.

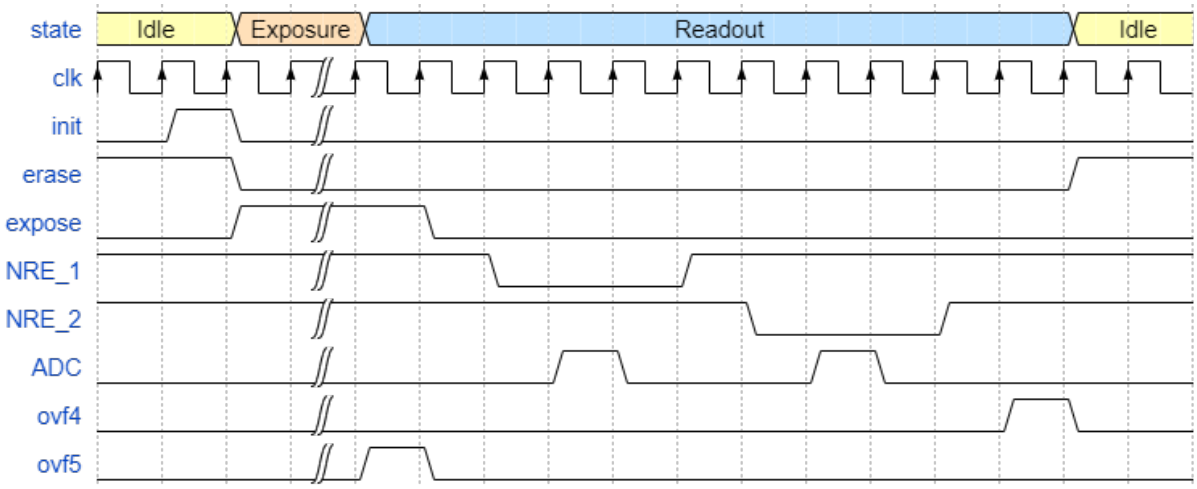


Figure 5: Wave diagram

The controller is designed using HDL (Verilog). The code Verilog code for the controller is shown in

Listing 4 in the appendix. At the beginning of the code the RE control module is defined along with all of its inputs and outputs. Below the outputs the FSM states are defined as parameters. After that all of the required registers are defined and initiated. The output registers are then assigned to the outputs.

In the first process controls the state. The state transitions are triggered by the conditions shown in state diagram (Fig.4). A case statement is used to easily describe the behavior in each state. If the state somehow is not one of the ones described, then the state will be set to idle.

The second process describes the counters, The counters counts up one tick every clock cycle. One tick corresponds to 1ms, because the clock frequency is 1kHz. This process also sets triggers the overflow flags. The counters and flags are reset when the state returns to idle.

The next process increments or decrements the exposure time register. Incrementing is prioritized over decrementing. If both increase and decrease are high concurrently, then the exposure time will increase.

The final process controls the output registers. The outputs are static during idle and exposure states. However, during the readout state the outputs have to follow a particular pattern. To achieve this pattern the register array "R" is used to store the values for "ADC", "NRE_1" and "NRE_1". The readout counter is used to select the correct array element to output. Each array element is a three bit vector.

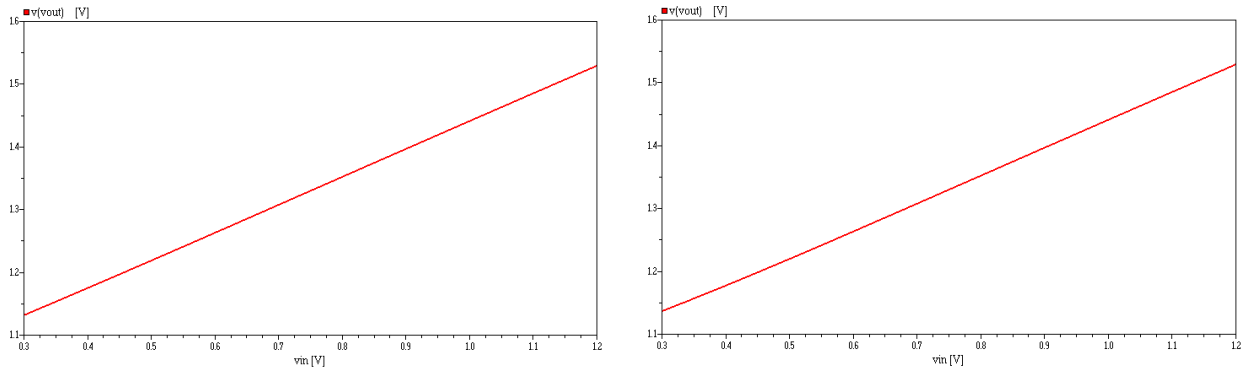
The design process of the code started by using the state diagram and waveform diagram to build most of the code. First defining the states along with the state transitions. Once the states were clearly defined everything else was designed using the the behavior of the individual signals in the waveform diagram. The simulator was then used to check the behavior of the controller. The information from the simulation was used as feedback in order to make minor tweaks to the code (adjusting counters etc.).

3 Simulations

3.1 Analog

3.1.1 Amplifier

Figure 6 shows a simulation of the amplifier with (b) and without (a) the amplifier M4 where the input voltage V_{in} is swept from $0.3V$ to $1.2V$ which equals the maximum voltage range of the capacitor CS as discussed in 2.1.1. This was done to check if the assumption that M4 does not have an impact on the output made in 2.1.2 is right or not and to see how the amplifier behaves.



(a) without transistor M4

(b) with transistor M4

Figure 6: Spice simulation of amplifier

Comparing the two plots shows that the assumption made was admissible. At $V_{in} = 0.3V$ the difference between the output voltages of the simulation with and without the transistor M4 is $4.9mV$ and decreases with increasing V_{in}. The difference is much smaller than the possible error that occurs when hand calculated values are compared to the simulation.

This simulation also shows that the output voltage ranges from about $1.13V$ to $1.53V$ for an input voltage $0.3V \leq V_{in} \leq 1.2V$. The difference between the maximum and minimum voltage ΔV_{in} that the ADC has to quantize is $0.4V$. The output is also linear and therefore bijective.

At $V_{in} = 0.6V$ the output Voltage is $V_{out} = 1.26V$. The hand calculated value would be $V_{in} + V_{off} = 0.6V + 0.6V = 1.2V$, which is only $60mV$ or $\frac{60mV}{1.26V} = 4.7\%$ off compared the simulated value. At other values of V_{in} the value V_{off} in the simulation differs much more compared to the chosen value in the hand calculations, but those were only made for the most common default cause of $V_{in} = 0.6V$.

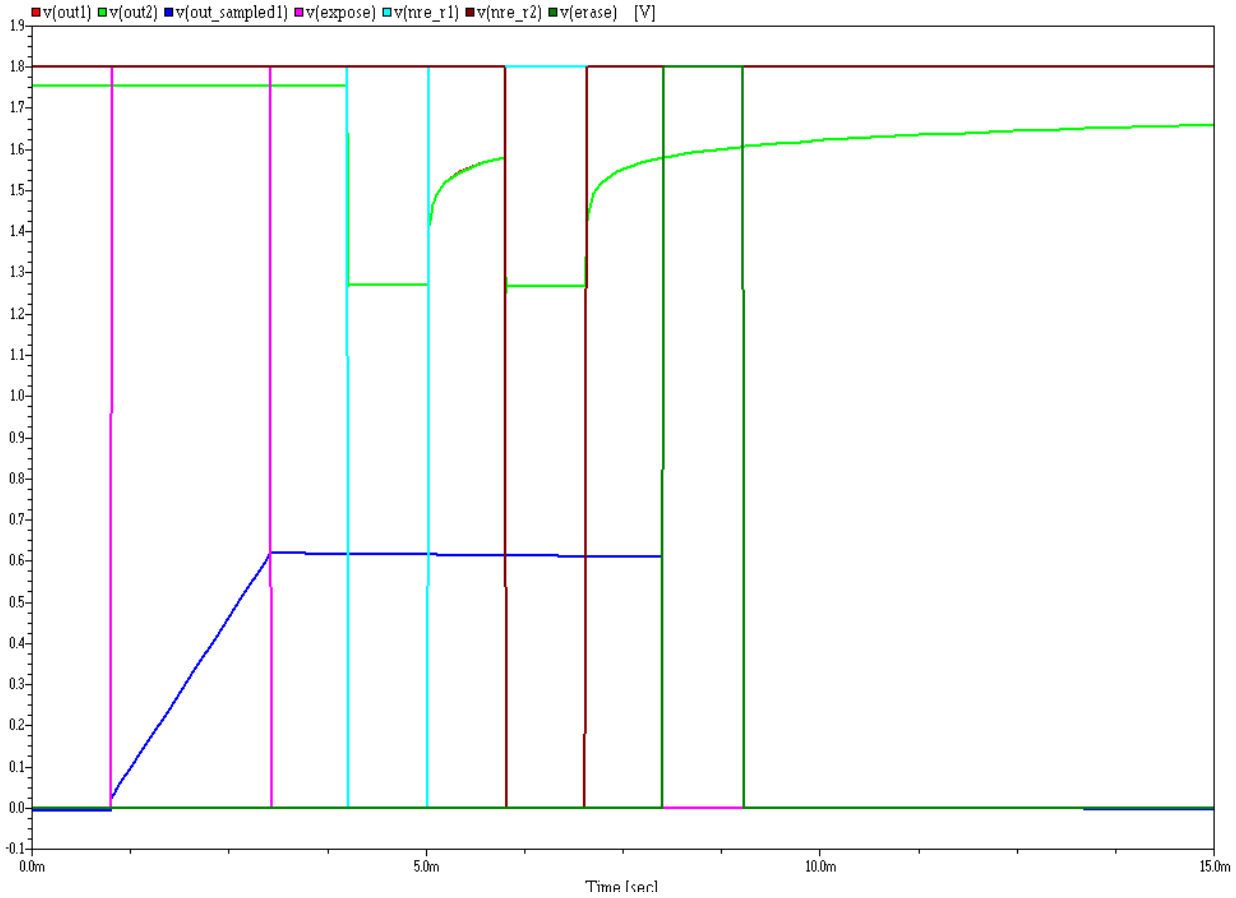


Figure 7: Spice simulation of the entire circuit for $I_{pd1} = 750pA$ and $t_{Expose} = 2ms$

3.1.2 Analog circuit

In Figure 7 all steps that are involved when a picture is taken are simulated with spice. The blue line represents the voltage of the capacitor CS. During the exposure phase ($1ms \leq t \leq 3ms$) the capacitor is charged with a constant current of $750pA$ up to $0.6V$ and holds the charge until it is discharged at $t = 8ms$. The in 2.1.1 calculated voltage matches the value from the simulation. During the readouts there is a small

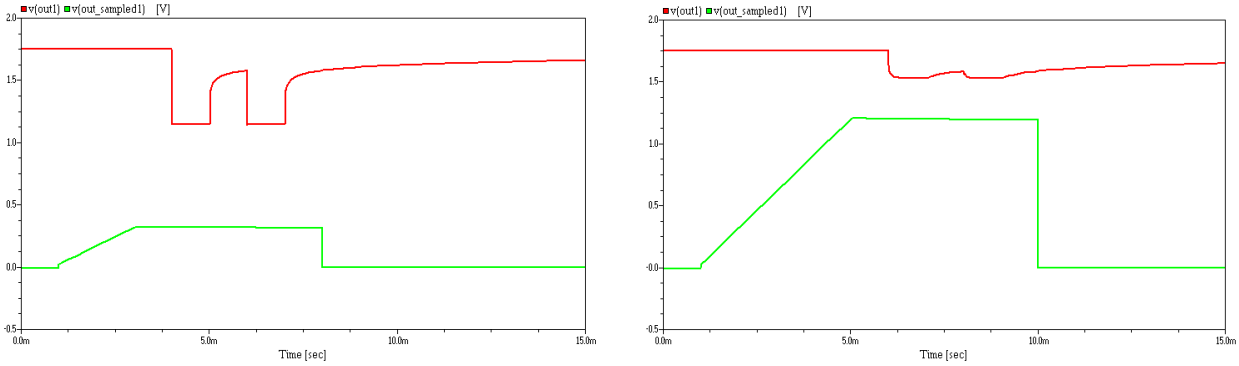
decrease of the charge/voltage, that could be caused by leakage, but does not have an impact on the output voltage which in contrast remains constant.

During the readout phases ($4ms \leq t \leq 5ms$ for row 1 and $6ms \leq t \leq 7ms$ for row 2) the NRE-signal is low which connects the two transistors of the amplifier (see Figure 2). The output capacitance is discharged by the amplifier to the to $V_{in} = V_{CS}$ corresponding output voltage. The capacitors CC1/2 are, as previous calculations in (2.1.3 suggested, discharged fast enough so that the signals are stable when the ADC converts them.

The simulations shows no unexpected behavior ore values that deviate more than what is normal from those calculated in chapter 2.

In Figure 8 the simulation is done with the in 2.1.1 discussed minimum and maximum values. All control signals that do not change compared to Figure 7 are left out for better visibility. In Figure 8(a) the current is set to $I_{pd1} = 375pA$ and exposure time to $t_{Expose} = 2ms$ which equals a minimum charge of $0.75pC$ and a voltage of $V_{CS} = 0.3V$. The simulation shows that everything works for the minimal assumed parameters for exposure time and current from the photo diode.

In Figure 8(b) the upper charge limit of $3pA$ for what the capacitor was sized for is simulated. To do this the exposure time was set to $4ms$ and the current to $750pA$. The calculated value of $V_{CS} = 1.2V$ is also identical to the simulated one. The amplifier needs more time to discharge the capacitors CC1/2, but is still able to produce stable signals within the $1ms$ timer period after that the ADC starts converting. Those simulations show that the circuit works for the entire voltage range $(0.3 - 1.2V)$ the capacitor was designed for.



(a) minimum charge: $Q_{min} = 0.75pC$

(b) maximum charge: $Q_{max} = 3pC$

Figure 8: Spice simulation for minimum (a) and maximum (b) assumed charge of CS

3.2 Digital

All digital simulations were done using Xilinx Vivado. Fig.9 shows the result from simulating the controller. The testbench used to simulate the circuit is in Listing 5 in the appendix.

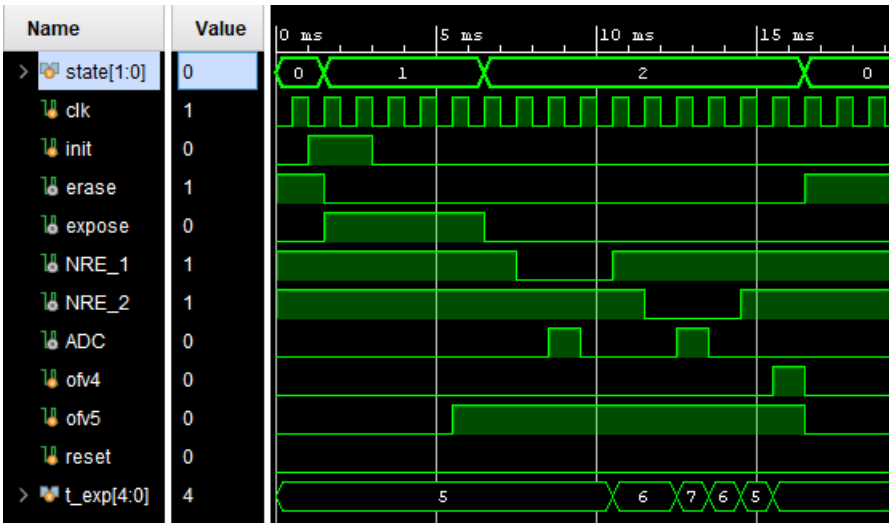


Figure 9: Digital simulation waveform

The controller starts in the idle state. The initiating signal "init" then changes the state to exposure. The exposure state is held for the amount of time indicated by the "t_exp"$register.Once$"$ovf5$"$istriggeredthecontrollermovesontot$

Once inside the readout state, the outputs follow the desired behavior. The final outputs in the readout state are held for one more clock cycle than required. The state then returns to idle once the overflow flag "ovf4" is triggered.

The exposure time of the is adjusted each clock cycle according to the increase and decrease input signals, see Fig.10. The option to increase the time is prioritized over decreasing the time.

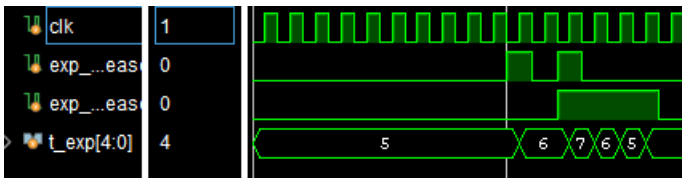


Figure 10: Exposure time adjustment

The new value of the exposure time is used the next time a picture is taken, (Fig.11).

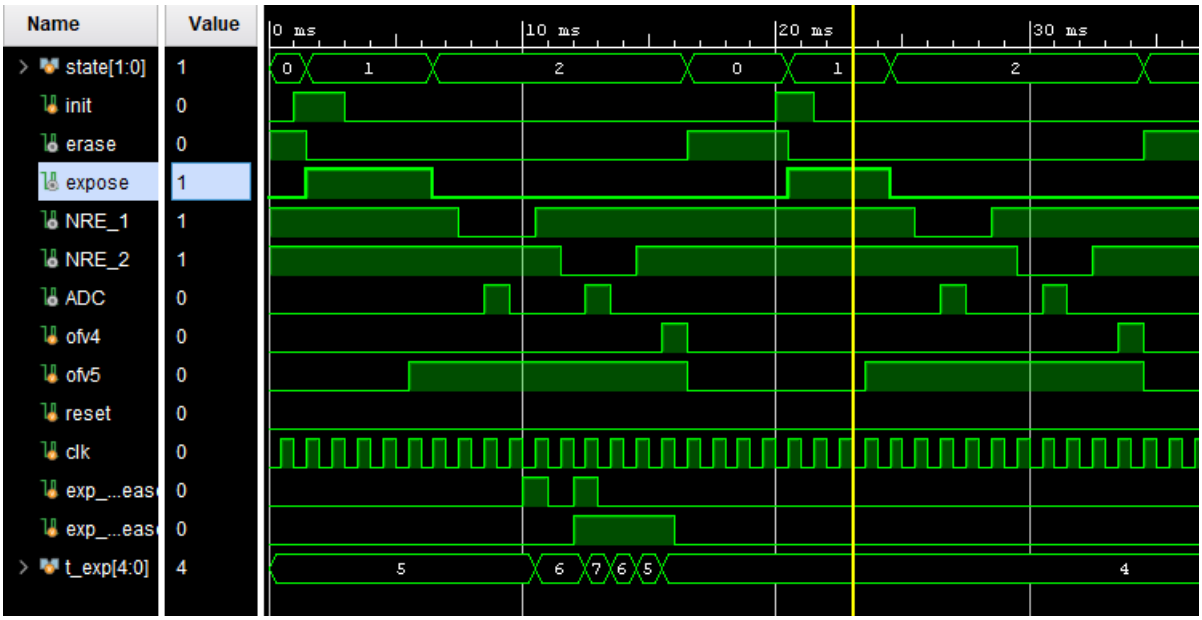


Figure 11: Exposure time change

The reset signal will reset the state back to idle (Fig.12).

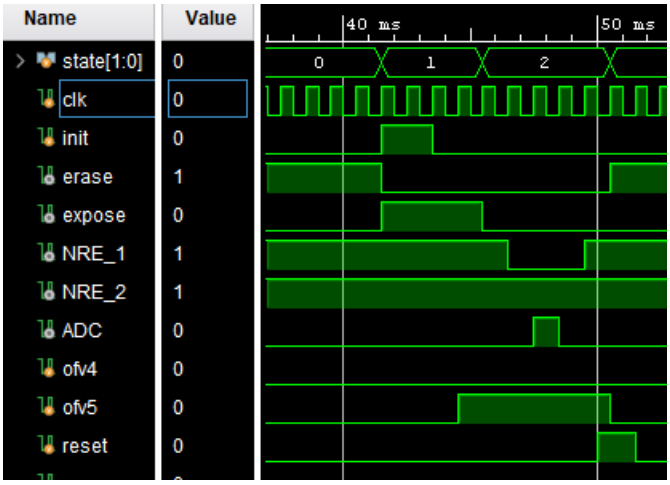


Figure 12: System reset

4 Results

4.1 Analog

The results from the hand calculations in 2 in general do not differ much compared to those obtained by simulations in 3.1.1.

The error in the hand calculations for the capacitor are as expected negligible, because the equations describe the behavior very precisely. All results from the transistor equations in contrast are only simplified descriptions of the real behavior and thus differ to some extend from the results obtained by the spice

simulations. All transistors were designed with the goal that this error is so small that it is not noticeable.

The transistors M1 and M2 responsible for controlling the exposure time and discharge of the capacitor are used as simple on-off switches. Important here is that they are switching fast enough and do not influence the rest of the circuit. In the simulations (Figure 7) the voltage of the capacitor does not show any signs of a e.g. (dis)charging curve of a RC-network and also all curves are linear. This means that the transistors behave as expected and intended.

The simulations for the amplifier are more complex and thus are likely to differ from the simplified hand calculations, which in addition were only made for one input voltage of $V_{in} = 0.6V$. For this value the difference to the simulations is only $60mV$ or about 5 %. This is better than what could be expected. For different input voltages the error of V_{off} is proportional to the $|V_{in} - 0.6V|$. At $V_{in} = 0.3V$ the error of V_{off} is $0.83V - 0.6V = 0.13V$ and for $V_{in} = 1.2$ even $0.27V$. This was expected, because the calculations were only made for one specific value of $V_{in} = 0.6V$ and because of the nonlinear characteristics of the transistor that do not change proportional to the voltage V_{in}. The transistor M4 changed the output voltage only to a very small extend so neglecting it in the amplifier calculations was admissible and did not result in a bigger error at $V_{in} = 0.6V$.

The simulations show that the circuit works for the in 2.1.1 specified voltage range of $0.3 - 1.2V$ which should cover all intended use cases and even work when there is a operating error by the user (e.g. wrong exposure time for given light conditions). The output voltage of the amplifier in Figure 6 ranges from $1.13V$ to $1.53V$ with a ΔV of $0.4V$ which should be enough for a standard ADC to convert the information without loosing to much data.

4.2 Digital

The RE controller just like it was designed to do. The simulations math up with the theoretical design.

Instead of having the whole digital circuit described in one module, the Verilog code could be split up into smaller submodules. Segmenting the module would make it easier to see the higher level design, but it would also make it harder to keep track what signal goes where. The code is already split into separate processes that are essentially submodules.

5 Conclusion

We achieved the goals set out for this project. The digital camera allows for digital processing of the light hitting the camera sensor.

The analog components of the circuit were sized by doing hand calculations which were later verified by simulating the circuit in spice. The hand calculations were quite accurate resulting in only a small error compared to the simulated values and only starts do differ if a different value for V_{in} compared to one assumed in the calculations is used.

The digital circuit, that controls the pixel exposure and readout, was implemented using an finite sate machine. The finite state machine made describing the behavior of the digital circuit, using Verilog, a fairly simple task. The results from the simulations where as expected.

A Code

A.1 Spice

Listing 1: Testbench for amplifier simulations

```
amp_test

M3 0 N001 m1out VDD PMOS l=0.84U w=5.04U
M5 Vout Vout VDD VDD PMOS l=0.36U w=2.16U
M4 m1out 0 Vout VDD PMOS l=0.36U w=5.04U
C1 Vout 0 3p    ! capacitance CC1/2
V1 VDD 0 1.8    ! supply voltage
Vin N001 0 0.6  ! input voltage

.plot dc V(Vout)

.include p18_cmos_models.inc
.include p18_model_card.inc
```

Listing 2: Pixel Circuit

```
.subckt PhotoDiode VDD N1
I1  VDD   N1   DC  Ipd_1
d1 N1 vdd dwell 1
.model dwell d cj0=1e-14 is=1e-12 m=0.5 bv=40
Cd1 N1 VDD 30f
.ends


.subckt pixelcircuit VDD 0 EXPOSE ERASE NRE OUT N2

.param W1 = 1.08U
.param L1 = 0.36U
.param W2 = 1.08U
.param L2 = 0.36U
.param W3 = 5.04U
.param L3 = 0.84U
.param W4 = 5.04U
.param L4 = 0.36U

X1 VDD N1 PhotoDiode
M1 N1 expose n2 0 NMOS L=L1 W=W1
C1 N2 0 2.5e-12                         ! Capacitor CS
M2 N2 erase 0 0 NMOS L=L2 W=W2
M3 0 N2 N3 VDD PMOS L=L3 W=W3
M4 N3 nre out VDD PMOS L=L4 W=W4

.ends


.subckt activeLoad VDD 0 OUT

M1 OUT OUT VDD VDD PMOS L=0.36e-6 W=2.16e-6
C1 OUT 0 3e-12

.ends
```

Listing 3: Spice testbench for analog circuit

```
testbench

.param Ipd_1 = 750p ! Photodiode current, range [50 pA, 750 pA]
.param VDD = 1.8 ! Supply voltage
.param EXPOSURETIME = 2m ! Exposure time, range [2 ms, 30 ms]

.param TRF = {EXPOSURETIME/100} ! Risetime and falltime of EXPOSURE and ERASE signals
.param PW = {EXPOSURETIME} ! Pulsewidth of EXPOSURE and ERASE signals
.param PERIOD = {EXPOSURETIME*10} ! Period for testbench sources
.param FS = 1k; ! Sampling clock frequency
.param CLK_PERIOD = {1/FS} ! Sampling clock period
.param EXPOSE_DLY = {CLK_PERIOD} ! Delay for EXPOSE signal
.param NRE_R1_DLY = {2*CLK_PERIOD + EXPOSURETIME} ! Delay for NRE_R1 signal
.param NRE_R2_DLY = {4*CLK_PERIOD + EXPOSURETIME} ! Delay for NRE_R2 signal
.param ERASE_DLY = {6*CLK_PERIOD + EXPOSURETIME} ! Delay for ERASE signal

VDD 1 0 dc VDD
VEXPOSE EXPOSE 0 dc 0 pulse(0 VDD EXPOSE_DLY TRF TRF EXPOSURETIME PERIOD)
VERASE ERASE 0 dc 0 pulse(0 VDD ERASE_DLY TRF TRF CLK_PERIOD PERIOD)
VNRE_R1 NRE_R1 0 dc 0 pulse(VDD 0 NRE_R1_DLY TRF TRF CLK_PERIOD PERIOD)
VNRE_R2 NRE_R2 0 dc 0  pulse(VDD 0 NRE_R2_DLY TRF TRF CLK_PERIOD PERIOD)

X11 1 0 EXPOSE ERASE NRE_R1 OUT1 OUT_SAMPLED1 pixelcircuit
X12 1 0 EXPOSE ERASE NRE_R1 OUT2 N12 pixelcircuit
X21 1 0 EXPOSE ERASE NRE_R2 OUT1 N21 pixelcircuit
X22 1 0 EXPOSE ERASE NRE_R2 OUT2 N22 pixelcircuit
Xmc1 1 0 OUT1 activeLoad
Xmc2 1 0 OUT2 activeLoad

.plot V(OUT1) V(OUT2) V(OUT_SAMPLED1) V(EXPOSE) V(NRE_R1) V(NRE_R2) V(ERASE)

.include C:\Users\Jonas\Documents\Uni\19W\design_of_integrated_circuits\project\PixelCircuit.txt
.include C:\Users\Jonas\Documents\Uni\19W\design_of_integrated_circuits\project\p18_cmos_models.inc
.include C:\Users\Jonas\Documents\Uni\19W\design_of_integrated_circuits\project\p18_model_card.inc
```

A.2 Verilog

Listing 4: RE controller

```
1  `timescale 1us / 1ns
2
3  module RE_control(
4      input exp_increase,
5      input exp_decrease,
6      input clk,
7      input reset,
8      input init,
9      output NRE_1,
10     output NRE_2,
11     output ADC,
12     output expose,
13     output erase
14     );
15     // FSM states
16     parameter [1:0] idle = 2'b00;
17     parameter [1:0] exposure = 2'b01;
18     parameter [1:0] readout = 2'b10;
19
20     // registers
21     reg [1:0] state;         // The current state
22     reg [4:0] t_exp;         // Exposure time
23     reg [4:0] t_read;        // Readout time
24     reg [4:0] exp_counter ; // Counts up to t_exp
25     reg [4:0] read_counter; // Counts up to t_read
26     reg ofv4;                // triggered when readout complete
27     reg ofv5;                // triggered when exposure complete
28     //output registers
29     reg NRE_1_r;
30     reg NRE_2_r;
31     reg ADC_r;
32     reg expose_r;
33     reg erase_r;
34     // R stores the outputs of ADC, NRE_1 and NRE_2 used during the readout state
35     reg [2:0] R [9:0];
36
37     initial begin
38         state = idle;
39         t_exp = 5;
40         t_read = 9; ///maybe 9
41         exp_counter = 0;
42         read_counter = 0;
43         ofv4 = 0;
44         ofv5 = 0;
45         NRE_1_r = 1;
46         NRE_2_r = 1;
47         ADC_r = 0;
48         expose_r = 0;
49         erase_r = 1;
50         R[0] = 3'b110;
51         R[1] = 3'b110;
52         R[2] = 3'b010;
53         R[3] = 3'b011;
54         R[4] = 3'b010;
55         R[5] = 3'b110;
56         R[6] = 3'b100;
```

```
57          R[7] = 3'b101;
58          R[8] = 3'b100;
59          R[9] = 3'b110;
60      end
61
62      // assigning the outputs to the output registers
63      assign NRE_1 = NRE_1_r;
64      assign NRE_2 = NRE_2_r;
65      assign ADC = ADC_r;
66      assign expose = expose_r;
67      assign erase = erase_r;
68
69      // state control
70      always @(posedge clk) begin
71          case (state)
72              idle: begin
73                  if (init == 1 && reset == 0)
74                      state = exposure;
75                  else
76                      state = idle;
77                  end
78              exposure: begin
79                  if (ofv5 == 1)
80                      state = readout;
81                  else if (reset == 1)
82                      state = idle;
83                  else
84                      state = exposure;
85                  end
86              readout: begin
87                  if (ofv4 == 1 || reset == 1)
88                      state = idle;
89                  else
90                      state = readout;
91                  end
92              default:  begin state = idle; end
93          endcase
94      end
95
96      // counters
97      always @(posedge clk)
98          case (state)
99              exposure: begin
100                 if (exp_counter < t_exp - 1)
101                     exp_counter = exp_counter +1;
102                 else
103                     ofv5 = 1; // exposure complete
104                 end
105             readout: begin
106                 if (read_counter < t_read )
107                     read_counter = read_counter +1;
108                 else
109                     ofv4 = 1; // readout complete
110                 end
111             default: begin
112                 exp_counter = 0;
113                 read_counter = 0;
114                 ofv4 = 0;
115                 ofv5 = 0;
```

```
                end
        endcase

    // exposure control
    always @(posedge clk)
        if ((exp_increase == 1)&& (t_exp < 30 && t_exp >= 2))
            t_exp = t_exp + 1;
        else if((exp_decrease == 1)&& (t_exp <= 30 && t_exp > 2))
            t_exp = t_exp - 1;

    // outputs
    always @(posedge clk)
        case (state)
        exposure: begin
            NRE_1_r = 1;
            NRE_2_r = 1;
            ADC_r = 0;
            expose_r = 1;
            erase_r = 0;
            end
        readout: begin
            NRE_1_r = R[read_counter][2];
            NRE_2_r = R[read_counter][1];
            ADC_r = R[read_counter][0];
            expose_r = 0;
            erase_r = 0;
            end
        default: begin  // this includes idle
            NRE_1_r = 1;
            NRE_2_r = 1;
            ADC_r = 0;
            expose_r = 0;
            erase_r = 1;
            end
         endcase

endmodule
```

Listing 5: RE controller testbench

```
`timescale 1us / 1ns

module RE_control_tb();

    reg exp_increase;
    reg exp_decrease;
    reg clk;
    reg reset;
    reg init;
    wire NRE_1;
    wire NRE_2;
    wire ADC;
    wire expose;
    wire erase;

  RE_control RE(//
        .exp_increase(exp_increase),
        .exp_decrease(exp_decrease),
        .clk(clk), .reset(reset),
```

```
20          .init(init),
21          .NRE_1(NRE_1),
22          .NRE_2(NRE_2),
23          .ADC(ADC),
24          .expose(expose),
25          .erase(erase));
26
27      initial begin
28      clk = 0;
29      forever #500 clk = ~clk;
30      end
31
32      initial begin
33      init = 0;
34      #1000 init = 1;
35      #2000 init = 0;
36      #17000 init = 1;
37      #1500 init = 0;
38      #20000 init = 1;
39      #2000 init = 0;
40      end
41
42      initial begin
43      exp_increase = 0;
44      #10000 exp_increase = 1;
45      #1000 exp_increase = 0;
46      #1000 exp_increase = 1;
47      #1000 exp_increase = 0;
48      end
49
50      initial begin
51      exp_decrease = 0;
52      #12000 exp_decrease = 1;
53      #4000 exp_decrease = 0;
54      end
55
56      initial begin
57      reset = 0;
58      #50000 reset = 1;
59      #1500 reset = 0;
60      end
61
62  endmodule
```