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EE540 HW#4

Design Procedure

Control unit of the CPU is implemented as a module. It decodes the current instruction and generates control signals for datapath, data memory and determines the next PC value. Control signals used in the design are given as follows:

Control Signal	***Length(bit)***	***Function***
ImFlag	1	HIGH if an immediate value is given in the instruction, LOW otw.
shiftFlag	1	HIGH if a shift instruction is given, LOW otw.
mem_r	1	HIGH if a LOAD instruction is given, LOW otw.
mem_w	1	HIGH if a STOR instruction is given, LOW otw.
reg_w	1	HIGH if register file of the CPU needs to be written, LOW otw.
comp_Flag	1	HIGH if a CMP instruction is given, LOW otw.
s_ext	1	HIGH if sign extension required for the immediate value, LOW otw.
jcond	1	HIGH if a Jcond instruction is given, LOW otw.
jal	1	HIGH if a JAL instruction is given, LOW otw.
branch	1	HIGH if a Bcond instruction is given, LOW otw.

Table 1: Control Signal Descriptions

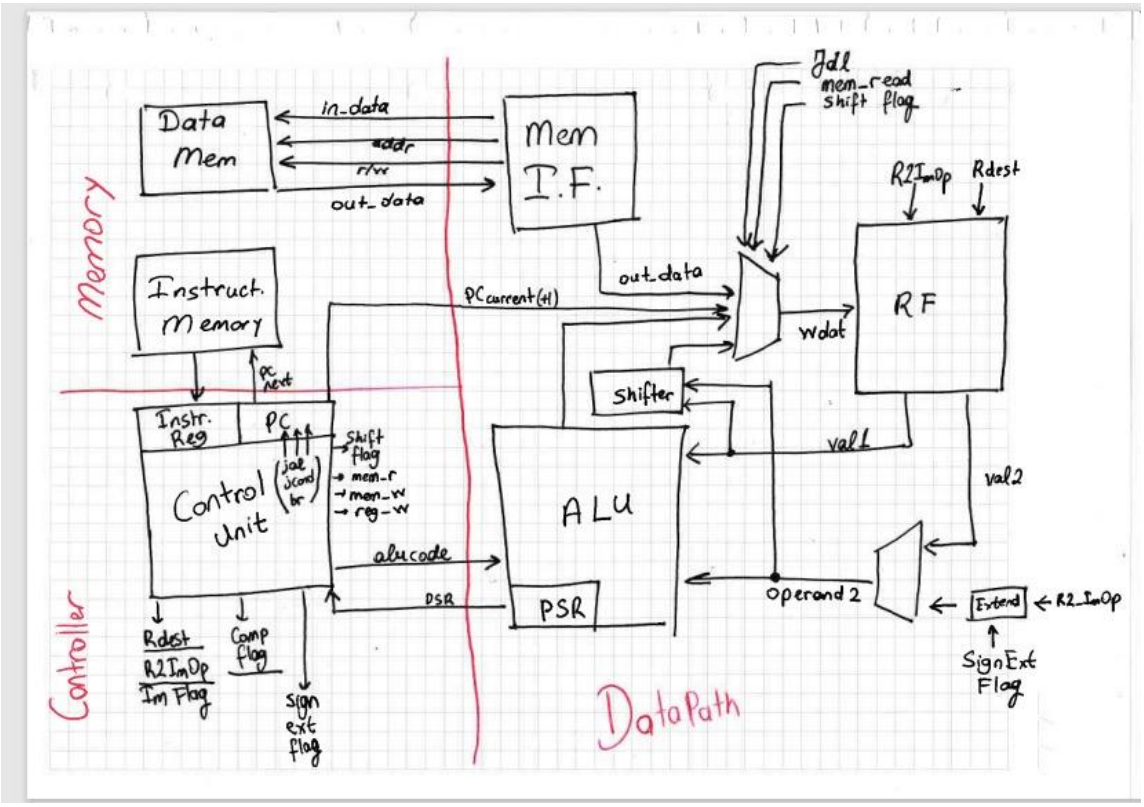

Fig. 1: Proposed Circuit Block Diagram

Datapath of the CPU is not explicitly implemented as a module since it consists of an ALU, a 16-bit 16-word register file and a 16-bit barrel shifter. Components of datapath are instantiated in the top module.

spblockram.v module given in the homework is used to implement the 32-words 16-bit data memory of the CPU.

Simulation Results

To indicate that both datapath and control unit works properly, the entire microprocessor with data and instruction memories are implemented and simulated together.

Test instructions in the HW5 is used for simulation. In addition, Jcond and JAL instructions are given to the CPU to test jump operation. It can be seen that the program counter updates properly after Bcond, Jcond and JAL instructions. (Bcond -> 29 to 40, Jcond -> 49 to 56, JAL -> 60 to 12).

dout shows the R0 content in register file. It is checked that R0 content updates accordingly after relevant instruction.

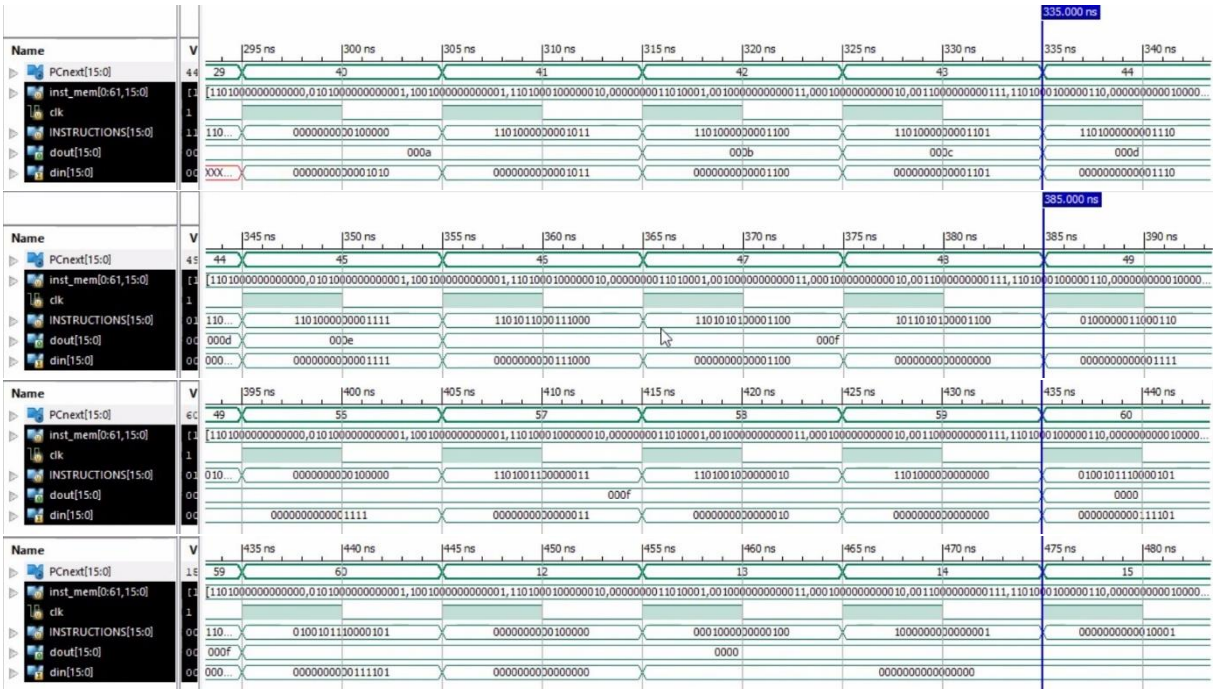

Fig. 2: Simulation Results

Synthesis Outputs

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	292	18224	1%
Number of Slice LUTs	510	9112	5%
Number of fully used LUT-FF pairs	68	734	9%
Number of bonded IOBs	33	232	14%
Number of BUFG/BUFGCTRLs	1	16	6%

```
Primitive and Black Box Usage:
------------------------------
# BELS                          : 633
#      GND                     : 1
#      INV                     : 1
#      LUT1                    : 15
#      LUT2                    : 2
#      LUT3                    : 15
#      LUT4                    : 36
#      LUT5                    : 146
#      LUT6                    : 279
#      MUXCY                   : 15
#      MUXF7                   : 74
#      MUXF8                   : 32
#      VCC                     : 1
#      XORCY                   : 16
# FlipFlops/Latches            : 292
#      FD                      : 21
#      FDE                     : 257
#      LD                      : 14
# RAMS                         : 6
#      RAM32M                  : 2
#      RAM32X1D                : 4
# Clock Buffers                : 1
#      BUFGP                   : 1
# IO Buffers                   : 32
#      IBUF                    : 16
#      OBUF                    : 16
```

Fig. 3: Resource Usage

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 12.002ns (Maximum Frequency: 83.319MHz)
   Minimum input arrival time before clock: 14.265ns
   Maximum output required time after clock: 4.240ns
   Maximum combinational path delay: No path found

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 12.002ns (frequency: 83.319MHz)
  Total number of paths / destination ports: 582304 / 344
-------------------------------------------------------------------------
Delay:               12.002ns (Levels of Logic = 11)
  Source:            CPU0/RF0/rg[14].rg16/rgstr[1].df/q (FF)
  Destination:       CPU0/ALU0/W_psr_6 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

Fig. 4: Timing Reports

In the timing summary, the maximum allowable clock frequency of the CPU is around 83 MHz, which satisfies timing requirements of a typical microprocessor applications.