EE 540 FINAL PROJECT

FFT IMPLEMENTATION FOR FPGA

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The project includes an FFT design for FPGAs. Altough it has not been tested yet on hardware, the simulation and synthesis results can be found on this report.

The project consists of: Real addition, real subtraction, real multiplication, real division, complex addition, complex multiplication, square root, logarithm, arctan, and magnitude & phase calculation blocks, in addition to FFT module.

Design Overview

Radix-2 FFT algorithm with IEEE 754 single precison floating point format is implemented. The point amount of FFT is parameterized in order to make the design adjustable for different architectures.

Operation

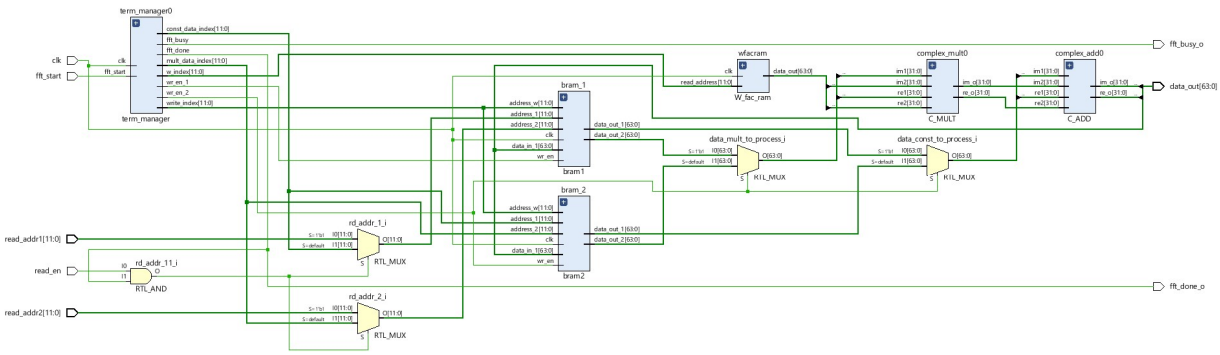

Figure 1: RTL Schematic of Design

As can be seen in the RTL Schematic of the design, the FFT module contains 3 BRAMs, one 'term_manager' module and complex add and complex multiplication modules. 2 dual port BRAMs are used to store data between stages and one BRAM is used to store W factors.

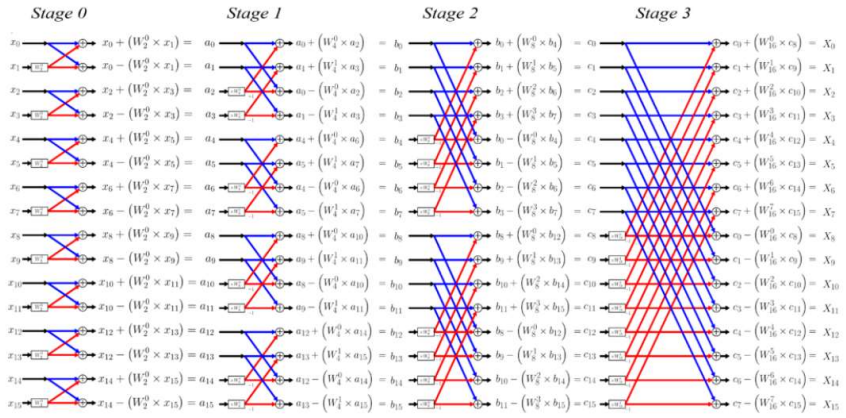

Figure 2: 16 Point Radix-2 FFT [1]

Once the ‘fft_start’ signal arives, the operation starts. In the first stage of the operation, the input samples are read from one dual port BRAM, the corresponding node is calculated with complex arithmetic modules and the results are written to other BRAM. At the end of a stage, the read and write BRAMs switch and the process goes on until final result is ready. The ‘fft_done’ signal indicates that FFT is finished. ‘term_manager’ module controls the process with write enable and address signals.

Synthesis Results

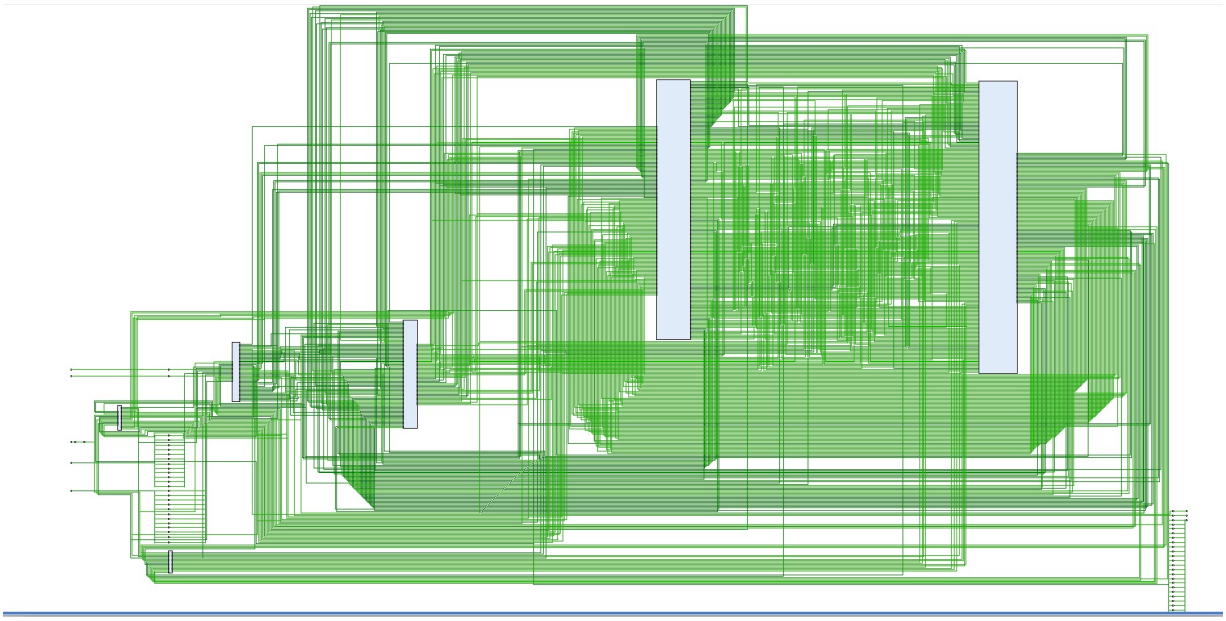

Figure 3: Synthesized Schmatic for 4096 point FFT design

The resource usage for 4096-Point FFT module is as follows:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2598	0	53200	4.88
LUT as Logic	2598	0	53200	4.88
LUT as Memory	0	0	17400	0.00
Slice Registers	309	0	106400	0.29
Register as Flip Flop	61	0	106400	0.06
Register as Latch	248	0	106400	0.23
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	38	0	140	27.14
RAMB36/FIFO*	36	0	140	25.71
RAMB36E1 only	36			
RAMB18	4	0	280	1.43
RAMB18E1 only	4			

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	8	0	220	3.64
DSP48E1 only	8			

7. Primitives

Ref Name	Used	Functional Category
LUT6	1215	LUT
LUT3	570	LUT
LUT5	521	LUT
LUT4	509	LUT
LUT2	366	LUT
LDCE	248	Flop & Latch
CARRY4	142	CarryLogic
OBUF	66	IO
FDRE	55	Flop & Latch
RAMB36E1	36	Block Memory
IBUF	27	IO
LUT1	19	LUT
DSP48E1	8	Block Arithmetic
FDSE	6	Flop & Latch
RAMB18E1	4	Block Memory
BUFG	1	Clock

Simulation Results

Simulation result for 16-Point FFT is as follows.

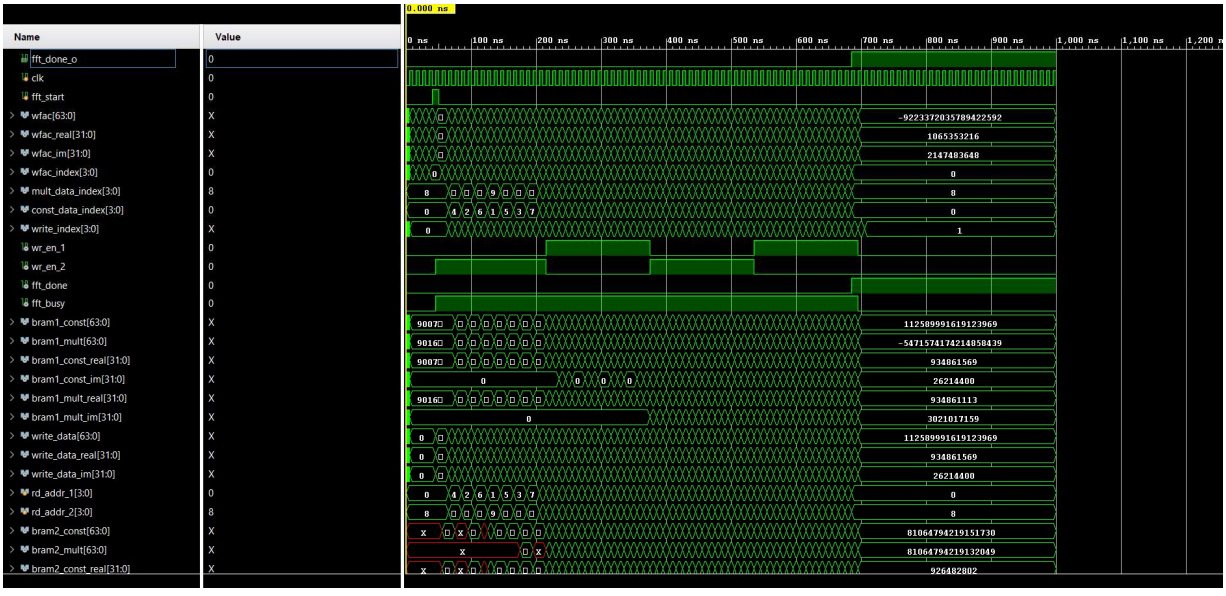

Figure 3: Simulation Results for 16 Point FFT

The final FFT results for 4096 Point FFT is checked via MATLAB.

MATLAB **vs** **FFT Module**

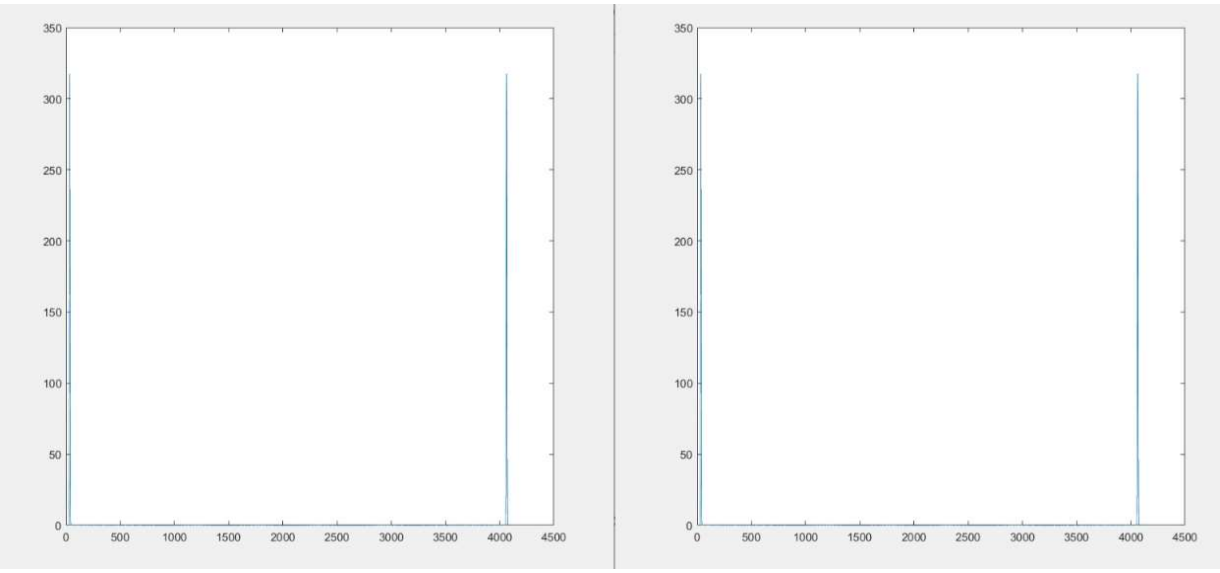

Figure 4: Magnitude comparison

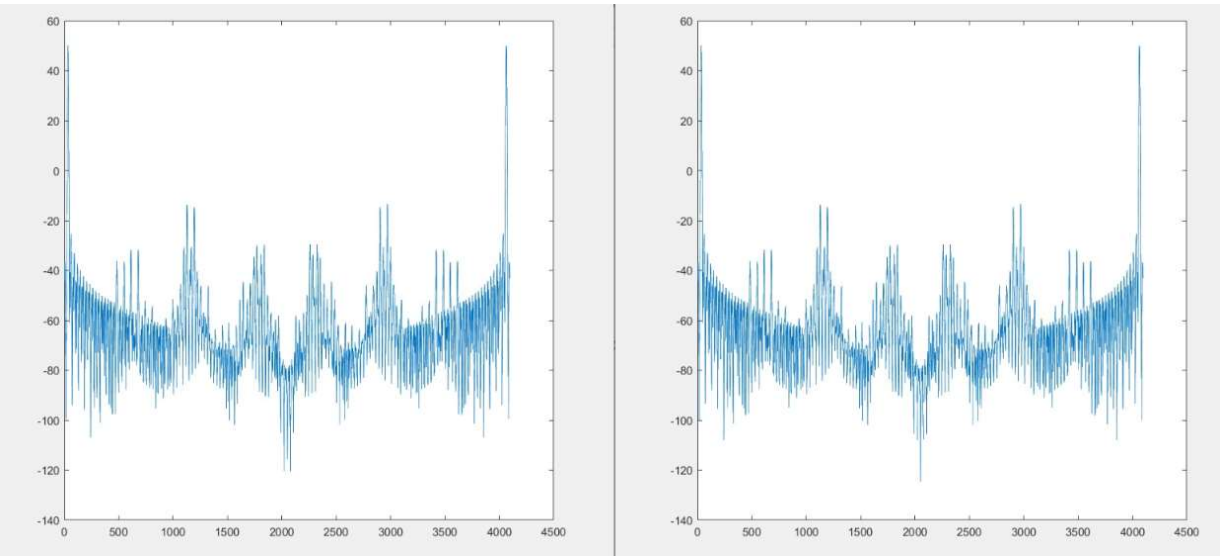

Figure 5: dB comparison

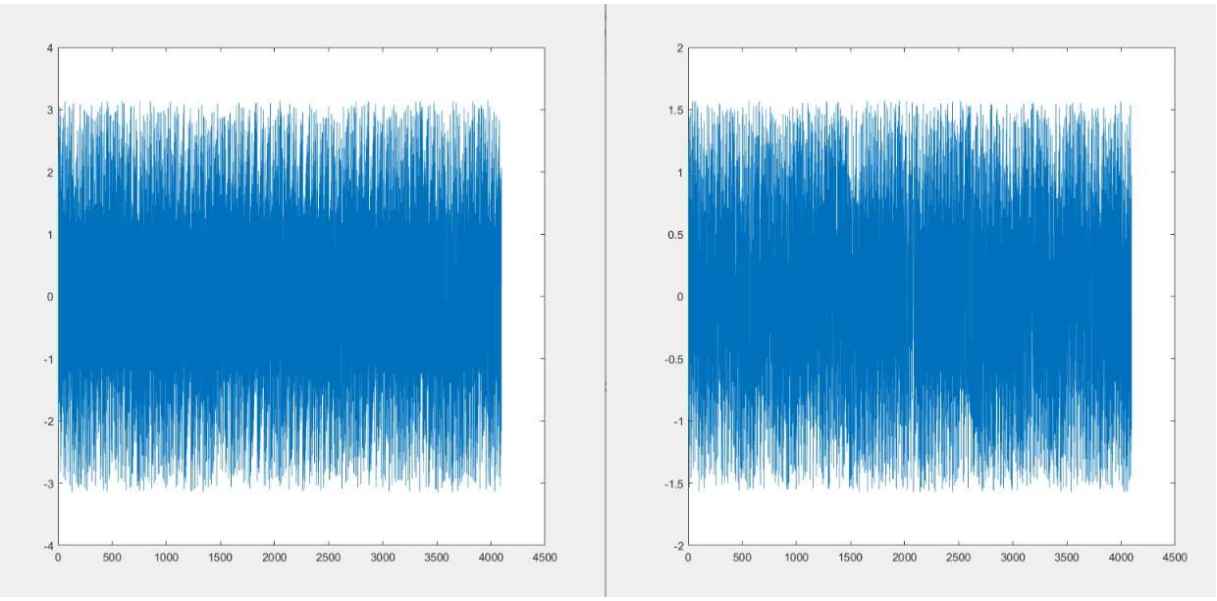

Figure 6: Phase comparison

References

[1] http://www.themobilestudio.net/the-fourier-transform-part-14