Computer Architecture (CS F342)

Design and Analysis of Instructions

Design of Datapath & CU for MIPS-based Pipelined Processor

MIPS-based pipelined processor

- Powerful way to improve the throughput
- Divide the single-cycle implementation
  - Fetch
  - Decode
  - Execute
  - Memory
  - Writeback
- A commercial MIPS processor: R2000/R3000

Latency of each instructions is unchanged, but throughput is ideally 5-times better

MIPS-based pipelined processor

- Delay/slow elements
  - Reading & writing the memory
  - Register file
  - ALU operation
- Each stage takes almost same amount of time
  - Consists of one slow element

Comparison of timing diagram

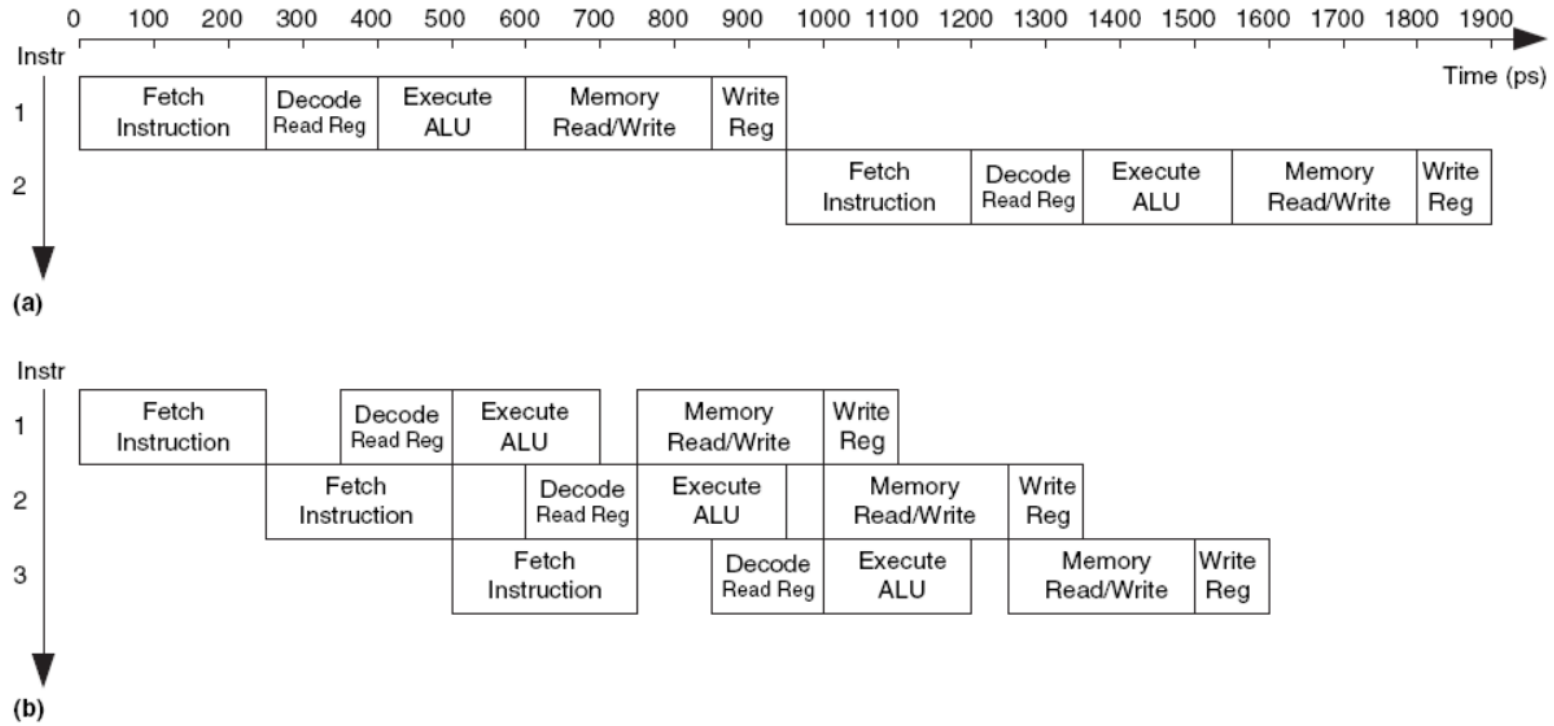
- Delay of the elements

Element	Parameter	Delay (ps)
Register clk-to-Q	T_{pcq}	30
Register setup	T_{setup}	20
Multiplexer	T_{mux}	25
ALU	T_{ALU}	200
Memory read	T_{mem}	250
Register file read	t_{RFread}	150
Register file setup	$t_{RFsetup}$	20

Critical Time
= Clock Time period

Comparison of timing diagram

- Delay of MUX & register is not included



Timing diagram of (a) single-cycle processor (b) pipelined processor

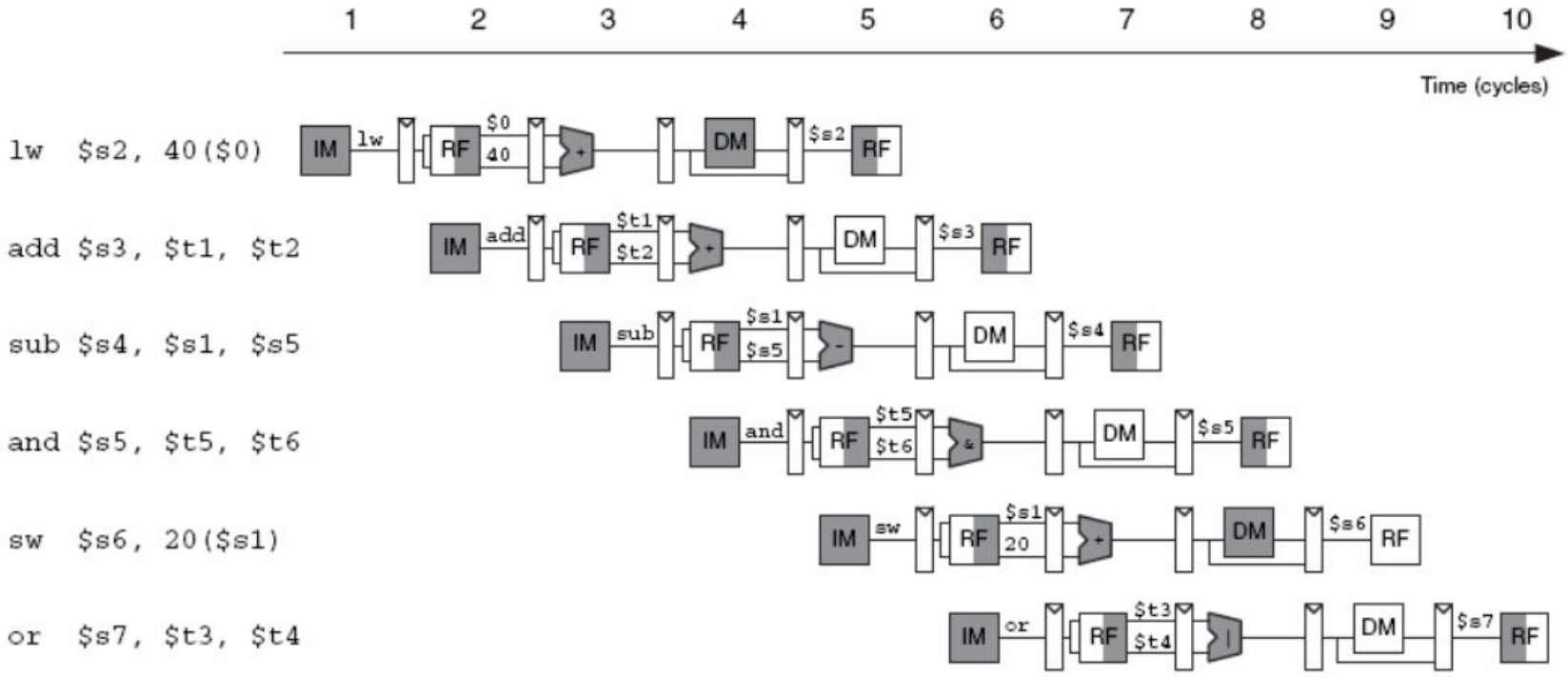
Comparison of timings

- **Single-cycle processor**
  - Instruction latency is 950 ps
  - Throughput 1 instruction per 950 ps
  - 1.05 billions instruction per second

- **Pipelined processor**
  - Length of pipeline stage is 250 ps (mem. access)
  - Instruction latency is 5*250 = 1250 ps
  - Throughput 1 instruction per 250 ps
  - 4 billions instructions per seconds

A view of pipeline in operation

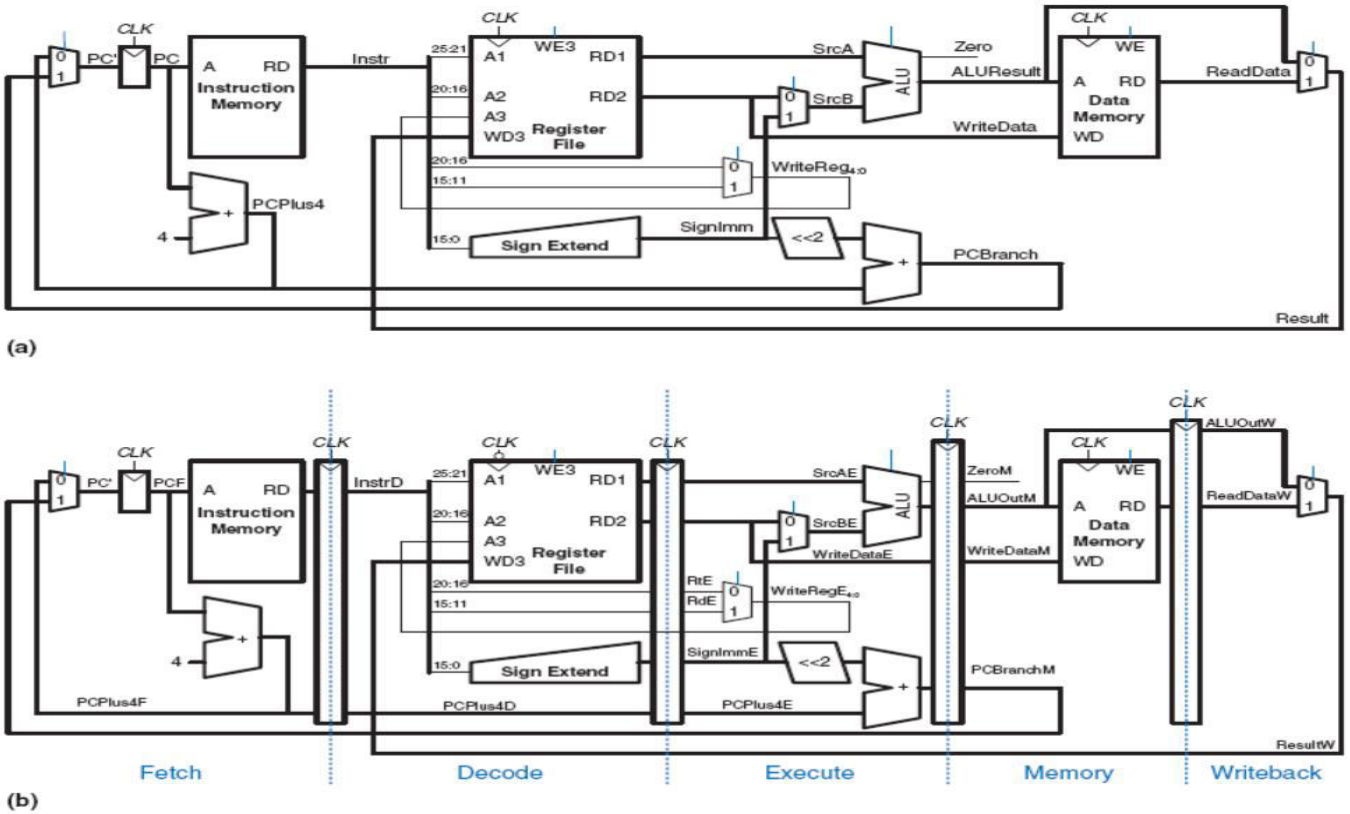
- Major component—instruction memory (IM), register file (RF) read, ALU execution and data memory (DM)
- Register file: write operation in the first part of a cycle and read in the second part



As we are breaking the cycle into multiple cycles, we would need latches. The latches store the intermediate values necessary to be taken forward.

Pipelined Datapath

- Datapath is formed by chopping the single-cycle datapath
  - Five stages separated by pipeline registers



Single-cycle

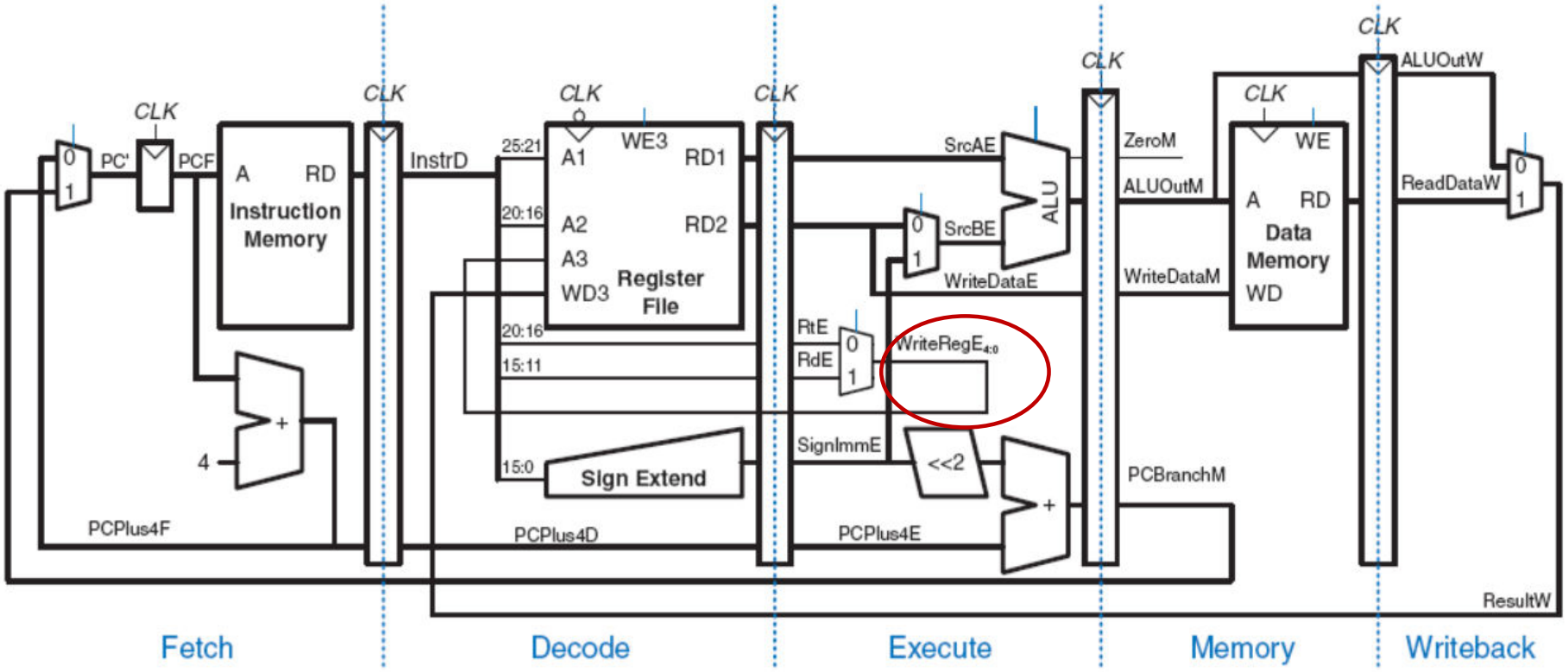
Pipelined

Is this datapath correct?

The data path is incorrect. The reg no. of the register to be written finally isn't forwarded till the 5th cycle. By that time, some other instruction in the pipeline might come and change the reg no. to be written. So, always forward all this info to the next latches until they are needed.

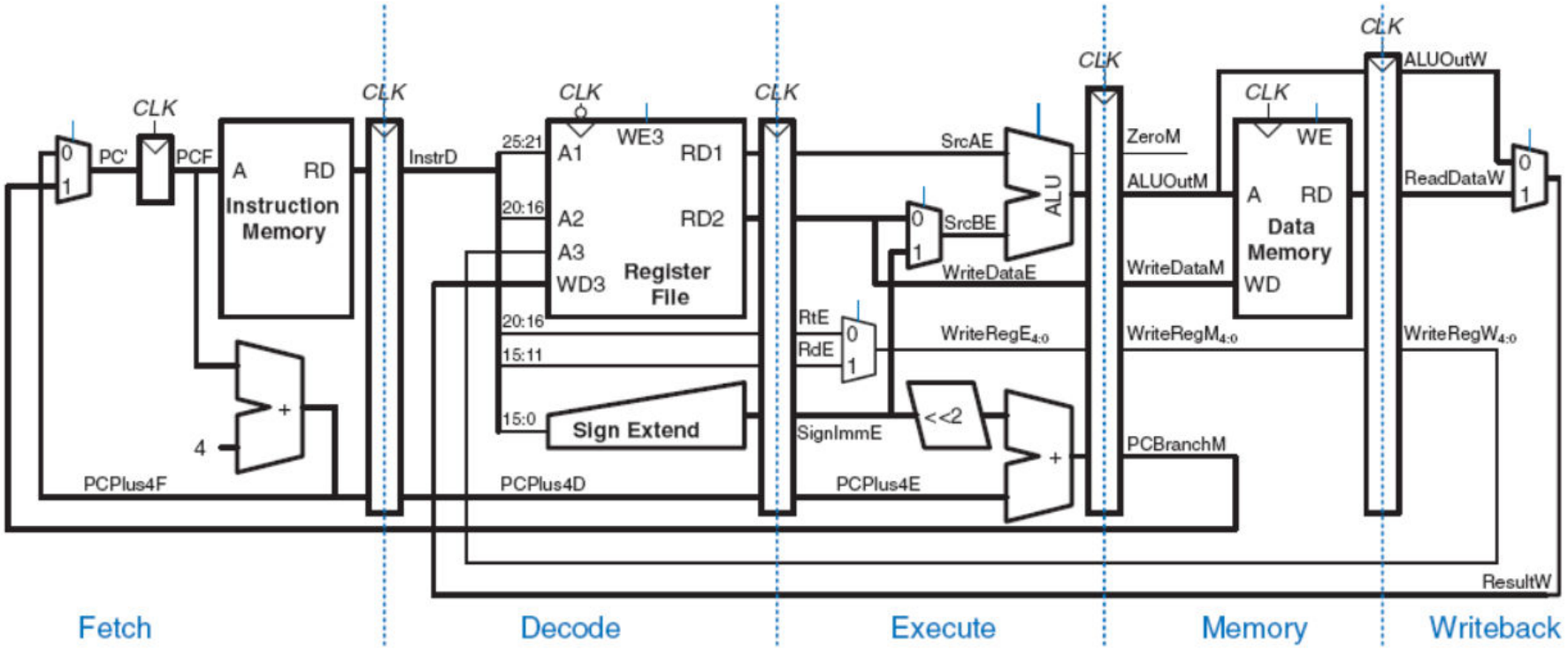
Pipelined Datapath

- Error in the datapath connection



Pipelined Datapath

- Modified datapath

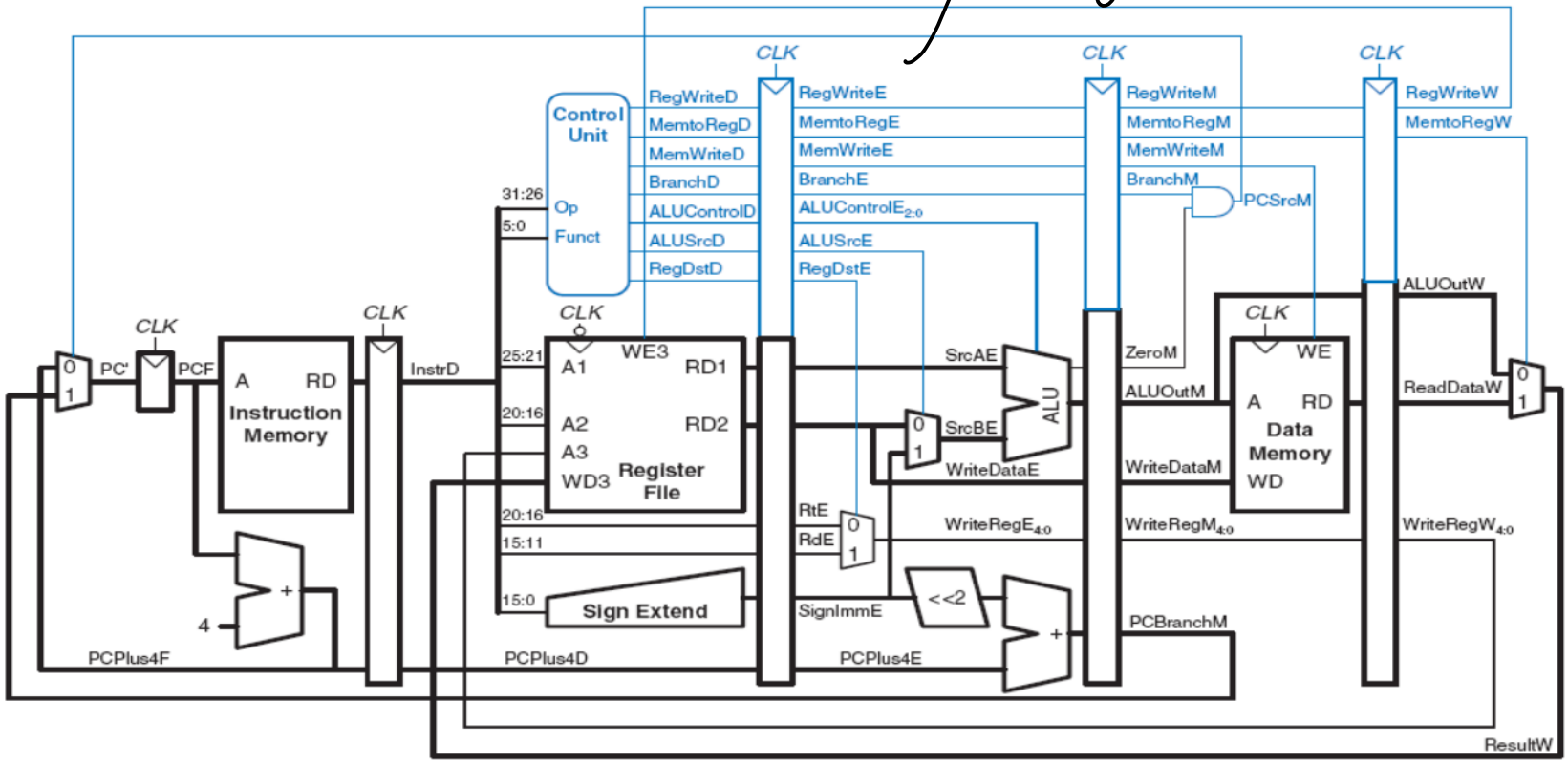


Is there any error in the datapath?

Pipelined Datapath & Control

- CU as in Single-cycle
- Control signals must be pipelined (remain synchronized with instruction)

All the control signals should also be carried in the latches



Summary

- Comparison between single-cycle and pipelined processor
- View of pipeline in operation
- Datapath and CU for pipelined processor