Cadence Project: Part 1

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1 Introduction

This project models and examines MOS transistors. By using Cadence Virtuoso, the designs of the N-Mos and P-Mos can be modified on the transistor-level for behavior analysis.

Given parameters for this project:

- For 0.5 μm CMOS technology:
  - Vdd = 5V,
  - V_{Tn0}= 0.73V, k$\prime$n= μnCox = 115μA/V^2,
  - V_{Tp0}=-0.94V, k$\prime$p = μpCox = 37μA/V^2
- Long channel transistor characteristics:
  - C_{ox}=2.5$\cdot 10^{-3}$ F/m^2
  - $L_S = L_D$ = 1.5 μm
    - Nmos:
      - C_j = 4.16$\cdot 10^{-4}$F/m^2,
      - C_{jsw} = 3.26$\cdot 10^{-10}$F/m,
      - C_{GD0}=C_{GS0}=1.93$\cdot 10^{-10}$F/m.
    - Pmos:
      - C_j = 7.1$\cdot 10^{-4}$F/m^2,
      - C_{jsw} = 2.18$\cdot 10^{-10}$F/m,
      - C_{GD0}=C_{GS0}=2.28$\cdot 10^{-10}$F/m.

2 Problem 1

First R_{sqn} and R_{sqp} are calculated in Problem 1.A.Then, R_{sqn} and R_{sqp} are later used in Problem 1.B to determine the corresponding pull-up and pull-down times (t_{pHL}, t_{pLH}). Minimum sized Nmos and Pmos transistors are defined as:

$$W_N = 1.8\mu m, W_P = 1.8\mu m, L_N = L_P = 0.6\mu m$$

2.1 Problem 1.A

By plotting the I_d vs V_{ds} characteristics, R_{eqn}, and R_{eqp} can be estimated using :

$$R_{eq} = \frac{R_{on1(Vout=Vdd)} + R_{on2(Vout=Vdd/2)}}{2}$$

where

$$R_{on1(Vout=Vdd)} = V_{dd}/I_{d(V_{out}=V_{dd})}$$
$$R_{on2(Vout=Vdd/2)} = V_{dd}/I_{d(V_{out}=V_{dd/2})}$$

Calculations based on Virtuoso simulation:
Nmos:

$$R_{on1(Vout=Vdd)} = V_{dd}/I_{d(V_{out}=V_{dd})} = 8.2025k \quad (1)$$
$$R_{on2(Vout=Vdd/2)} = V_{dd}/I_{d(V_{out}=V_{dd/2})} = 4.376k \quad (2)$$
$$R_{eqn} = \frac{8.2025k + 4.376k}{2} = 6.2892k \quad (3)$$

To determine R_{sqn}, use:

$$R_{sqn} = \frac{W_n}{L_n} \cdot R_{eqn}$$

$$R_{sqn} = \frac{1.8\mu m}{.6\mu m} \cdot 6.2892k = 18.868k \quad (4)$$

Pmos:

$$R_{on1(Vout=Vdd)} = V_{dd}/I_{d(V_{out}=V_{dd})} = 7.821k \quad (5)$$
$$R_{on2(Vout=Vdd/2)} = V_{dd}/I_{d(V_{out}=V_{dd/2})} = 12.95k \quad (6)$$
$$R_{eqp} = \frac{7.821k + 12.95k}{2} = 10.39k \quad (7)$$

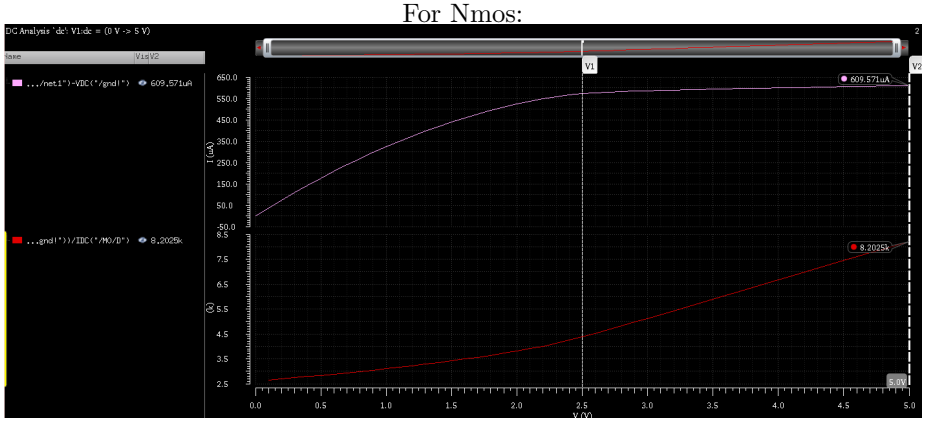
To determine R_{sqp}, use:

$$R_{sqp} = \frac{W_p}{L_p} \cdot R_{eqp}$$

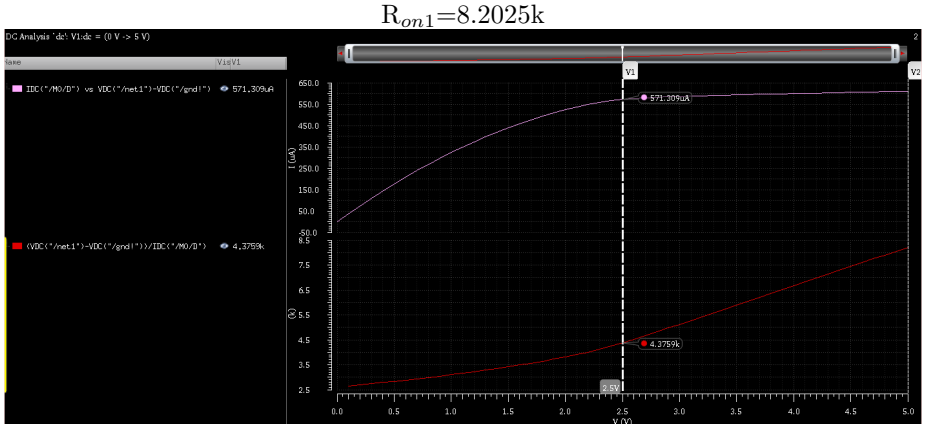
$$R_{sqp} = \frac{1.8\mu m}{.6\mu m} \cdot 10.39k = 31.157k \quad (8)$$

Using simulations on Cadence Virtuoso to determine corresponding R_{on1}, and R_{on2}.

For Nmos:

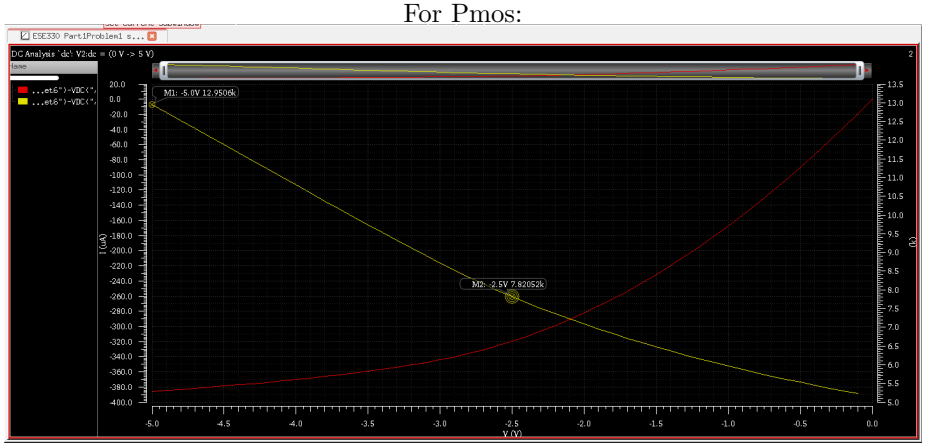


R_{on1}=8.2025k



R_{on2}=4.376k

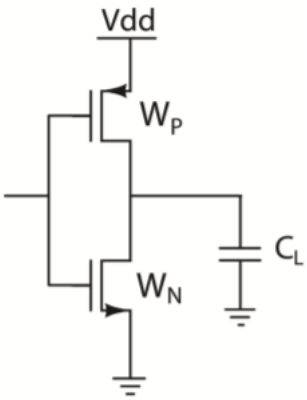
For Pmos:



R_{on1}=7.821k and R_{on2}=12.95k

2.2 Problem 1.B

Using R_{sqn} and R_{sqp}, from Problem 1.A, t_{pHL}, t_{pLH} can be determined with a capacitance load of 15pF as shown in the figure below:



Hand calculations:
Calculating t_{pHL} using (4):

$$t_{pHL} = .69 R_n C_L \tag{9}$$

$$R_n = \frac{L_n}{W_n} \cdot R_{sqn} \tag{10}$$

$$R_n = \frac{.6\mu m}{1.8\mu m} \cdot 18.868k = 6.289k \tag{11}$$

$$t_{pHL} = .69(6.289k)(15pF) = 65ns \tag{12}$$

Calculating t_{pLH} using (8):

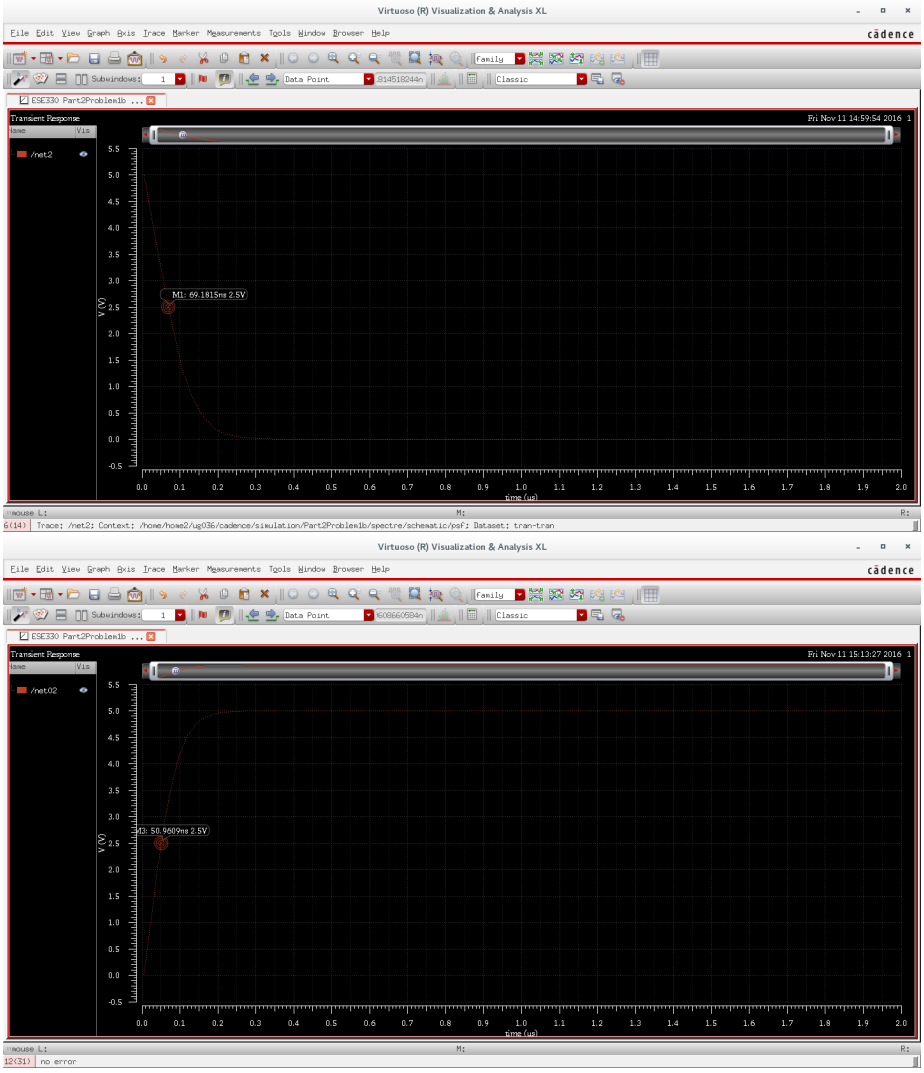
$$t_{pLH} = .69 R_p C_L \tag{13}$$

$$R_p = \frac{L_p}{W_p} \cdot R_{sqp} \tag{14}$$

$$R_p = \frac{.6\mu m}{3.6\mu m} \cdot 31.157k = 5.19k \tag{15}$$

$$t_{pLH} = .69(5.19k)(15pF) = 53ns \tag{16}$$

Simulations using Cadence Virtuoso :



t_{pHL}=69.18ns and t_{pLH}=50.96ns (respectively)

Comparison(ns) with 15pF load:		
	t_{pHL}	t_{pLH}
Hand Calc.	65	53
Simulation	69.18	50.96

Calculations and simulations are fairly close.

2.3 Problem 1.C

First calculating the value of the internal capacitance of the inverter, then finding the effective capacitance because the load capacitance is now comparable(10fF):

$$C_{internal} = C_{1,Pmos} + C_{2,Nmos}$$

where

$$C_{1,Pmos} = C_{DBp} + C_{GDp} = C_j \cdot L_D \cdot W_p + C_{jsw}(2L_d + W_p) + 2C_{GDO} \cdot W_p$$

$$= (7.1 \cdot 10^{-4})(1.5\mu m)(3.6\mu m) + \tag{17}$$
$$(2.18 \cdot 10^{-10})(2(1.5\mu m) + (3.6\mu m)) + \tag{18}$$
$$2(2.28 \cdot 10^{-10})(3.6\mu m) \tag{19}$$

$$C_{1,Nmos} = C_{DBn} + C_{GDn} = C_j \cdot L_D \cdot W_n + C_{jsw}(2L_d + W_n) + 2C_{GDO} \cdot W_n$$

$$= (4.16 \cdot 10^{-4})(1.5\mu m)(1.8\mu m) + \tag{20}$$
$$(3.26 \cdot 10^{-10})(2(1.5\mu m) + (1.8\mu m)) + \tag{21}$$
$$2(1.93 \cdot 10^{-10})(1.8\mu m) \tag{22}$$

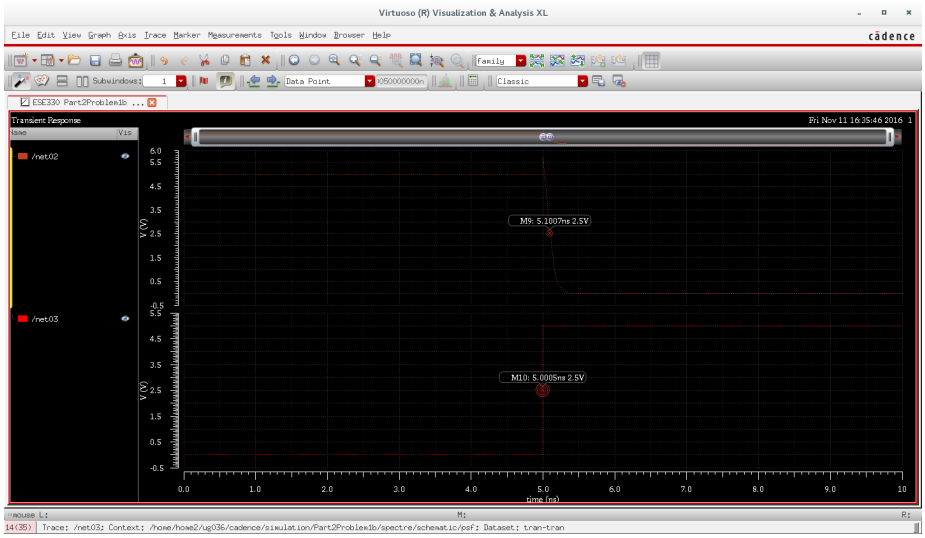
therefore;

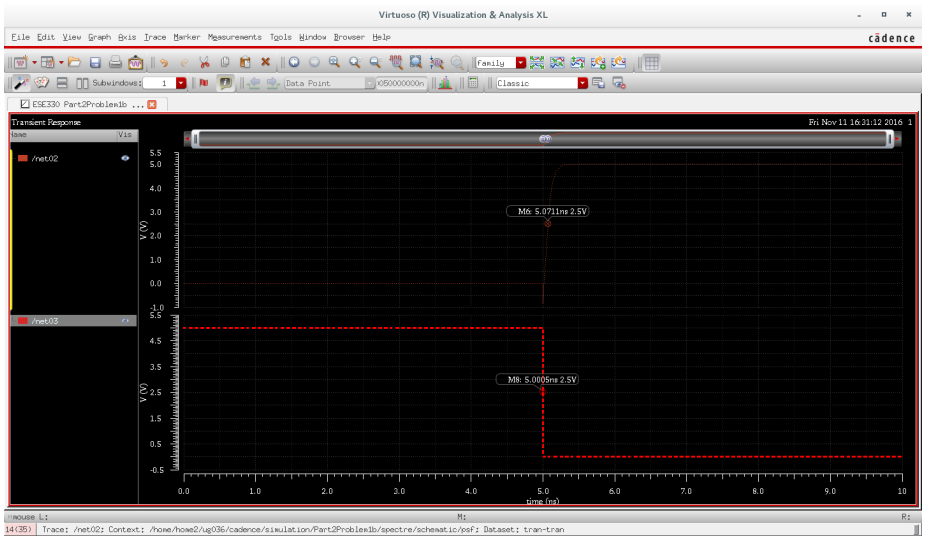
$$C_{internal} = 6.914 \cdot 10^{-15} + 3.2748 \cdot 10^{-15} = 10.189fF \tag{23}$$
$$C_{Leff} = C_{internal} + 10fF = 20.189fF \tag{24}$$

Using C_{Leff}(24) to find t_{pHL} and t_{pLH} for a load of 10fF:

$$t_{pLH} = .69R_pC_{Leff} \tag{25}$$
$$t_{pLH} = .69(5.19k)(20.189F) = 72.3pS \tag{26}$$
$$t_{pHL} = .69R_nC_{Leff} \tag{27}$$
$$t_{pHL} = .69(6.289k)(20.189F) = 87.61nS \tag{28}$$

Simulations using Cadence Virtuoso :





t_{pHL}=100.2ps and t_{pLH}=71ps (respectively)

Comparison(ps) with 10fF load:		
	t_{pHL}	t_{pLH}
Hand Calc.	87.61	72.3
Simulation	100.2	71

t_{pLH} are fairly close, however there is a difference of 13ps for t_{pHL}. t_{pLH} remains to have a shorter delay than t_{pHL} in both cases.

3 Problem 2

For chain of inverters the following expression is used to calculate the delay.

$$t_p = t_{p0}(1 + f/\gamma)$$

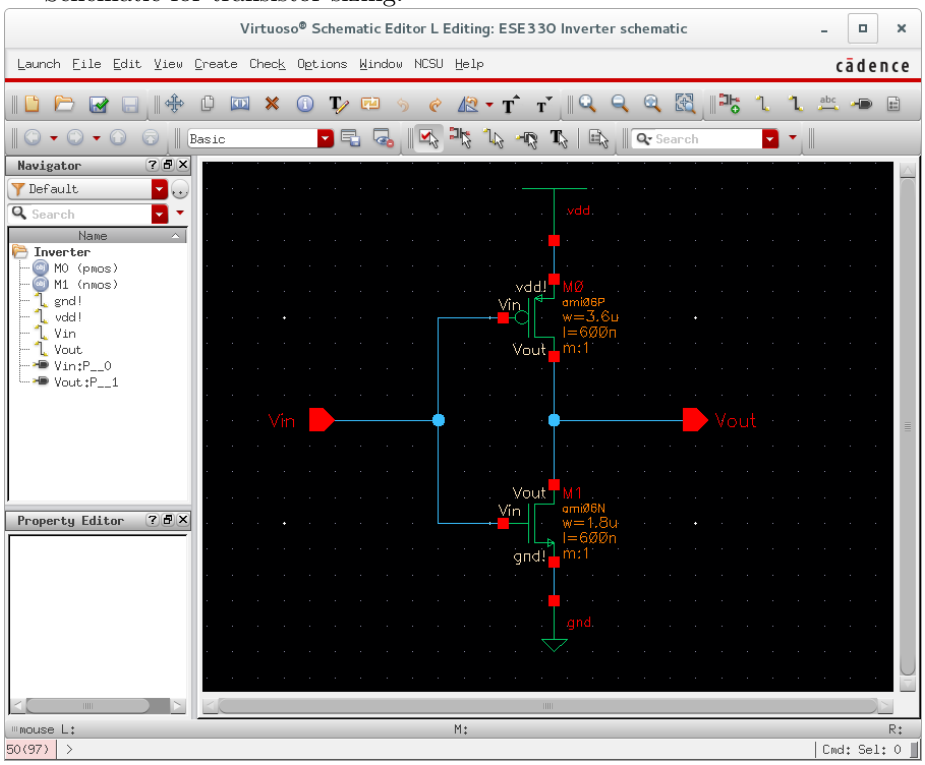
Where

- t_{p0} is the intrinsic delay
- f is fanout
- $\gamma = \frac{C_{intrinsic}}{C_{gate}}$, the ratio of input intrinsic to input gate capacitance

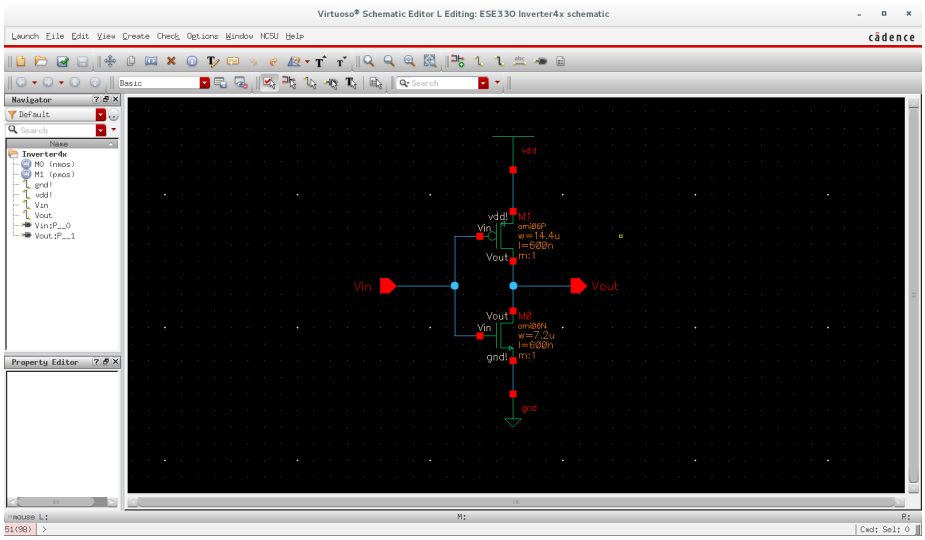
3.1 Problem 2.A

The propagation delay of the minimum sized inverter with a load of the minimum sized inverter and the propagation delay of the minimum sized inverter with a load of 4 times the minimum size can be used to help calculate t_{p0} and γ.

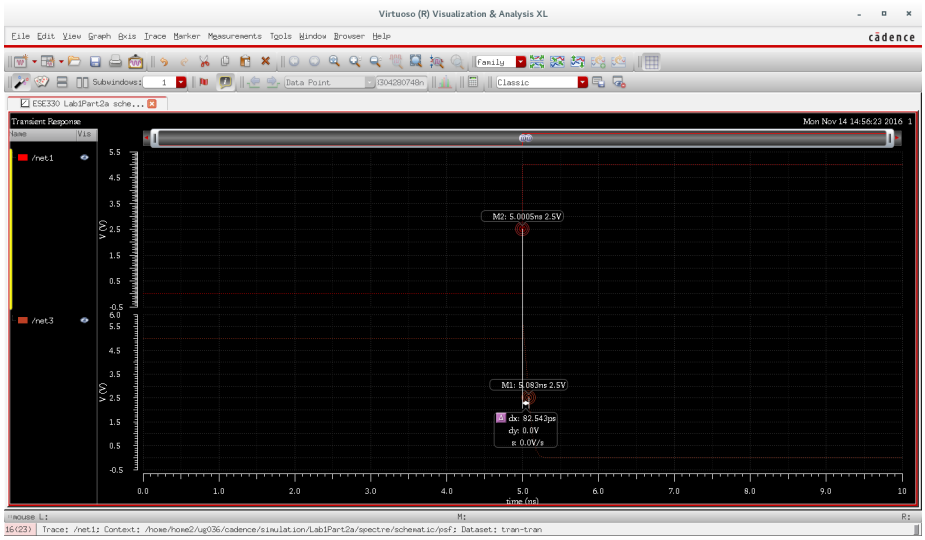
Schematic for transistor sizing:

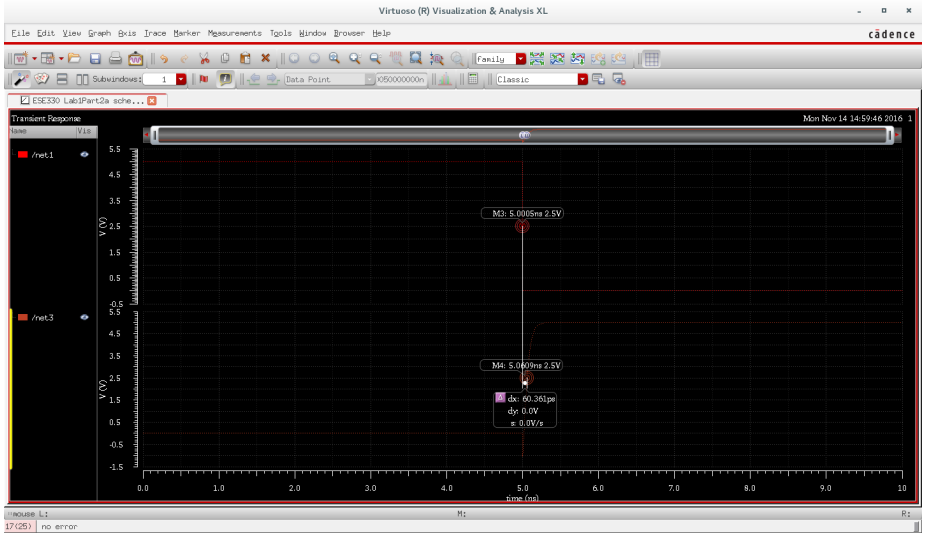


4x minimized; W_n= 7.2μ m , W_p= 14.4μ m

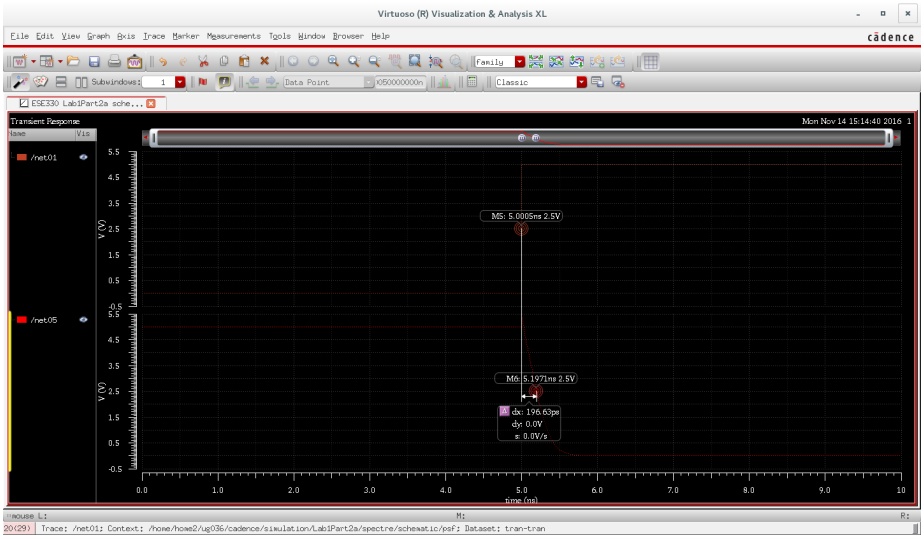

Virtuoso® Schematic Editor L Editing: ESE330 Inverter4x schematic
Launch File Edit View Create Check Options Window NCSU Help
cadence
Navigator
Property Editor
vdd
vdd!
M1
Vin
Vout
pmos
w=14.4u
l=600n
m:1
Vin
Vout
Vout
M0
Vin
nmos
w=7.2u
l=600n
m:1
gnd!
gnd

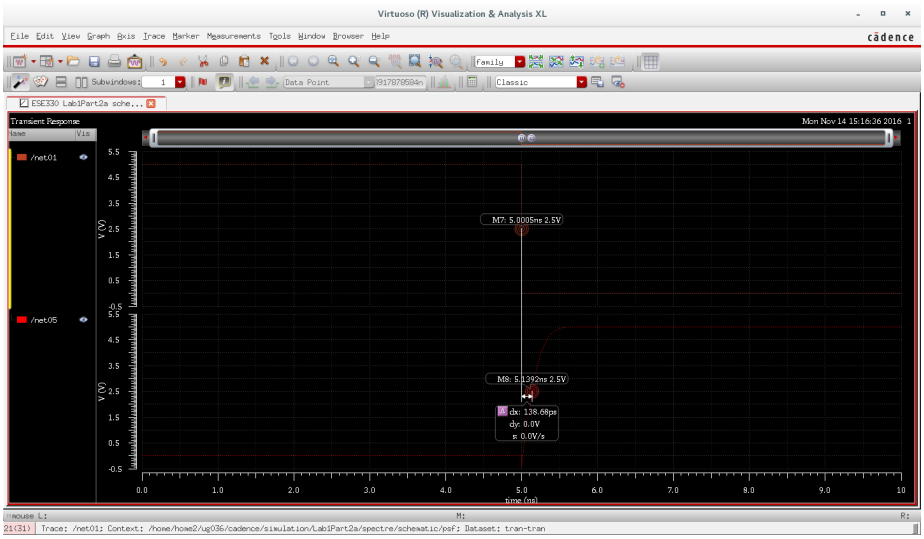
Timing simulation for 1:1 (minimum sized inverter with a load of the minimum sized inverter:





Timing simulation for 1:4 (minimum sized inverter with a load of 4 times the minimum size):





By taking the average, t_p can be defined as:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

Delay from simulations(ps)			
	t_{pHL}	t_{pLH}	t_p
1:1	82.54	60.361	71.452
1:4	196.93	138.68	167.805

Using these times, t_{p0} and γ can now be calculated:

$$71.452ps = t_{p0}(1 + \frac{1}{\gamma}) \tag{29}$$

$$167.805ps = t_{p0}(1 + \frac{4}{\gamma}) \tag{30}$$

$$\frac{71.452ps}{167.805ps} = \frac{t_{p0}(1 + \frac{1}{\gamma})}{t_{p0}(1 + \frac{4}{\gamma})} \tag{31}$$

$$.426 = \frac{1 + \frac{1}{\gamma}}{1 + \frac{4}{\gamma}} \tag{32}$$

$$.426(\gamma + 4) = \gamma + 1 \tag{33}$$

$$.7032 = .574\gamma \tag{34}$$

$$\gamma = 1.2251 \tag{35}$$

Plugging (35) into (29) to solve for t_{p0}:

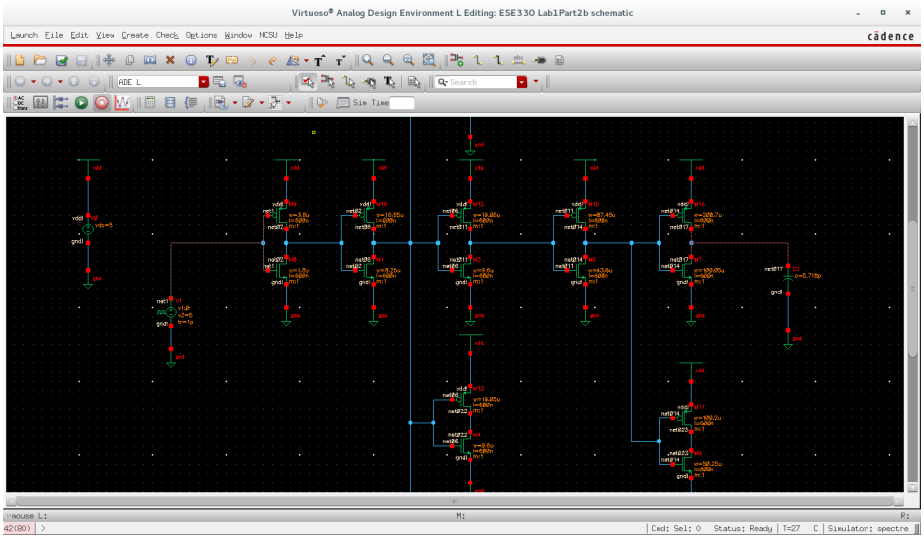
$$71.452ps = t_{p0}(1 + 1\frac{1}{1.2251}) \tag{36}$$

$$71.452ps = t_{p0}(1.816) \tag{37}$$

$$t_{p0} = 39.35ps \tag{38}$$

3.2 Problem 2.B

Using calculated t_{p0} and γ, the circuit below is optimized:



First determine the widths for each inverter. Given:

$$C_g = 2 \cdot C_o + LC_{ox}$$

where:

$$C_o = C_{GD0} = C_{GS0} = 1.93 \cdot 10^{-10} F/m.$$

$$L = L_S = L_D = 1.5\mu m and C_{ox} = 2.5 \cdot 10^{-3} F/m^2$$

Therefore:

$$C_g = 4.136 \frac{fF}{\mu m} \tag{39}$$

Using C_g (39) to find C_{inv}, where:

$$C_{inv} = 3W_{min}C_g = 3(1.8\mu m)(4.136\frac{fF}{\mu m}) = 22.3344fF \tag{40}$$

Next determine h for transistor width calculations,

$$h = \sqrt[n]{GBF}$$

where h=stage effort, N= number of stages, G = path logical effort, B= branching effort, and F= electrical effort.

$$N = 5 \tag{41}$$

$$G = 1 \cdot 1 \cdot 1 \cdot 1 \cdot 1 = 1 \tag{42}$$

$$B = 1 \cdot 4 \cdot 1 \cdot 2 \cdot 1 = 8 \tag{43}$$

$$F = \frac{256 C_{inv}}{C_{inv}} = 256 \tag{44}$$

$$h = \sqrt[N]{GBF} = \sqrt[5]{1 \cdot 8 \cdot 256} = 4.59 \tag{45}$$

Using h(45) and C_g (39) to find the optimized widths of each transistor at each stage:

$$C_5 = 1 \cdot 1 \cdot \frac{256(22.3344)}{4.59} = 1245.6fF \tag{46}$$

$$W_5 = \frac{1245.6}{3 \cdot C_g} = 100.3\mu m \tag{47}$$

$$W_{5n} = 100.3\mu m, W_{5p} = 200.6\mu m \tag{48}$$

$$C_4 = 2 \cdot 1 \cdot \frac{1245.6fF}{4.59} = 542.75fF \tag{49}$$

$$W_4 = \frac{542.75fF}{3 \cdot C_g} = 43.73\mu m \tag{50}$$

$$W_{4n} = 43.73\mu m, W_{4p} = 87.48\mu m \tag{51}$$

$$C_3 = 1 \cdot 1 \cdot \frac{542.75fF}{4.59} = 118.25fF \tag{52}$$

$$W_3 = \frac{118.25fF}{3 \cdot C_g} = 9.53\mu m \tag{53}$$

$$W_{3n} = 9.53\mu m, W_{3p} = 19.06\mu m \tag{54}$$

$$C_2 = 4 \cdot 1 \cdot \frac{118.25fF}{4.59} = 103.05fF \tag{55}$$

$$W_2 = \frac{103.05fF}{3 \cdot C_g} = 8.305\mu m \tag{56}$$

$$W_{2n} = 8.305\mu m, W_{2p} = 16.61\mu m \tag{57}$$

$$C_1 = 1 \cdot 1 \cdot \frac{103.05fF}{4.59} = 22.45fF \tag{58}$$

$$W_1 = \frac{22.45fF}{3 \cdot C_g} = 1.8\mu m \tag{59}$$

$$W_{1n} = 1.8\mu m, W_{1p} = 3.6\mu m \tag{60}$$

Given:

$$D = \frac{t_p}{t_{p0}} = \sum_{j=1}^{N} P_j + \frac{N \sqrt[N]{H}}{\gamma}$$

Using N (41), h(45), γ (35), t_{p0} (38) to find D(delay).

$$D = \frac{t_p}{39.35ps} = (1+1+1+1+1+1) + \frac{5 \cdot h}{\gamma} = 5 + \frac{5 \cdot 4.59}{1.2251} \tag{61}$$

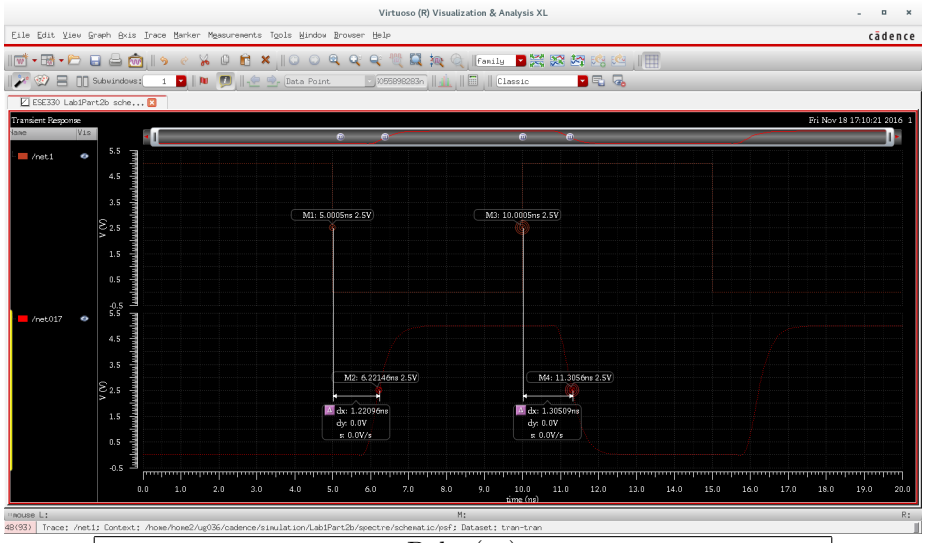
$$D = \frac{t_p}{39.35ps} = 23.733 \tag{62}$$

With D(62) normalized to t_{p0}, to get t_p:

$$t_p = D \cdot 39.35ps = 23.733 \cdot 39.35ps = .934ns \tag{63}$$

Using calculated widths (48),(51),(54),(57),and (60) construct the circuit as seen under problem 2.B. C_L=256 $\cdot$ C_{in} (C_{in} is the input capacitance of the minimum sized inverter); C_L= 5.718pF.

Simulation based on calculated parameters:



Delay(ns)			
	t_{pHL}	t_{pLH}	t_p
Simulation	1.305	1.221	1.263
Calculated	N/A	N/A	.934

There is a .329ns difference, nearly a 35.2 % error. One suspected reason for such huge error can be because of virtuoso forced rounding of transistor widths. It did not take the exact widths as calculated (48),(51),(54),(57),and (60), but to the snapped to the nearest 5^{th} hundredths.