Vitor Finotti Ferreira

Curriculum Vitae

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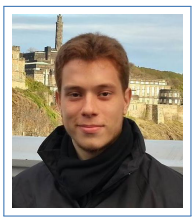

Education

2017 — **MSc. Electrical Engineering**,
Universidade de São Paulo, São Paulo, Brazil.
Computer Engineering, focused on convolutional neural networks on FPGA's.

2014 — **Electronics & Electrical Engineering (1 year)**,
University of Glasgow, Glasgow, United Kingdom.
Brazilian government fellowship "Ciência sem Fronteiras".

2010 – 2015 — **BSc. Electrical Engineering**,
Universidade Federal de São Carlos (UFSCar), São Carlos, Brazil.
Electronics & Control.

Experience

2016 — **Researcher**,
Center for Scientific Computing, Universidade Estadual Paulista (Unesp), São Paulo, Brazil.
Development of back-end electronics for the Phase-2 tracker upgrade, focusing on the Data, Timing and Control (DTC) cards, interfacing the tracker sensor hybrids to the DAQ, trigger and timing systems.
Main Duties:

- HDL development for Xilinx FPGA's
- Perform hardware tests, evaluation and debugging
- Planning and supervision of undergradate research projects
- Technical contributions to CMS tracker upgrade meetings

2016

Visiting Engineer (5 months),
Fermi National Accelerator Laboratory, Batavia (IL), USA.
Development of a real-time particle identification system (trigger) for the future central silicon detector of the CMS experiment at CERN.
Main Duties:
- Implementation of a backplane high-speed full mesh communication at an ATCA crate using Aurora 64b66b protocol between Virtex-7 FPGAs
- Calibration of MGT transceivers, seeking the best combination among various configurations of emphasis and equalization parameters using Python scripts
- Diagnostic tests on ATCA blades

2015
2016

Hardware Engineering Intern,
Centro Nacional de Pesquisa em Energia e Materiais (CNPEM), Campinas, Brazil.
Hardware engineering intern at the Beam Diagnostics group of the Brazilian Synchrotron Light Laboratory
Main Duties:
- Simulation of signal processing algorithms to determine the position of electron beam
- Implementation of wishbone stream protocol to standardize the communication between VHDL modules with different inputs, outputs and clock domains
- Planning, implementation and execution of transmission and reception tests of trigger signals in AMC boards in a MicroTCA crate

Languages

Portuguese	**Fluent**	*Mother Tongue*
English	**Fluent**	*Daily practice, most of the work is performed in English*
Spanish	**Intermetiate**	*Took classes during High School*

Skills

Languages
- C, Python, Matlab, VHDL, Git

Version Control
- Git, SVN

FPGA
- Xilinx Vivado, Modelsim, Hdlmake

Deep Learning
- CNNs, MLPs, Keras, Scrapy

Developed Projects

Autotuning system for Xilinx MGTs.
- Automatic tuning of emphasis and equalization of high-speed serial links between two Xilinx FPGA.

Biological signals recovery using lock-in amplifiers.

- Recovering of biological signals in noisy environments. In order to accomplish the recovery, a lock-in amplifier was designed, simulated and assembled. The simulation took place in GNU Octave environment, and the final printed circuit board for assembly was generated with the aid of KiCAD software.

Optical pulse meter using an Mbed microcontroller.

- Design of a device for measuring the heart rate using an Mbed microcontroller. The signal was captured from a finger and processed by the microcontroller, which displayed the heart beat waveform on a LCD screen along with the estimated heart rate.

Development of a management system for a vehicular regenerative breaking process.

- Development and simulation on Simulink environment of a management system to control the kinetic/electrical energy conversion in a vehicular breaking process.