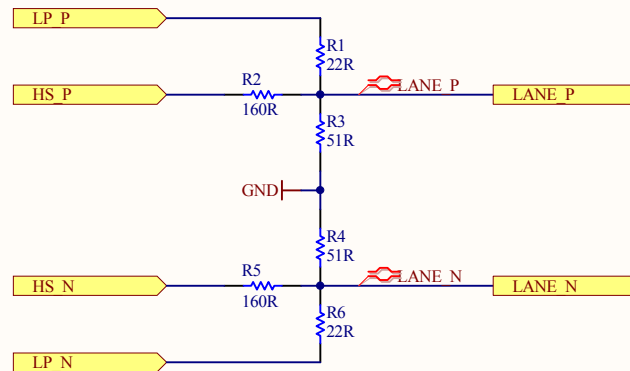


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Title		
DDR SDRAM		
Size	Number	Revision
A4		
Date:	2014-08-15	Sheet of
File:	C:\pcb\hdmi-dsi-shield\ddr_sdram.SchDoc	Drawn By:

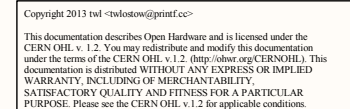
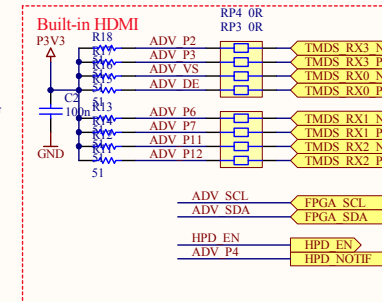
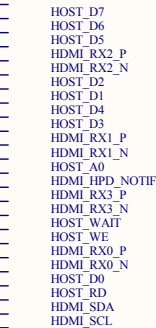
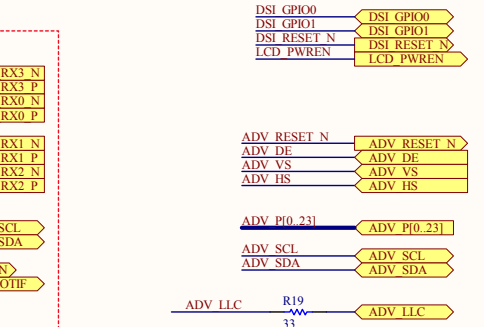
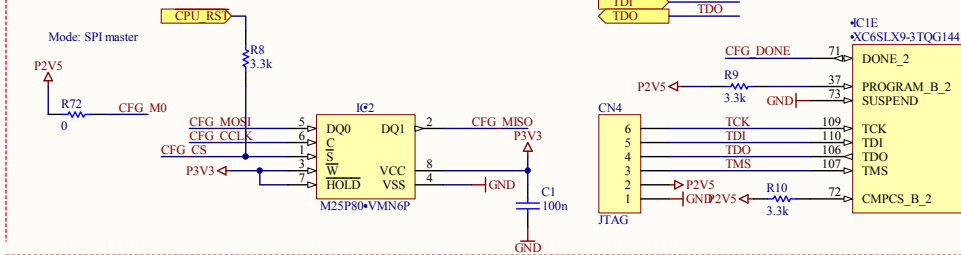
Not matched, place as close as possible to the FPGA pins



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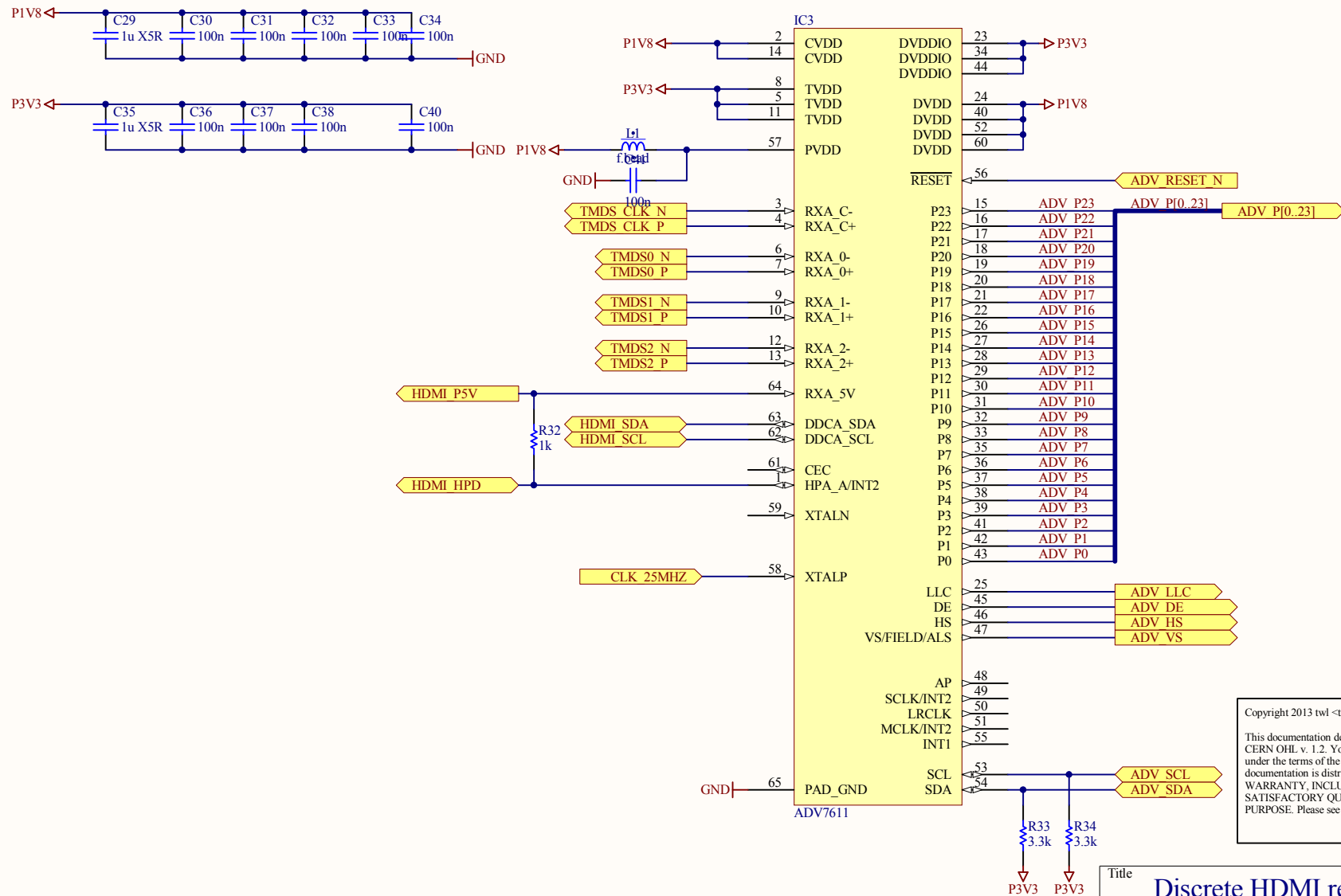
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Title		
SSTL/LVTTL to DSI level adapter		
Size	Number	Revision
A4		
Date:	2014-08-15	Sheet of
File:	C:\pcb\...\dsi_level_adapter.SchDoc	Drawn By:



Title	Main FPGA
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Size A3	Number	Revision
Date:	2014-08-15	Sheet of
File:	C:\pcb\hdm1-dsi-shield\figa.SchDoc	Drawn By:



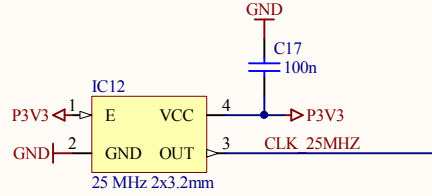
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Title		
Discrete HDMI receiver (ADV7611)		
Size	Number	Revision
A4		
Date:	2014-08-15	Sheet of
File:	C:\pcb\hdm receiver.SchDoc	Drawn By:

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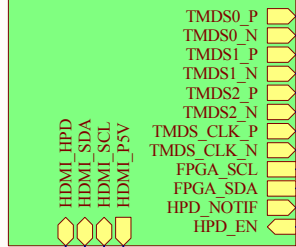
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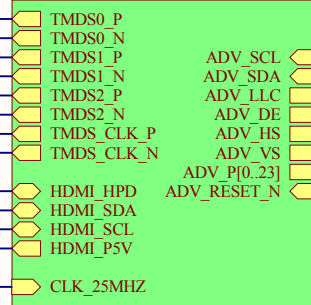
U_power_supply
power_supply.SchDoc



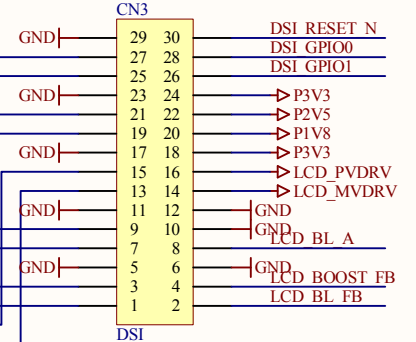
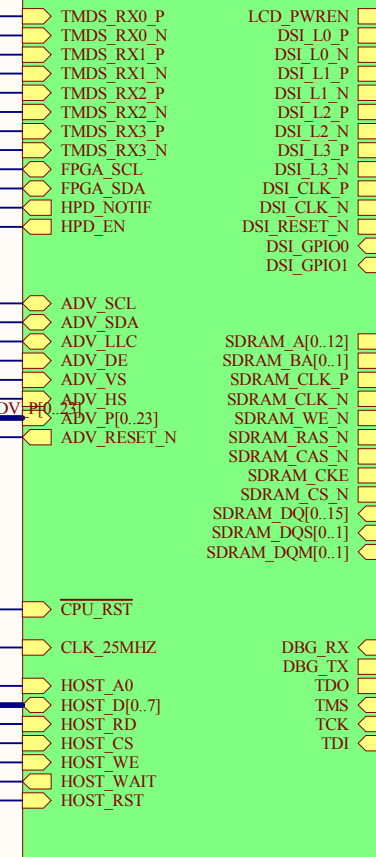
U_HDMI_IN
hdmi_in.SchDoc



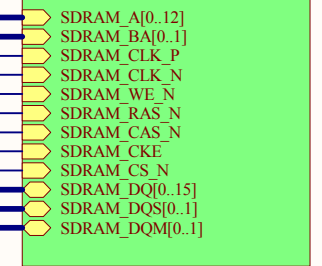
U_hdmi_receiver
hdmi_receiver.SchDoc



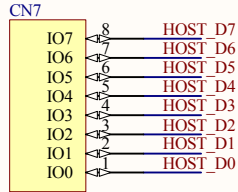
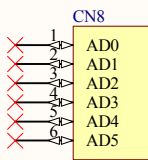
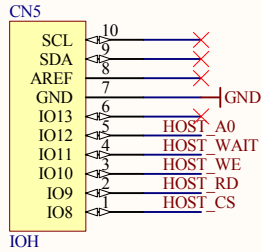
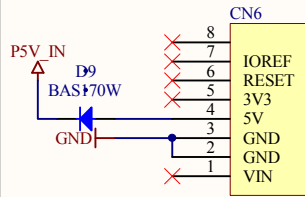
U_fpga
fpga.SchDoc



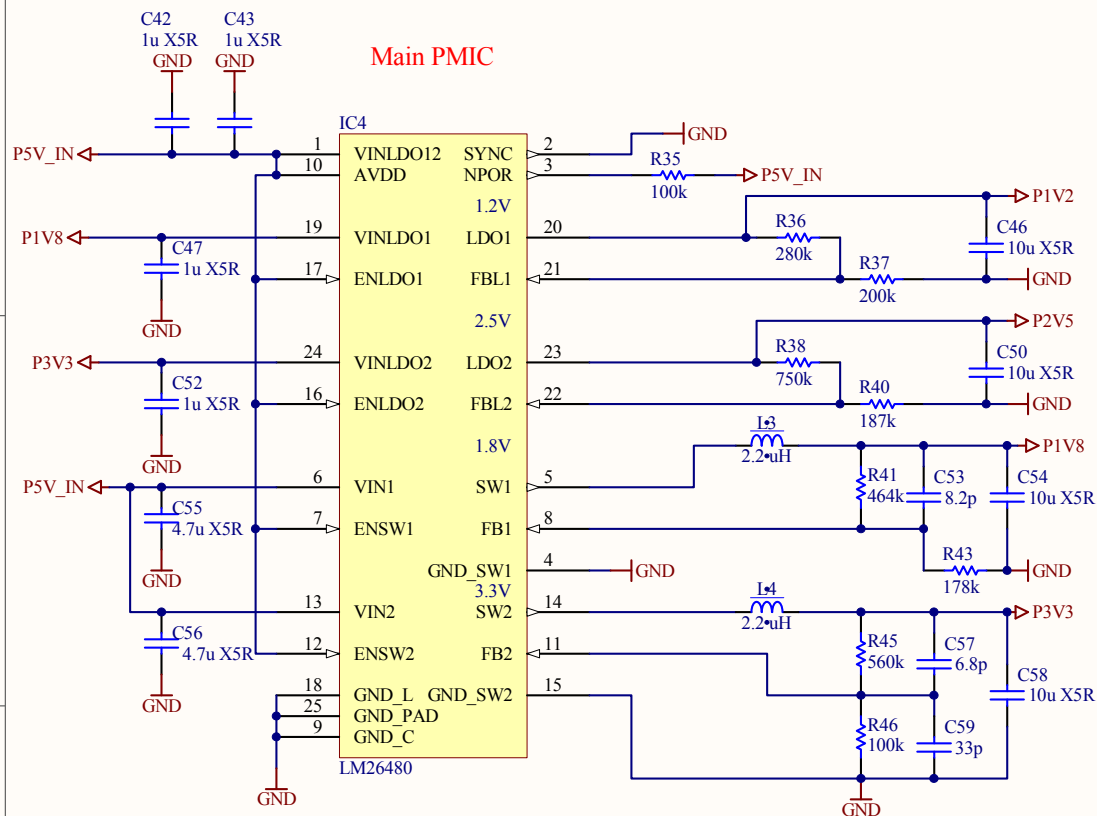
U_SDRAM
ddr_sdram.SchDoc



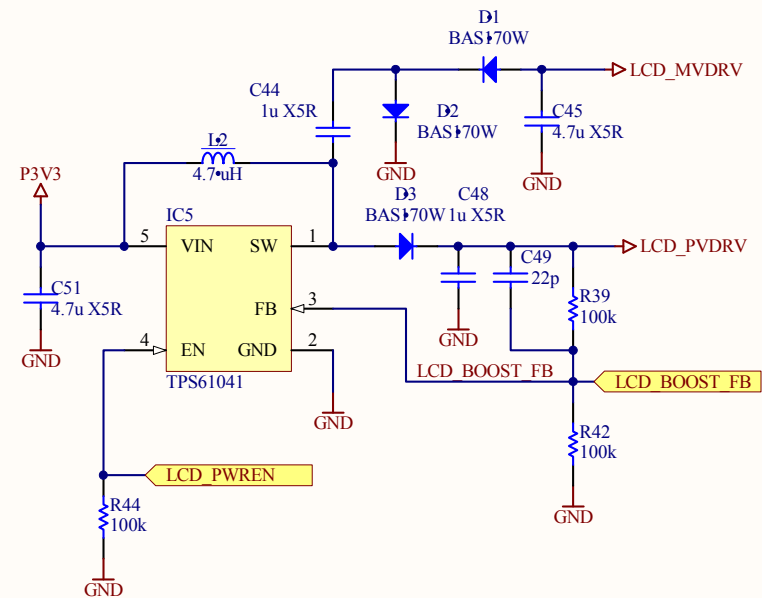
U_usb_uart_jtag
usb_uart_jtag.SchDoc



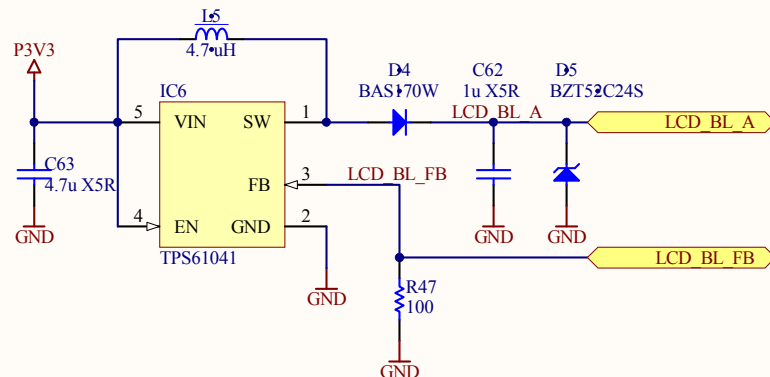
Title		
HDMI - DSI interface - top level		
Size	Number	Revision
A4		
Date:	2014-08-15	Sheet of
File:	C:\pcb\...\hdmi-dsi-top.SchDoc	Drawn By:



LCD Vdrv boost converter (default +- 2.5V)



Backlight boost converter



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Title		
Power supply		
Size	Number	Revision
A		
Date:	2014-08-15	Sheet of
File:	C:\pcb\...\power_supply.SchDoc	Drawn By:

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