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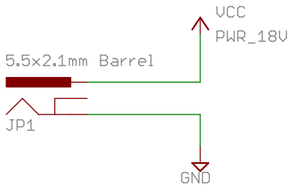
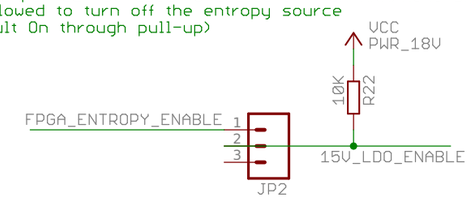
Main power input
18V DC

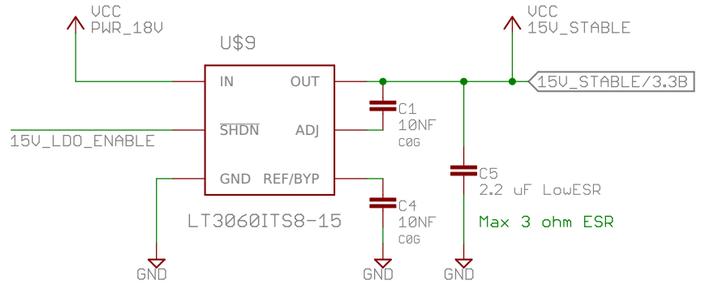


To mitigate component ageing in the avalanche noise circuit, this jumper can be used to decide if FPGA/ARM/None should be allowed to turn off the entropy source (default On through pull-up)

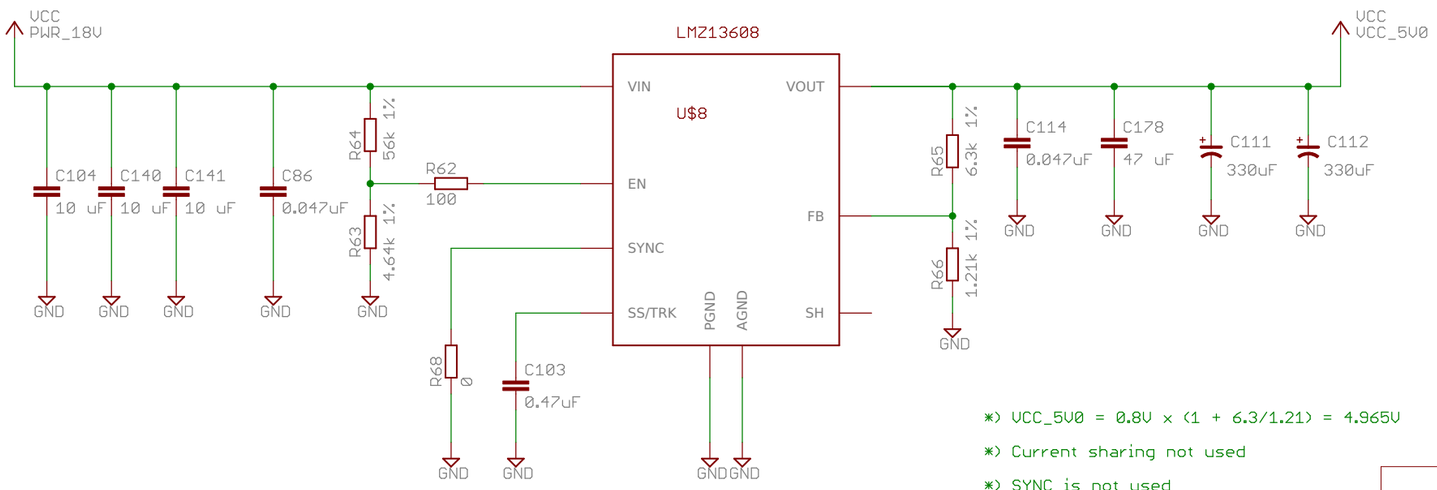


XXX add circuitry to allow FPGA/ARM to control sinking of the 18V from the 10K pull-up on pin 2.

15V LDO powered from external 18V and supplying stable 15V to noise source



*) Intermediate Regulator: 18V -> 5V



*) VCC_5V0 = 0.8V x (1 + 6.3/1.21) = 4.965V

*) Current sharing not used

*) SYNC is not used

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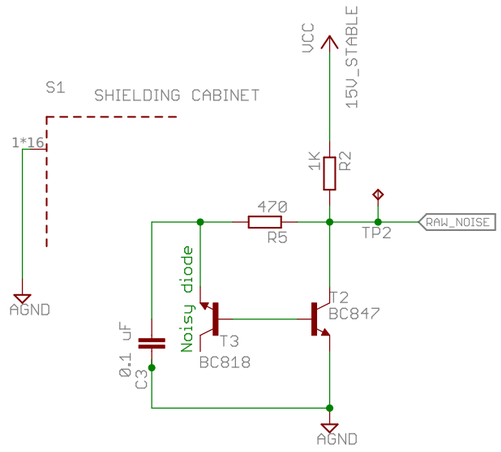
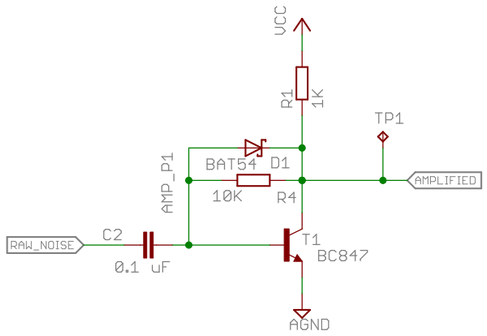
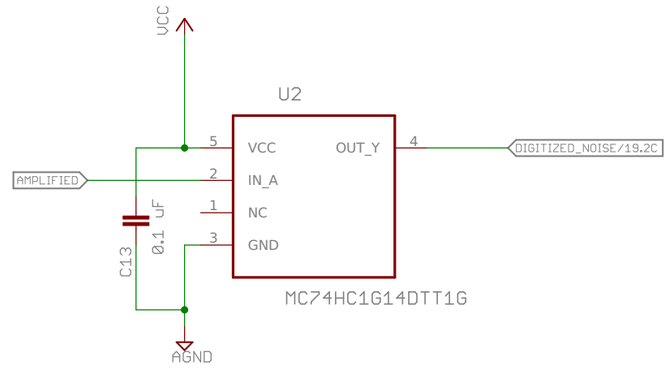
Noise generator



Amplifier



Digitizer



AGND is connected to GND on the board using polygons
(found no other good way) - not visible in schematics.

Add optocoupler as per Jacob's suggestion on tech@ 2015-07-24?

The suggestion is to add a fast optocoupler to really isolate AGND from GND.

As this appears to require a bigger digitizer, we are reluctant to add that
for the Alpha.

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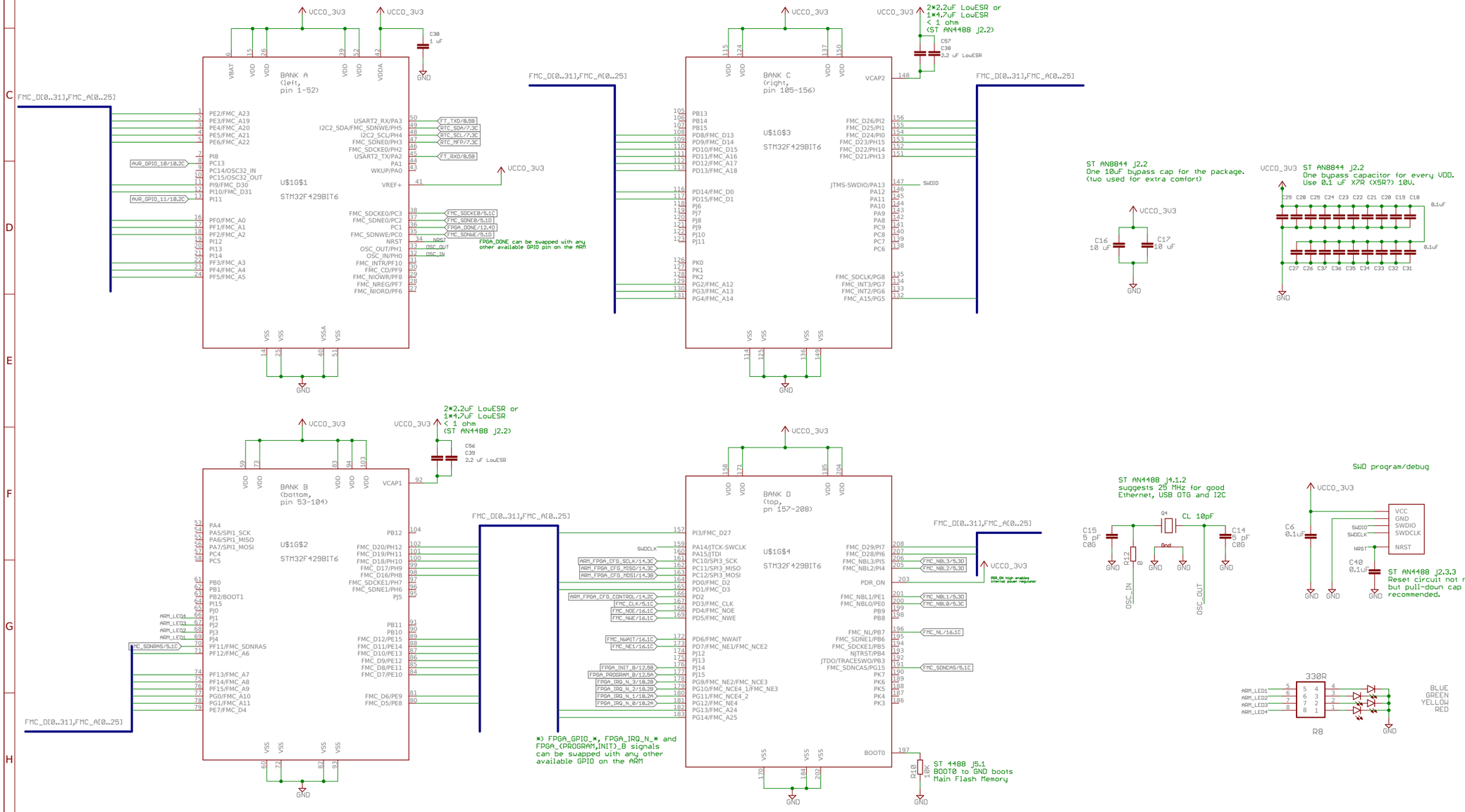

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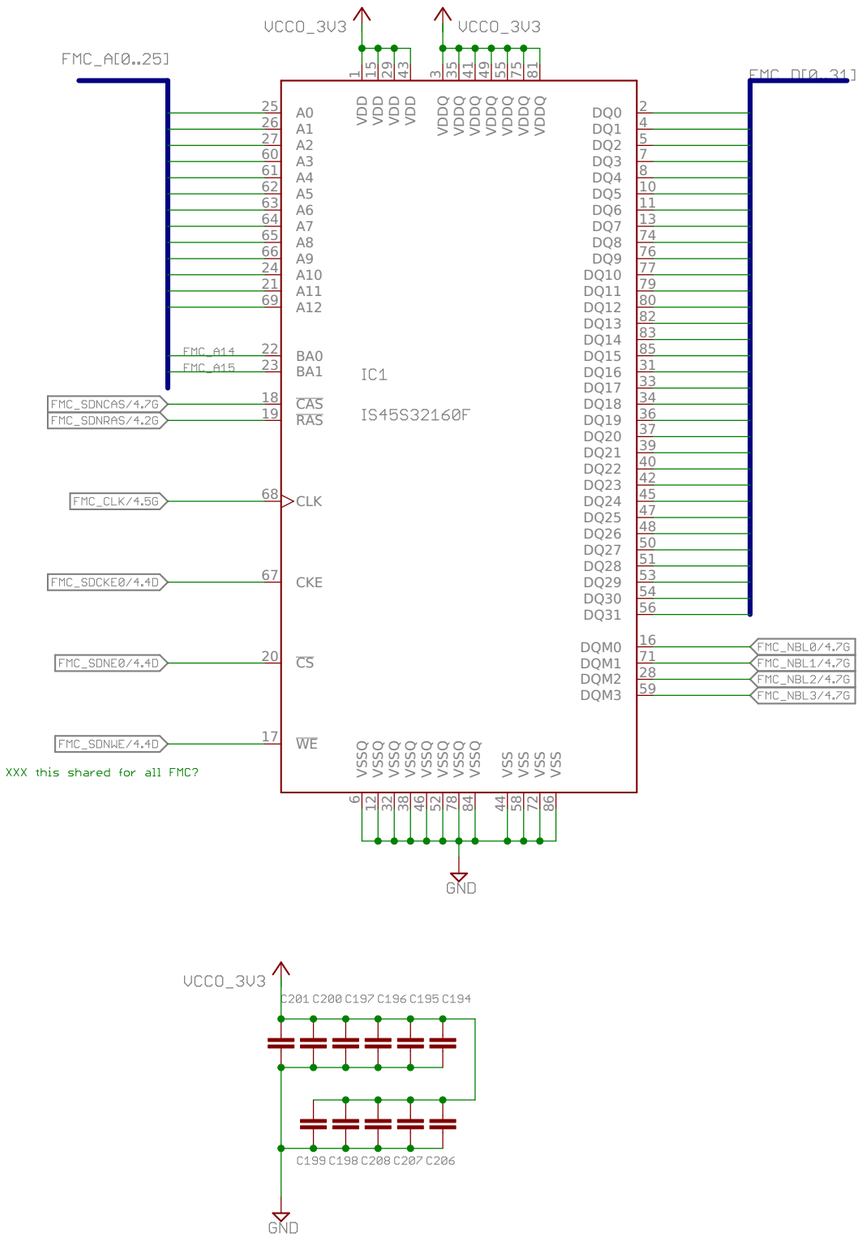

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Keystore memory (>= 8 MByte) goes here

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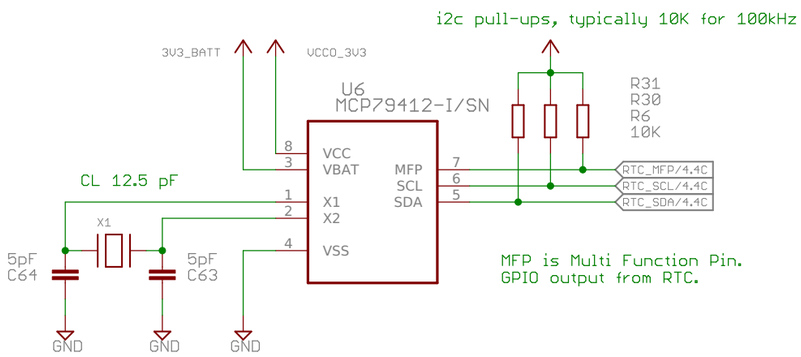
Real Time Clock



MFP is Multi Function Pin.
GPIO output from RTC.

Micro SD card goes here

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Do we need more speed?

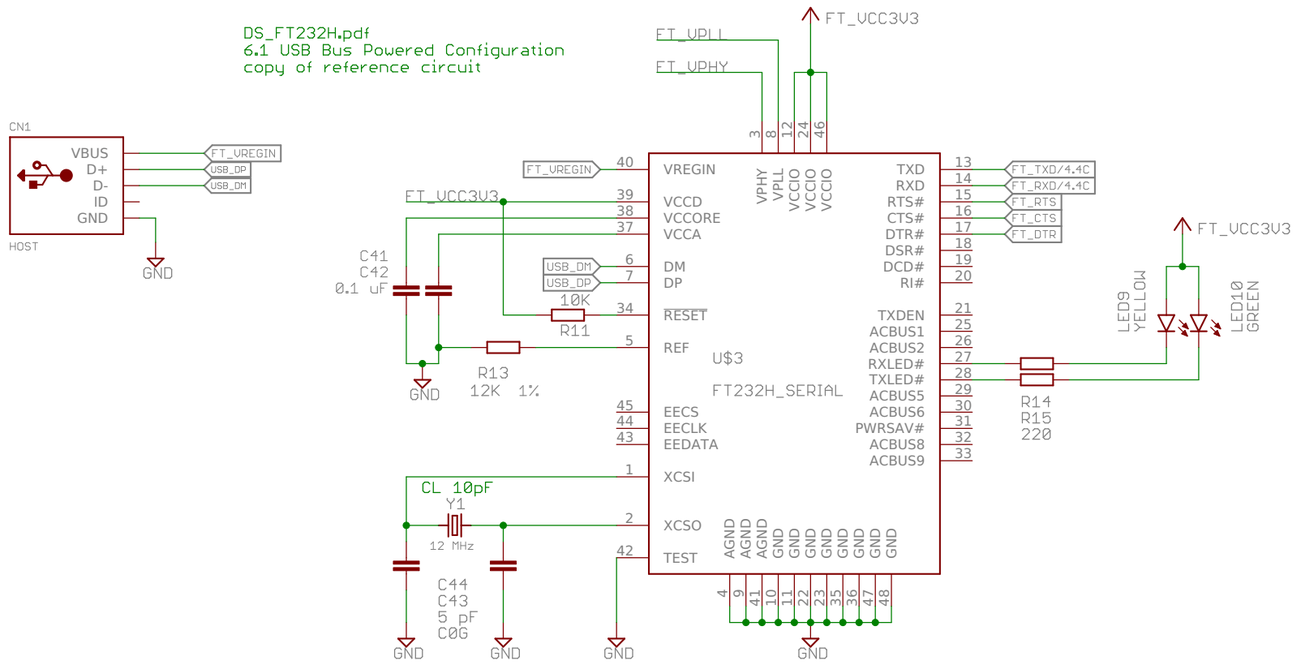
Joachim expressed that we might need a faster interconnect to the Alpha than the 12 Mbaud the FT232H can deliver in UART mode (in an e-mail to tech@ 2015-08-18).

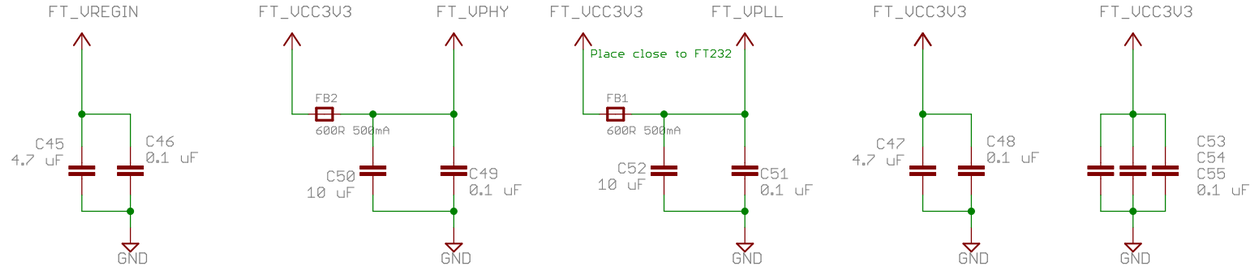
An alternative is to connect all of the ADBUS (and more) to the ARM, and use one of the faster modes this chip supports (fastest: synchronous FT245 parallel FIFO at 40 Mbyte/s).

Enabling the faster modes requires the addition of an EEPROM that can be configured from the host (yuck) though.

This requirement also applies to using our own USB VID/PID.

DS_FT232H.pdf
6.1 USB Bus Powered Configuration
copy of reference circuit





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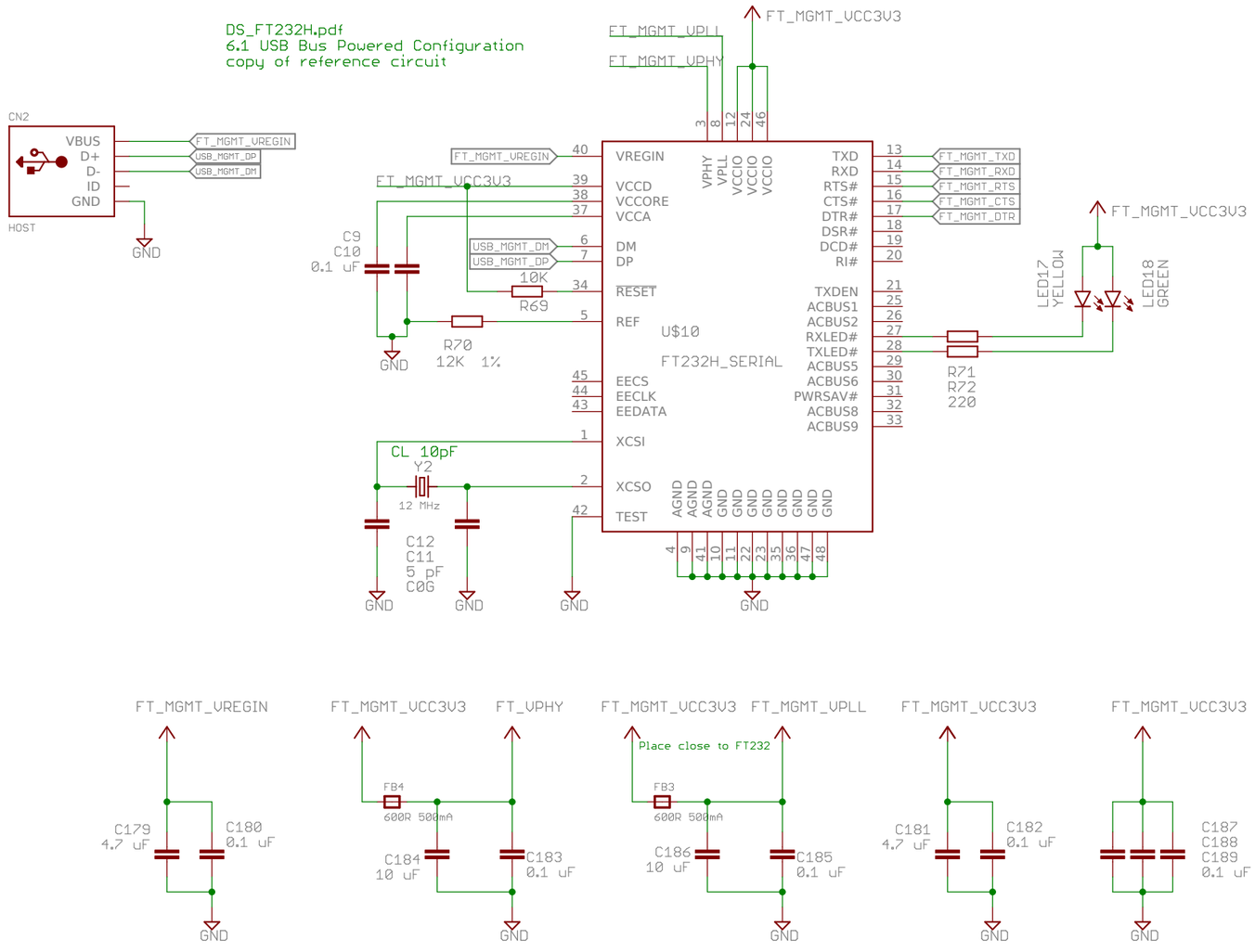

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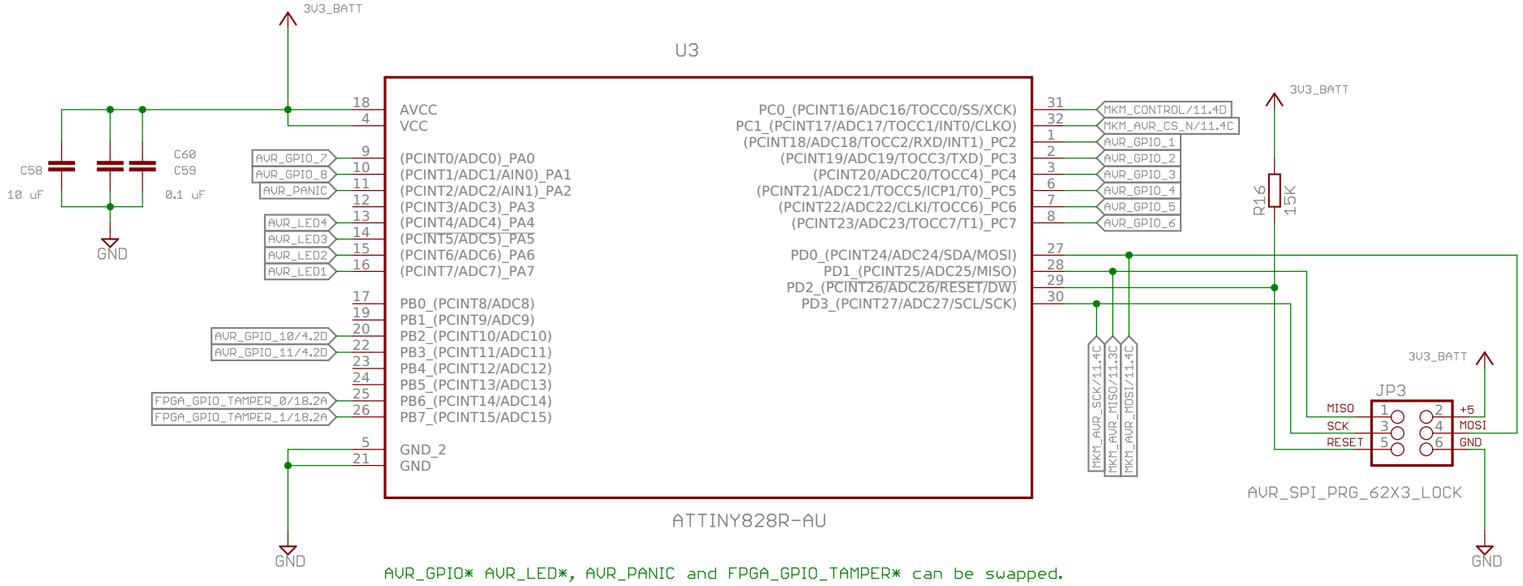
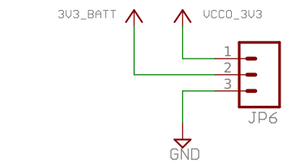
AVR Tiny Tamper Detect MCU

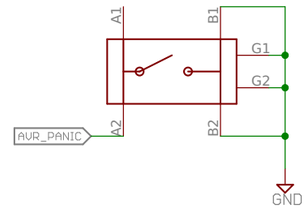


AVR_GPIO* AVR_LED*, AVR_PANIC and FPGA_GPIO_TAMPER* can be swapped.

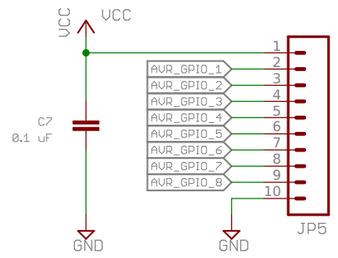
Place a jumper between pins 1-2
to "emulate" having a battery present.

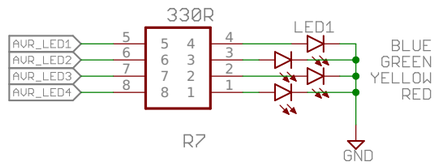


Panic button



Expansion GPIO





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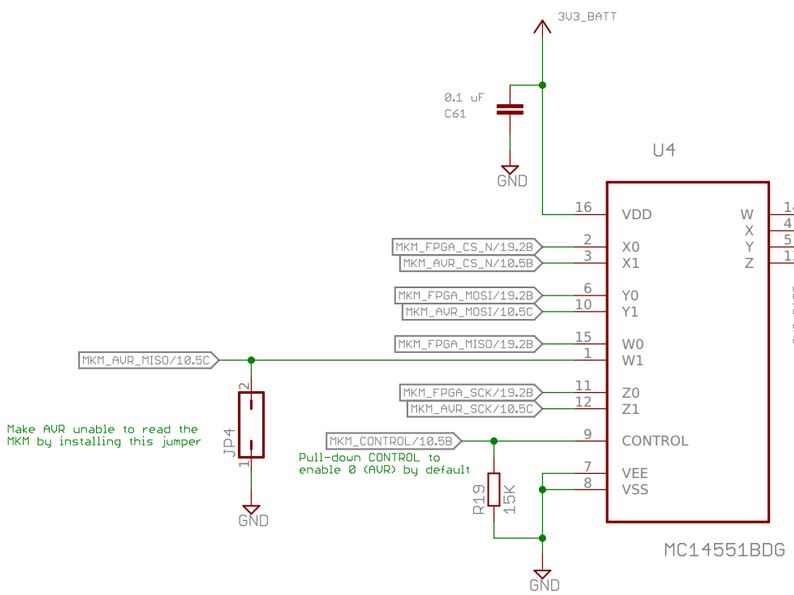
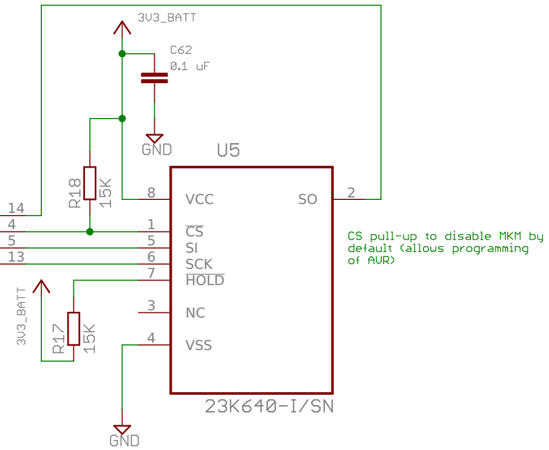
XXX test this circuit

Analog switch



Master Key Memory



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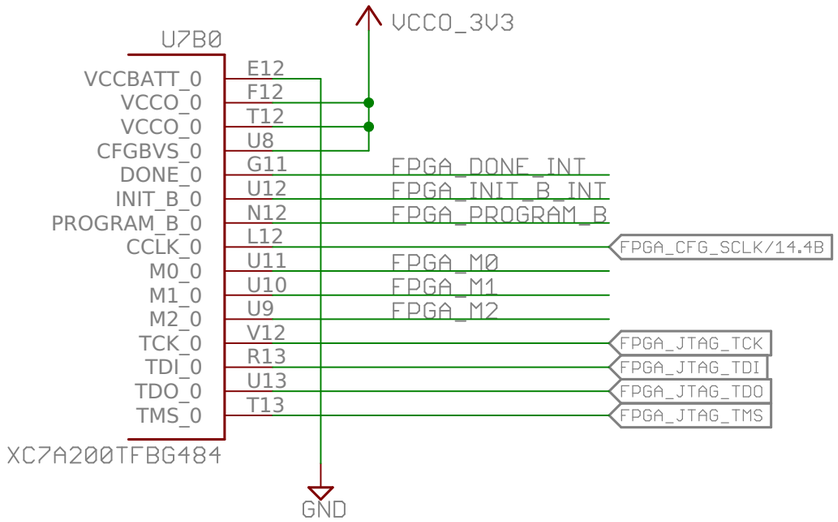
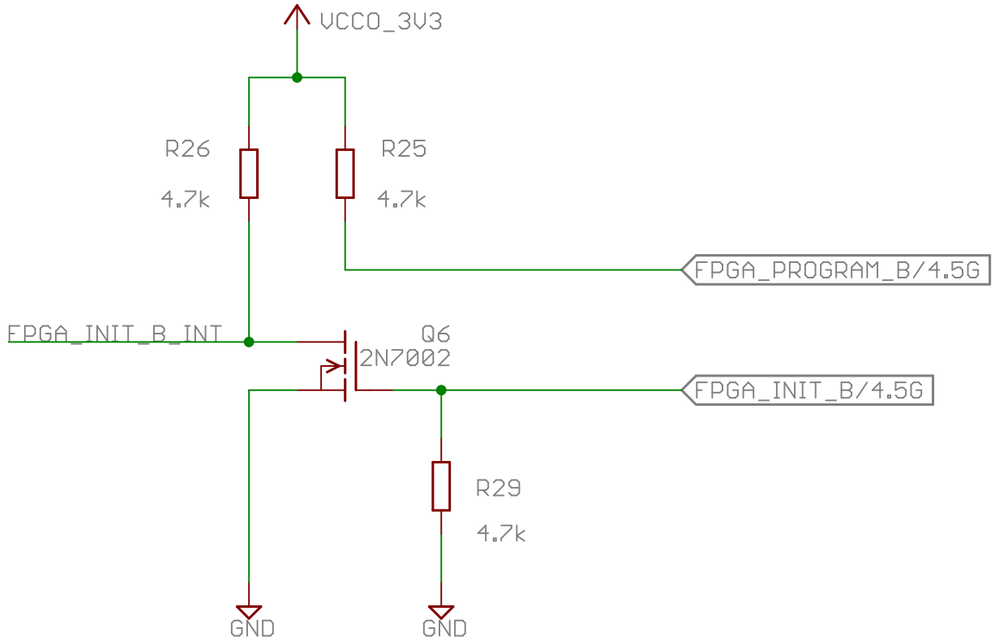
*) Configuration Interface



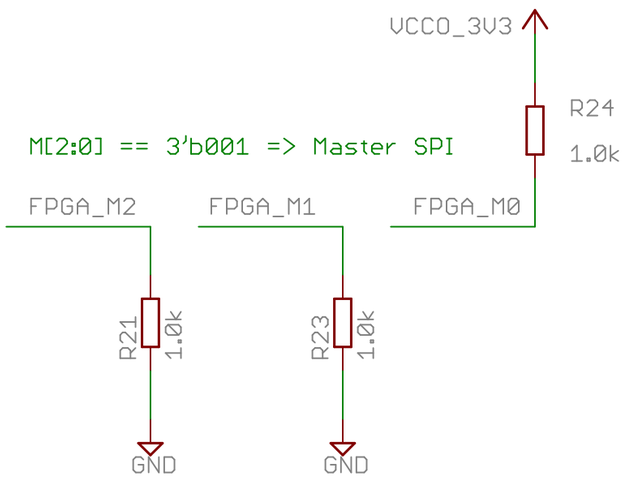


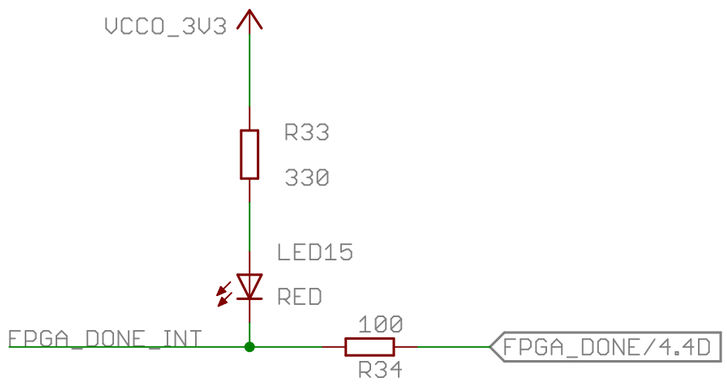
*) Since VCCO is 3.3V, CFGBVS must be tied High.

*) Battery is not used

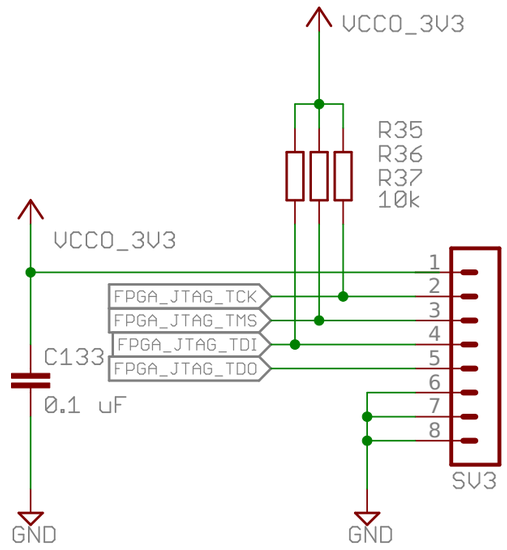
*) PROG_B is dedicated input -- can be driven by STM32 directly

*) INIT_B is bi-directional open-drain, must be driven with MOSFET to ground





*) "Not DONE" LED, should be of red color



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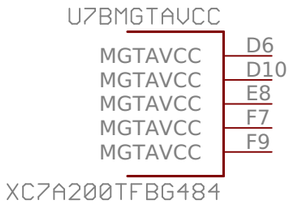
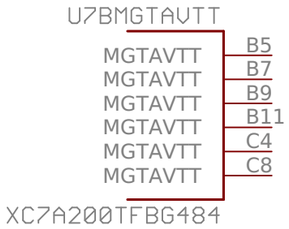
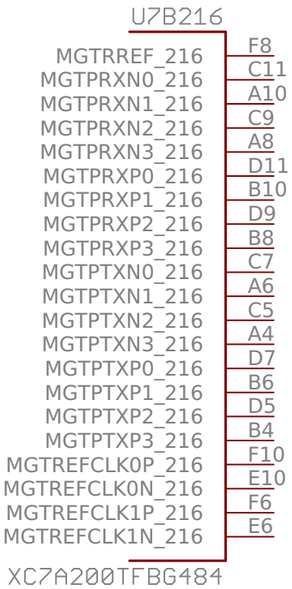
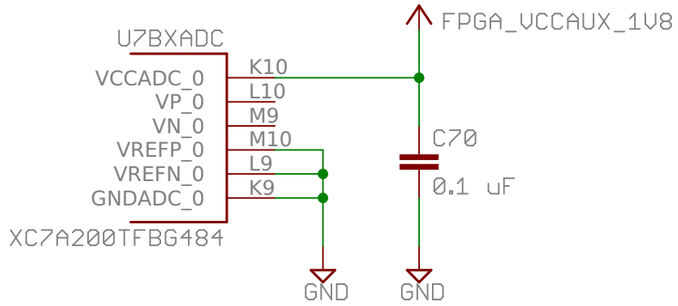
*) Transceivers [NOT USED]



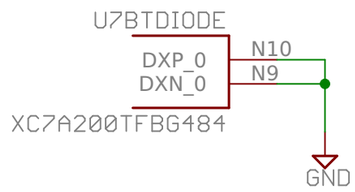




*) XADC [NOT USED]



*) Temperature Sensor [NOT USED]



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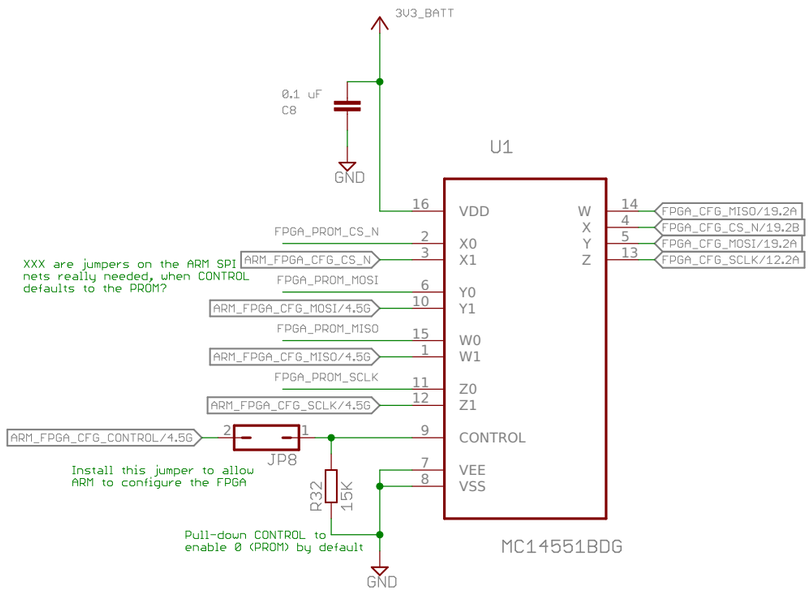
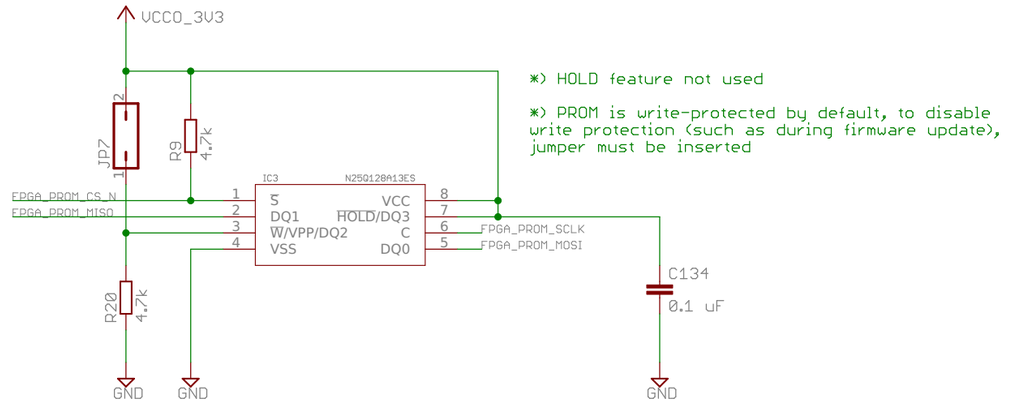
Analog switch to boot FPGA from config memory, or from ARM

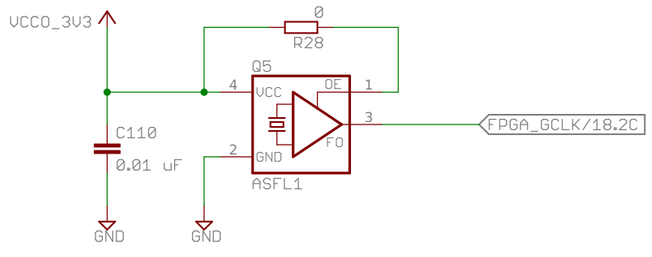
XXX this probably needs more HW support. FPGA is SPI master when booting from config memory,
but should be SPI slave when being fed a bitstream from the ARM.



FPGA config memory



FPGA clock



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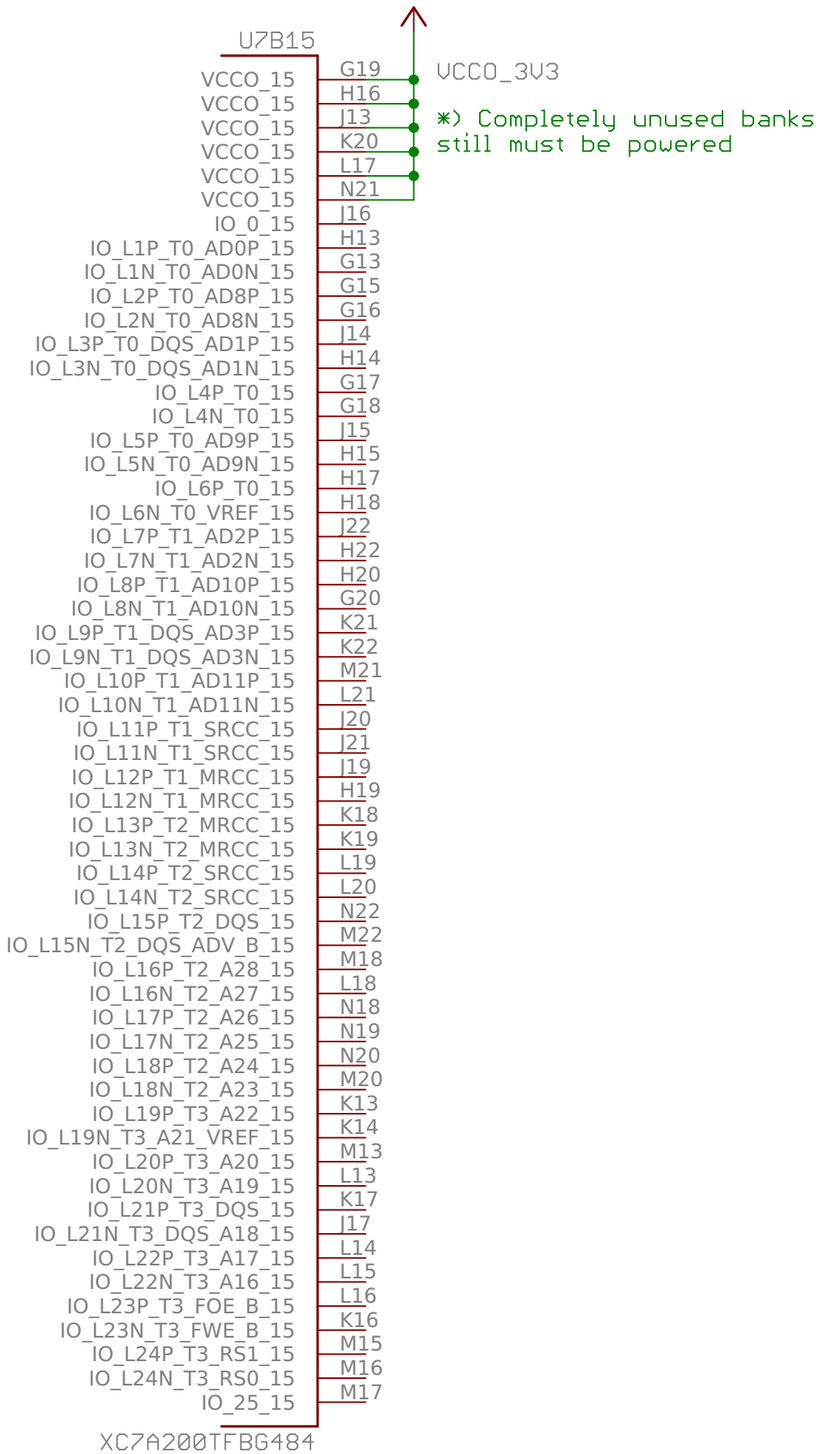
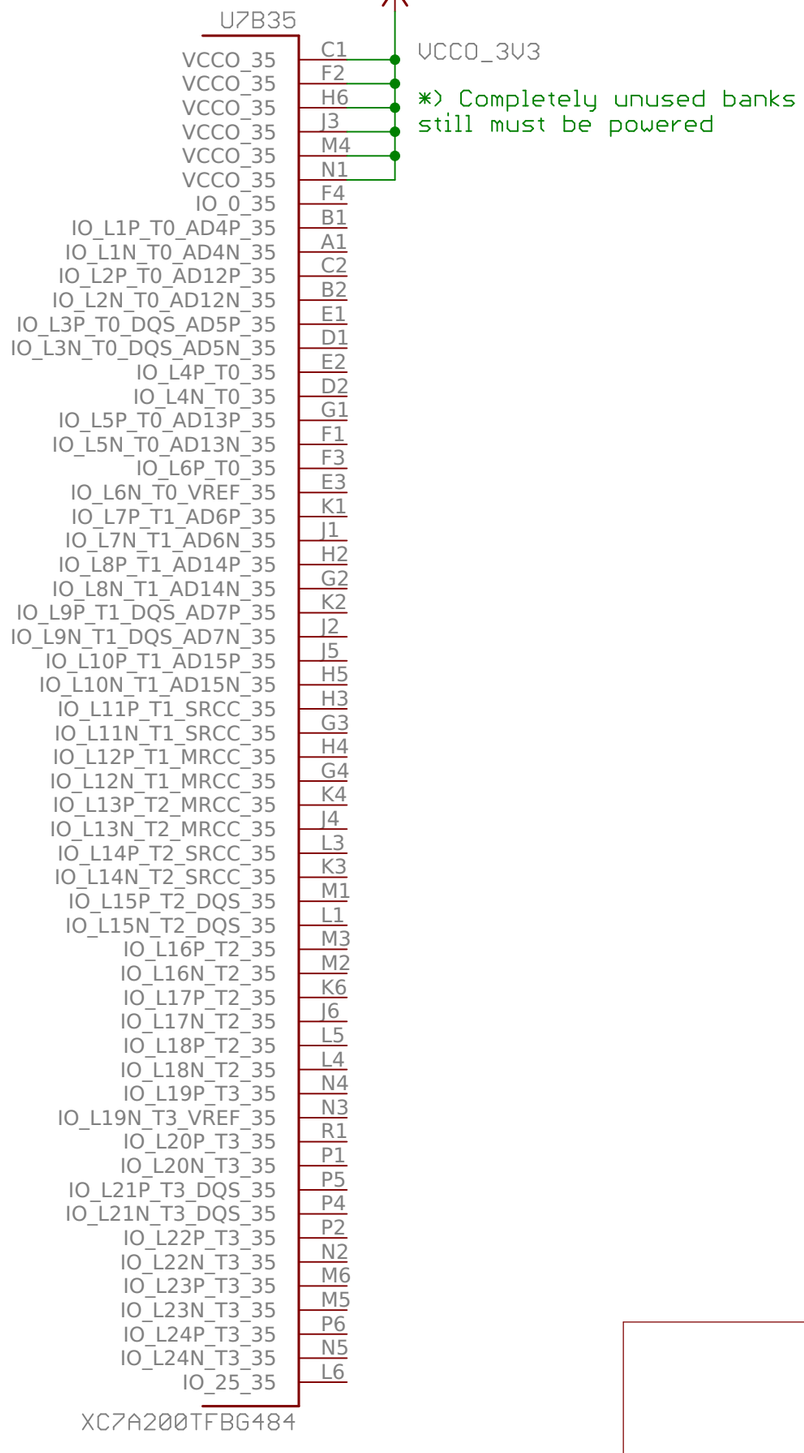
Drawing:	www.microbuilder.eu

*) Middle Right Bank



*) Upper Left Bank



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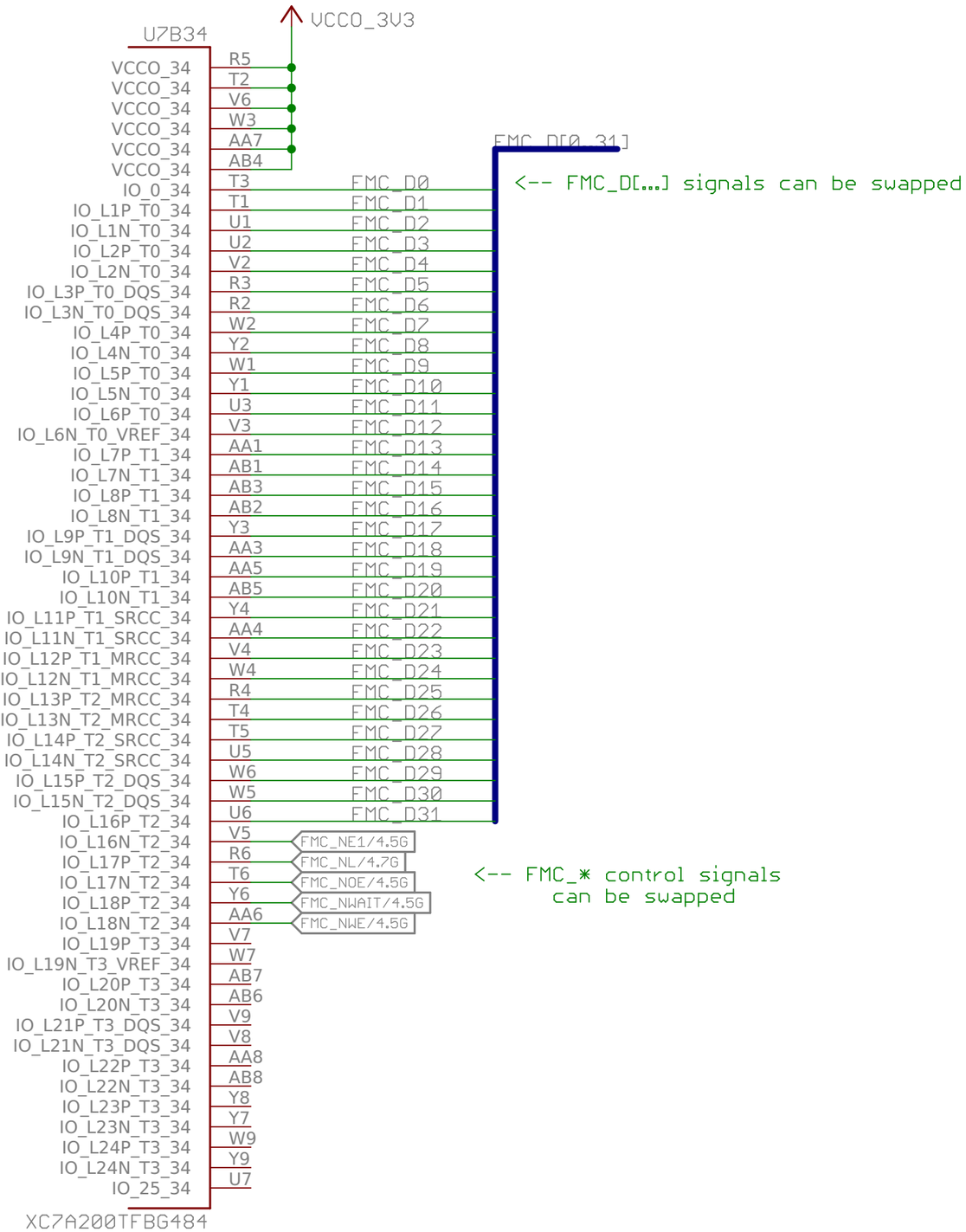
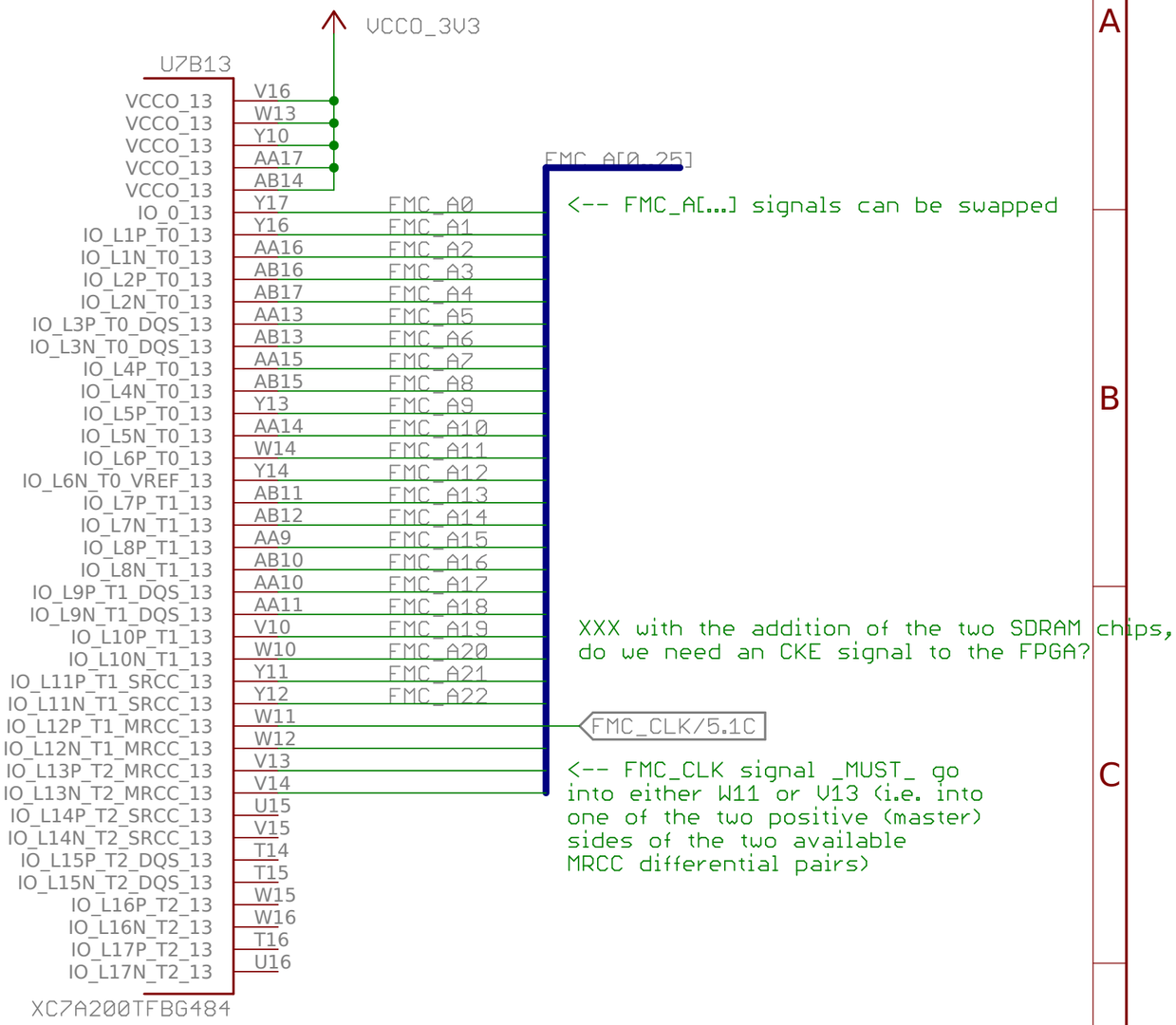
*) Lower Left Bank



*) Bottom Bank



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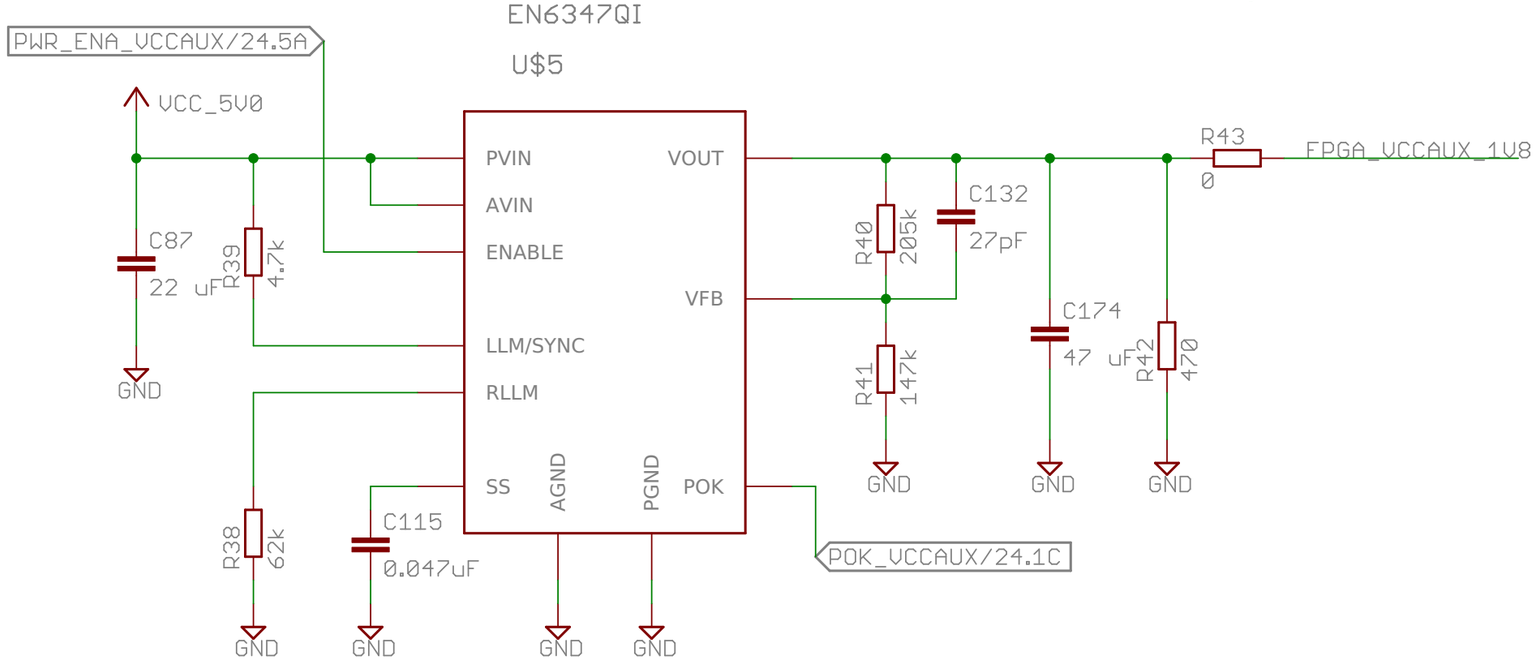
*) FPGA Power Subsystem -- AUX and I/O

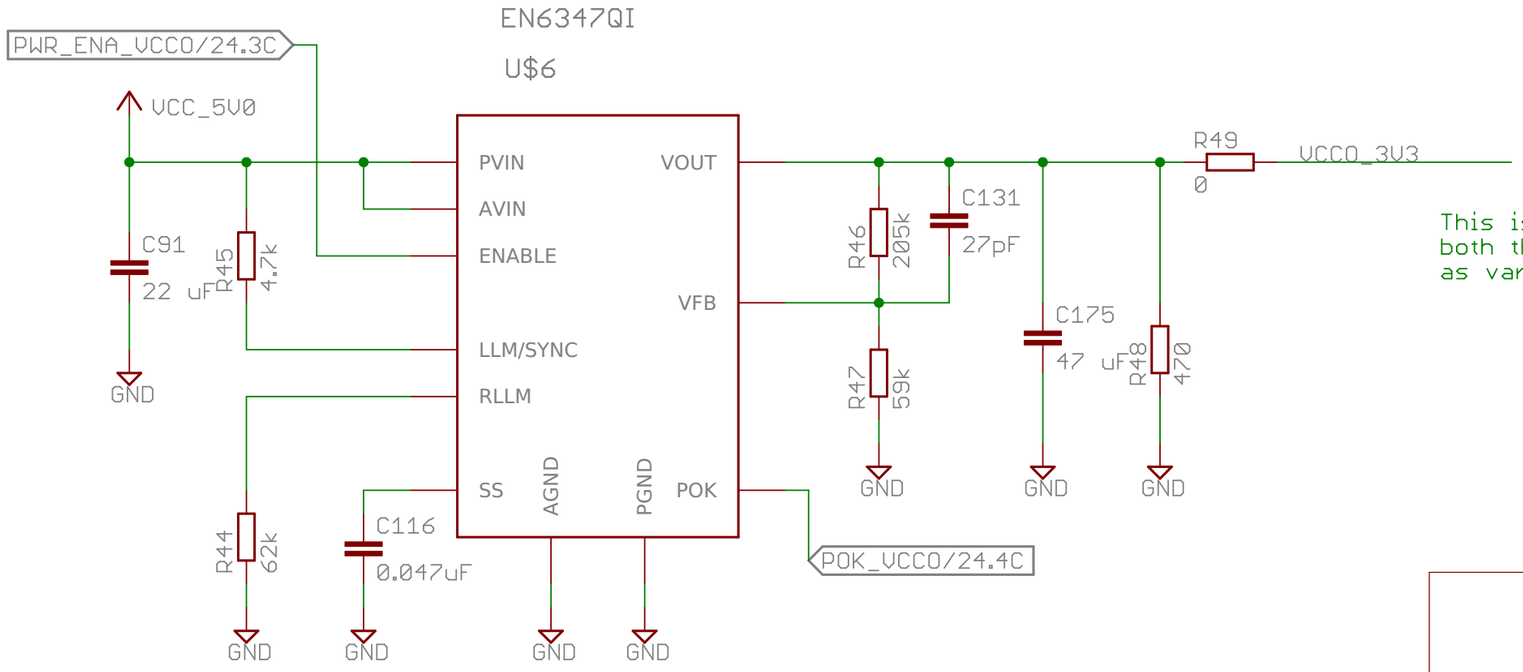
*) VCCAUX = 0.75V x (1 + 205 / 147) = 1.796V

*) VCCO = 0.75V x (1 + 205 / 59) = 3.356

*) Minimal load current is 2 mA:
1.8V / 470 Ohm = ~4mA
3.3V / 470 Ohm = ~7mA

*) Light-load mode is enabled





This is the 3V3 rail that powers
both the FPGA and the ARM as well
as various other components.

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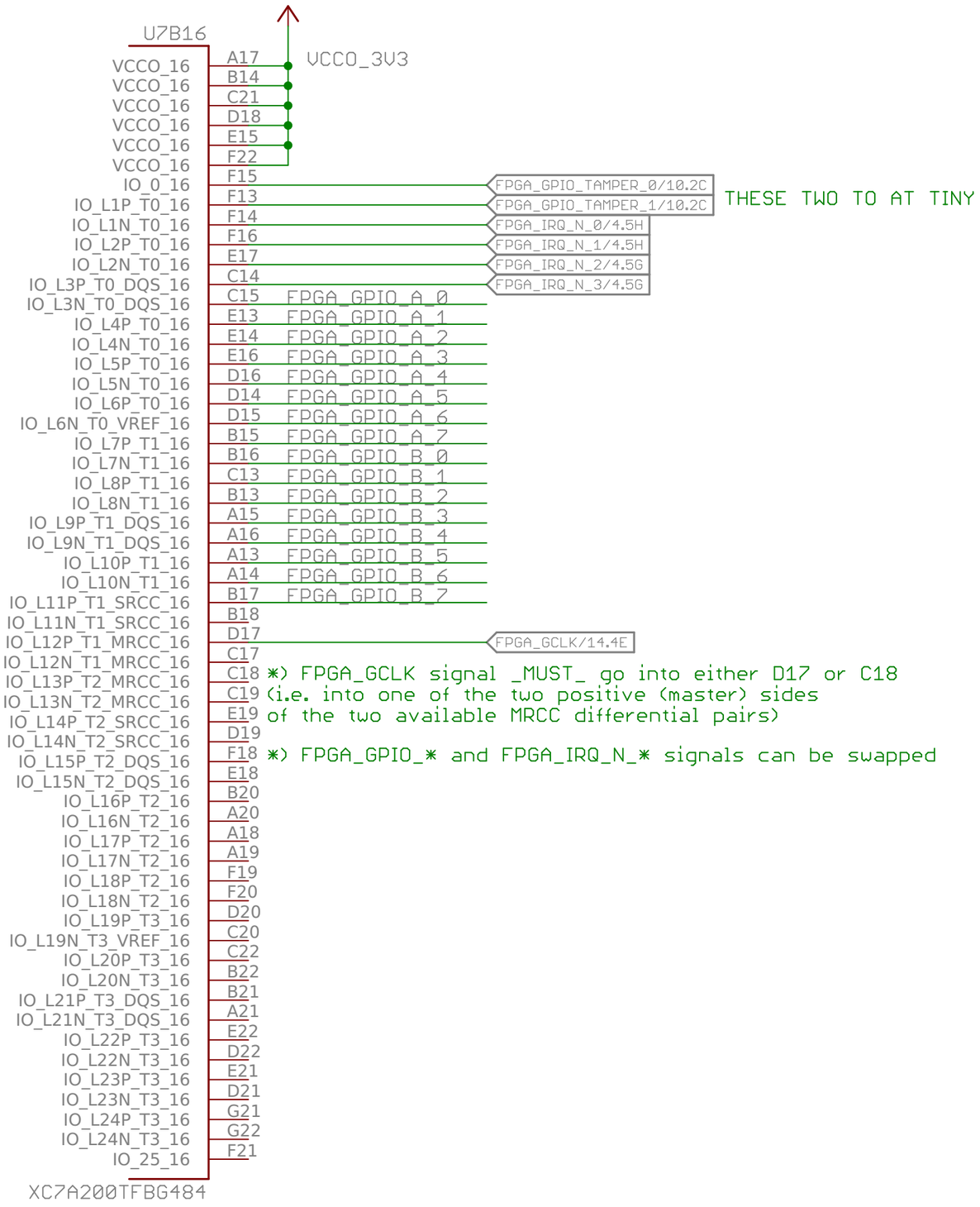
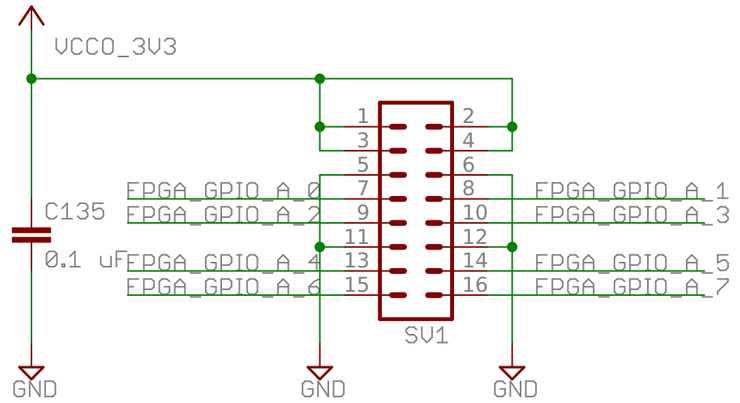
*) Upper Right Bank

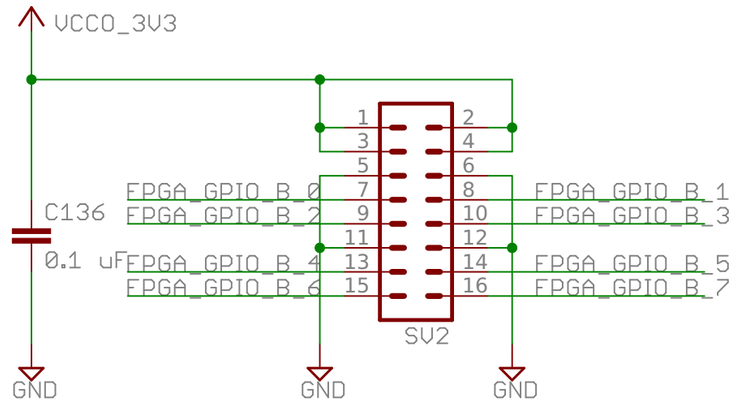


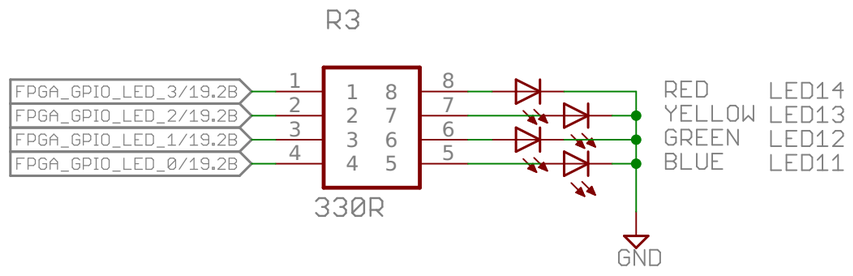
*) FPGA_GCLK signal _MUST_ go into either D17 or C18
(i.e. into one of the two positive (master) sides
of the two available MRCC differential pairs)

*) FPGA_GPIO_* and FPGA_IRQ_N_* signals can be swapped

*) Signals, that are allowed to be swapped, can be be swapped
with each other and/or moved to different pins within their bank.







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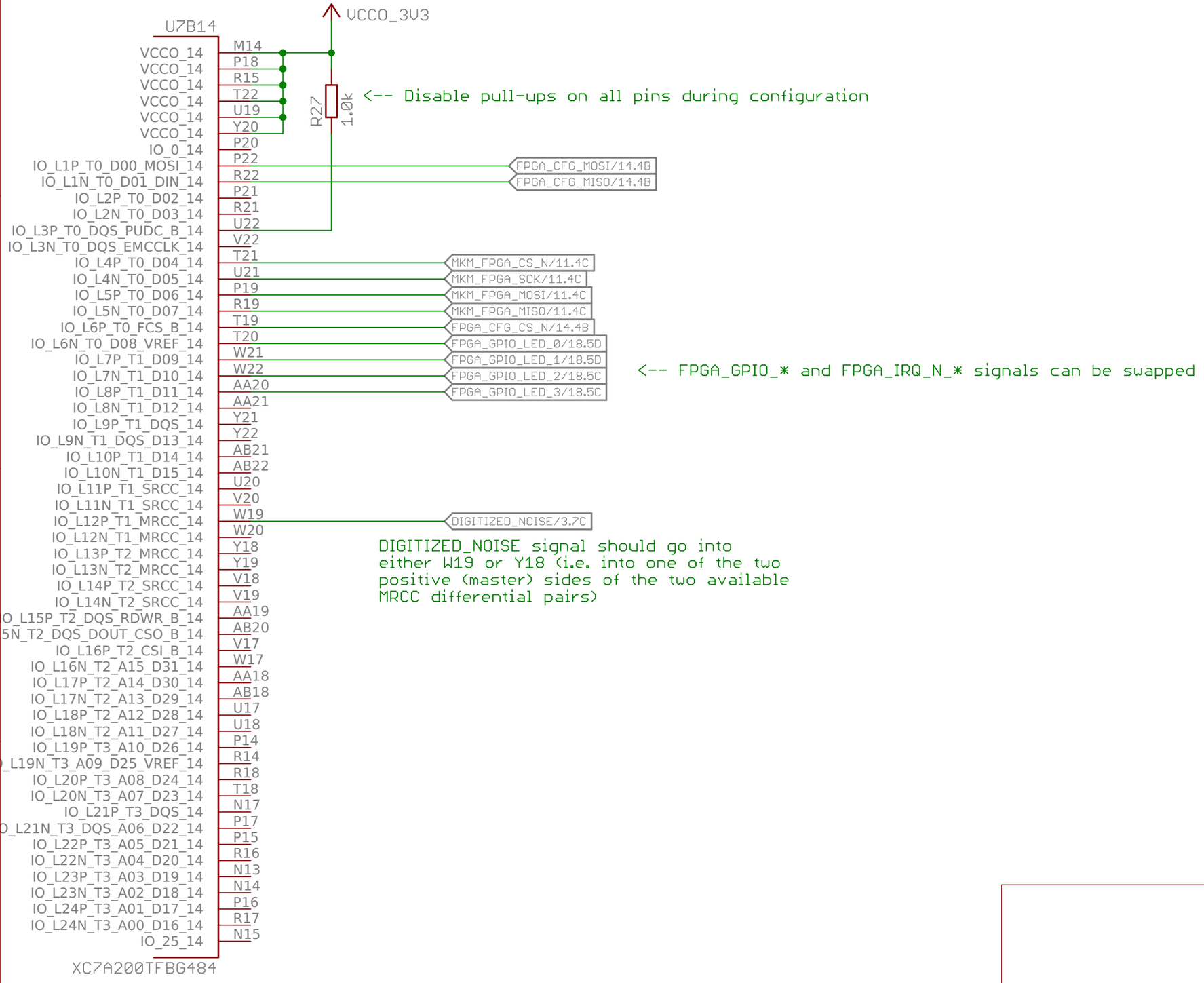
*) Signals, that are allowed to be swapped, can be be swapped with each other and/or moved to different pins within their bank.

*) Lower Right Bank



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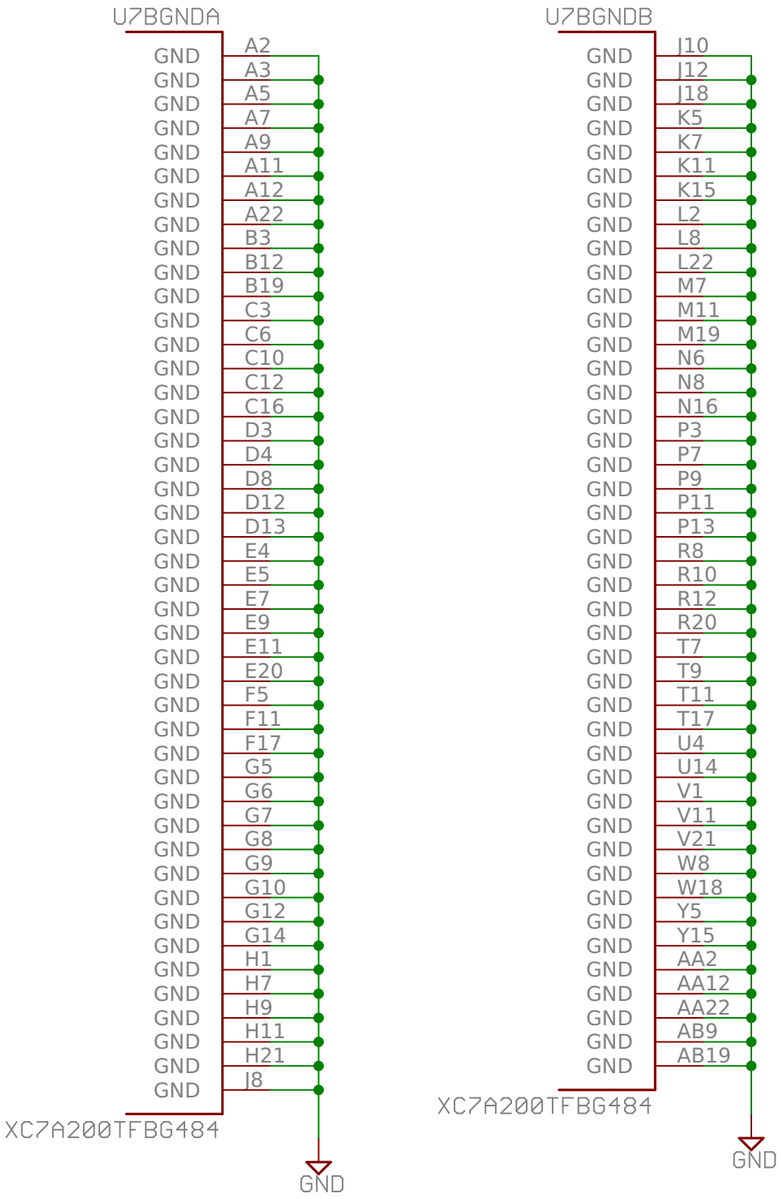
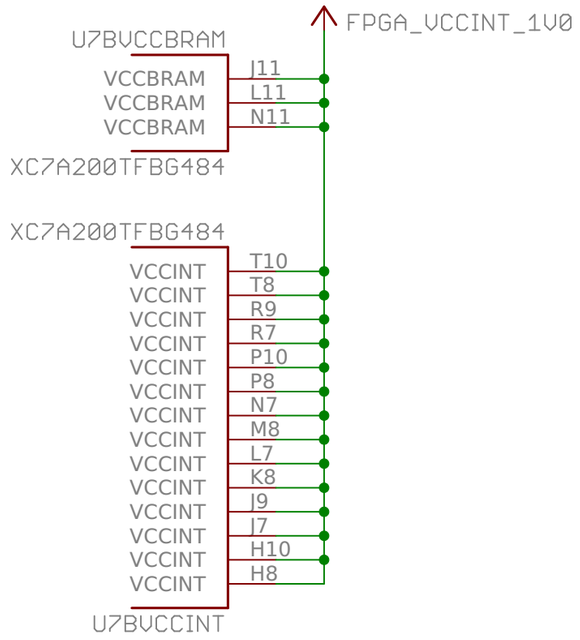
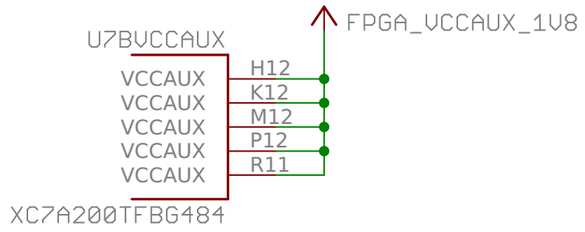
*) Ground Pins



*) Power - CORE & BRAM



*) Power - AUX



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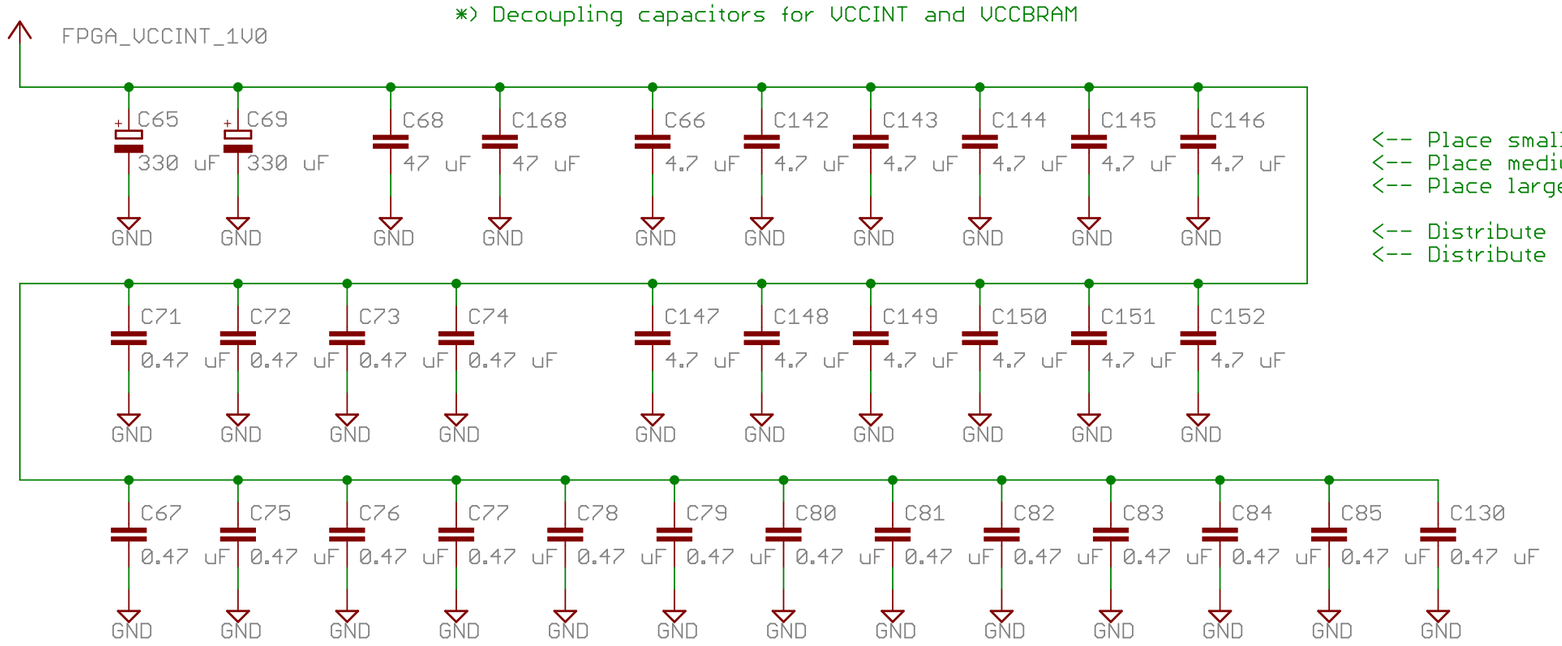
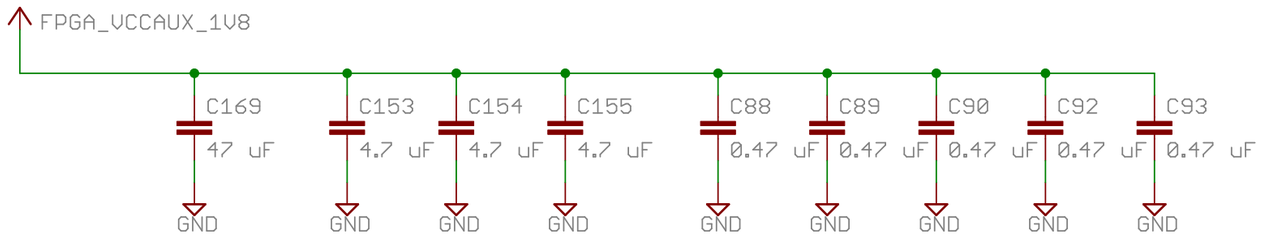
*) Decoupling capacitors for VCCINT and VCCBRAM



<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF and 330 uF caps not far from the BGA package

<-- Distribute smaller caps evenly under the BGA package
<-- Distribute larger caps evenly around the BGA package

*) Decoupling capacitors for VCCAUX



<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF caps not far from the BGA package

<-- Try to place smaller caps next to FPGA balls

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*) Decoupling capacitors for VCCO

VCCO_3V3

C170 47 uF GND
C171 47 uF GND
C172 47 uF GND
C173 47 uF GND

C156 4.7 uF GND
C157 4.7 uF GND
C97 0.47 uF GND
C98 0.47 uF GND
C100 0.47 uF GND
C101 0.47 uF GND

<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF caps not far from the BGA package

<-- Place one of four 47 uF caps on every side of the BGA package
<-- Distribute six sets of caps among six FPGA I/O banks

C159 4.7 uF GND
C158 4.7 uF GND
C102 0.47 uF GND
C105 0.47 uF GND
C106 0.47 uF GND
C107 0.47 uF GND

C160 4.7 uF GND
C161 4.7 uF GND
C108 0.47 uF GND
C109 0.47 uF GND
C113 0.47 uF GND
C117 0.47 uF GND

C163 4.7 uF GND
C162 4.7 uF GND
C118 0.47 uF GND
C119 0.47 uF GND
C120 0.47 uF GND
C121 0.47 uF GND

C164 4.7 uF GND
C165 4.7 uF GND
C122 0.47 uF GND
C123 0.47 uF GND
C124 0.47 uF GND
C125 0.47 uF GND

C167 4.7 uF GND
C166 4.7 uF GND
C126 0.47 uF GND
C127 0.47 uF GND
C128 0.47 uF GND
C129 0.47 uF GND

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*) FPGA Power Subsystem -- CORE

*) VCCINT = 0.6V x (1 + 150 / 226) = 0.998V

*) OCP_ADJ is not used (default over-current threshold)

*) MARx are not used (output at nominal 100%)

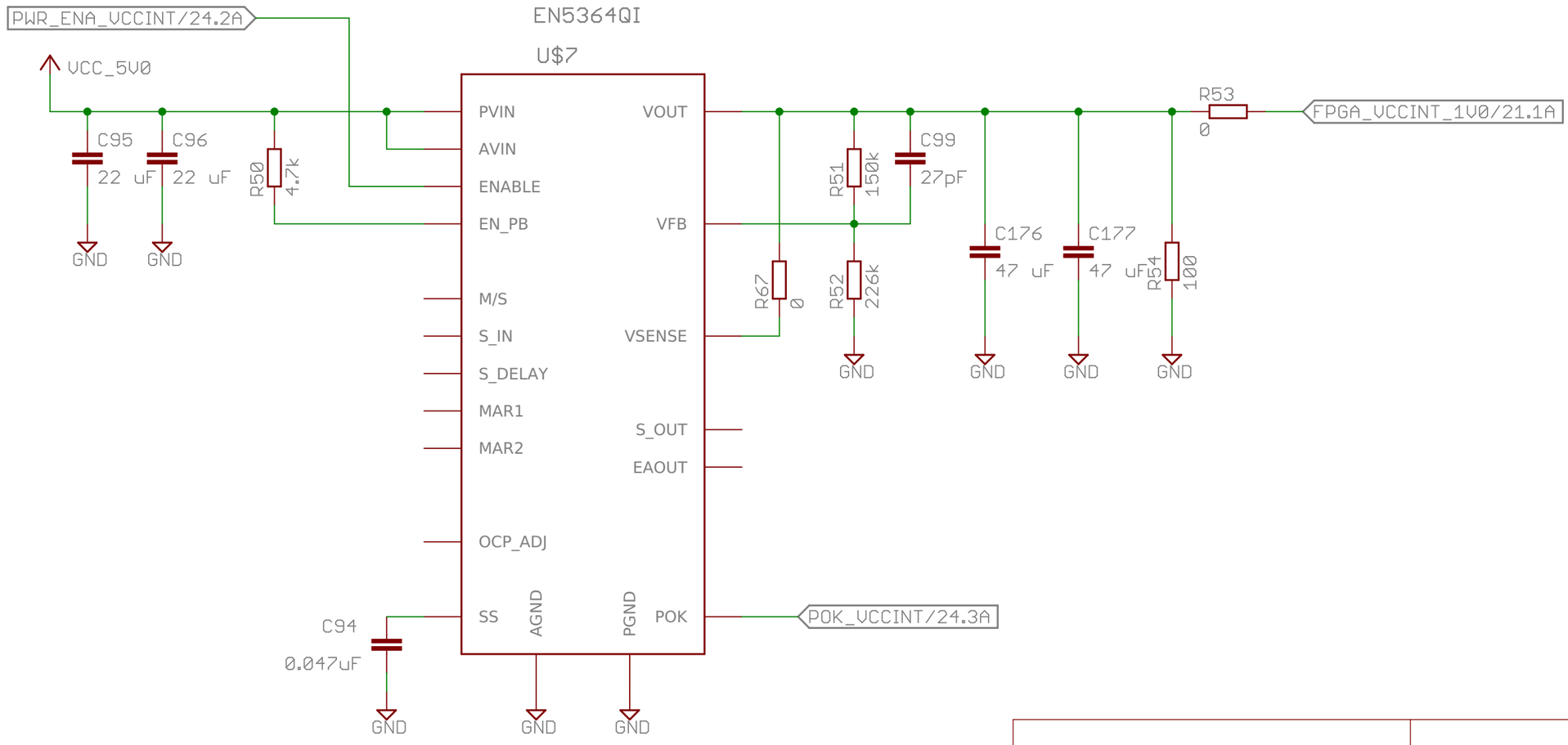
*) S_IN/S_OUT are not used (single regulator mode)

*) S_DELAY is not used (single regulator mode)

*) M/S is not used (parallel operation not needed)

*) EA_OUT is not used (default control loop)

*) Minimal load current is 0A, but we still place load of 100 Ohms just in case (gives 10 mA)



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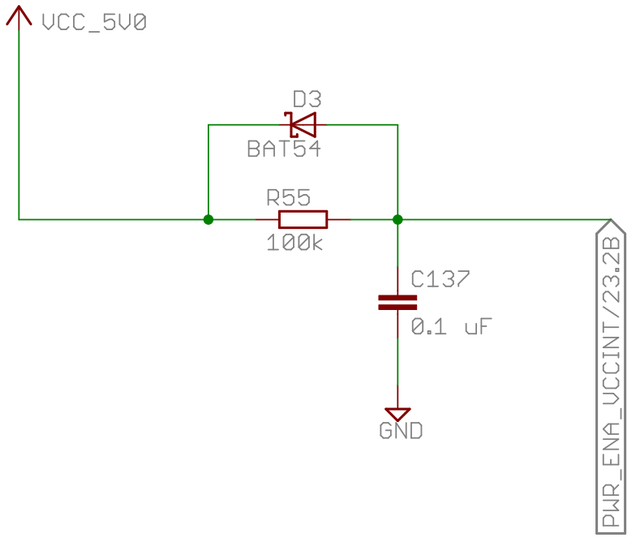
*) Recommended power-up sequence:

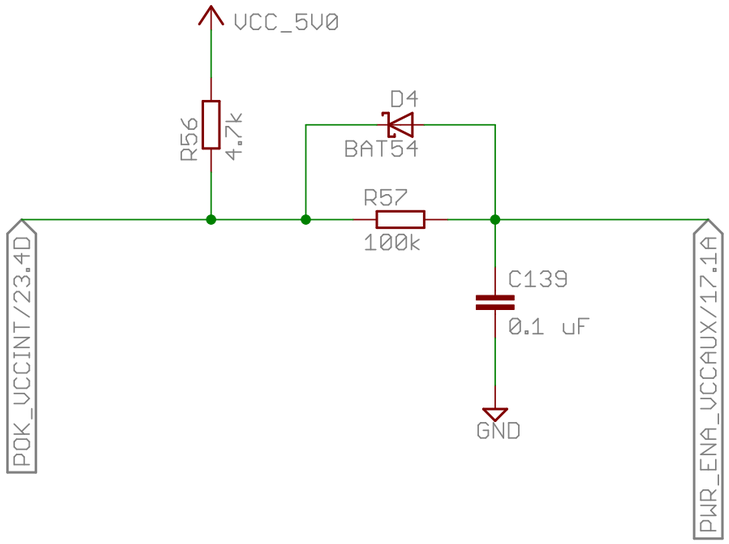
1) VCCINT

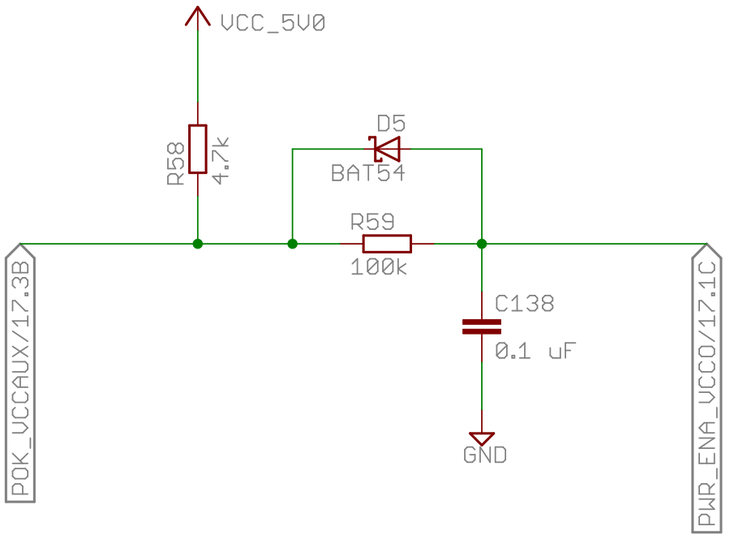
2) VCCAUX

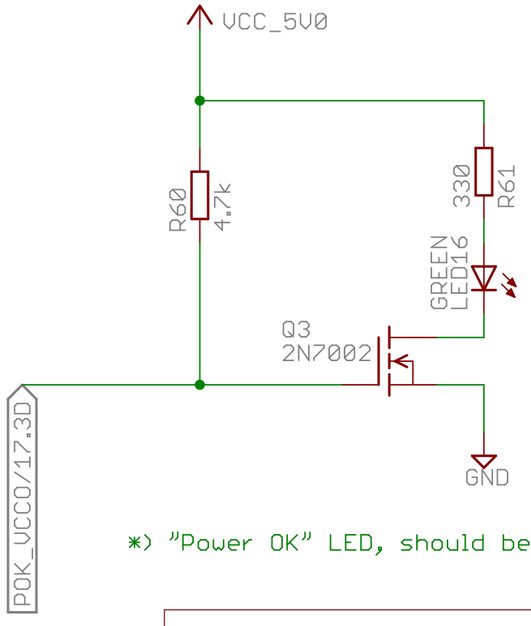
3) VCCO

RC network values are preliminary,
should be tweaked after experiments









*) "Power OK" LED, should be of green color

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