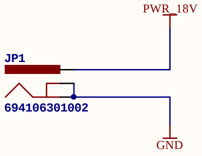
This document contains the electrical schematics for the Crypthech Alpha board.
The latest version of these schematics can be found here:
https://wiki.cryptech.is/browser/hardware/eagle/alpha
For more information about the Alpha board including functionality, goals
and block diagram, please see:
https://wiki.cryptech.is/wiki/AlphaBoardStrategy
For more information about the Cryptech project, please see:
https://cryptech.is/

| | | | |
|---|---|---|---|
| Title | | | |
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_0.SchDoc | Drawn By: | |

## Main power input 18V DC

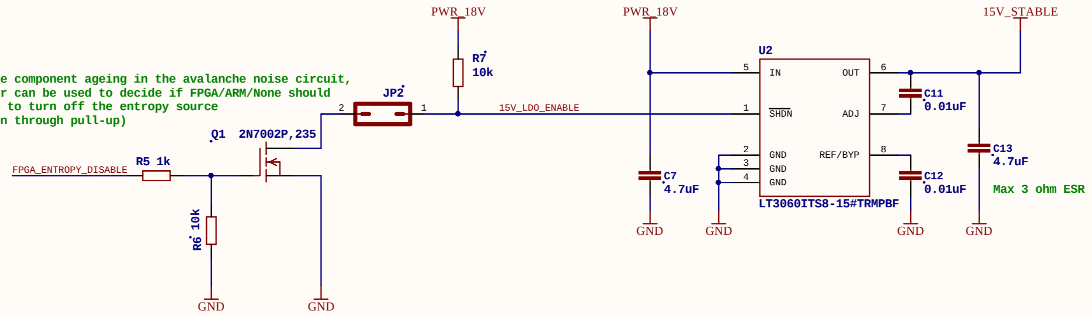


XXX verify symbol

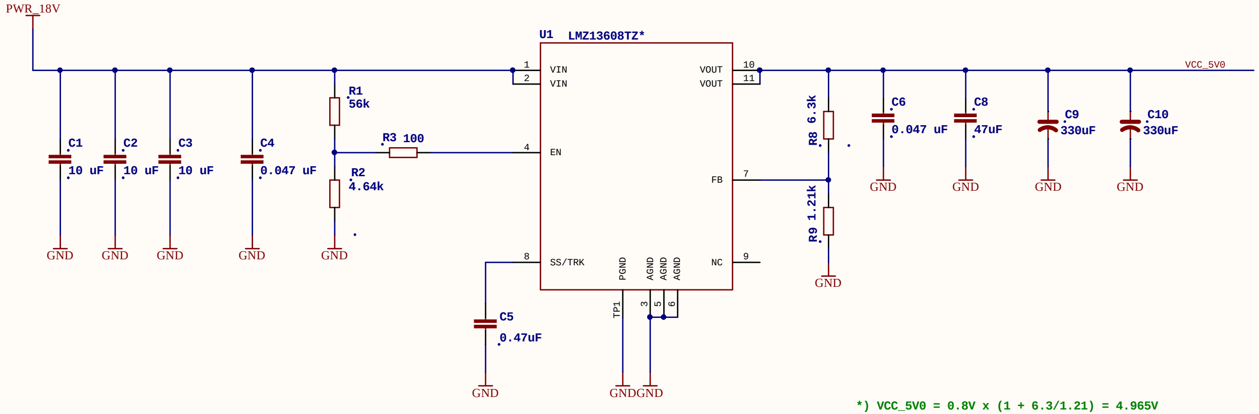
## Entropy source power

To mitigate component ageing in the avalanche noise circuit, this jumper can be used to decide if FPGA/ARM/None should be allowed to turn off the entropy source (default On through pull-up)

### 15V LDO powered from external 18V and supplying stable 15V to noise source



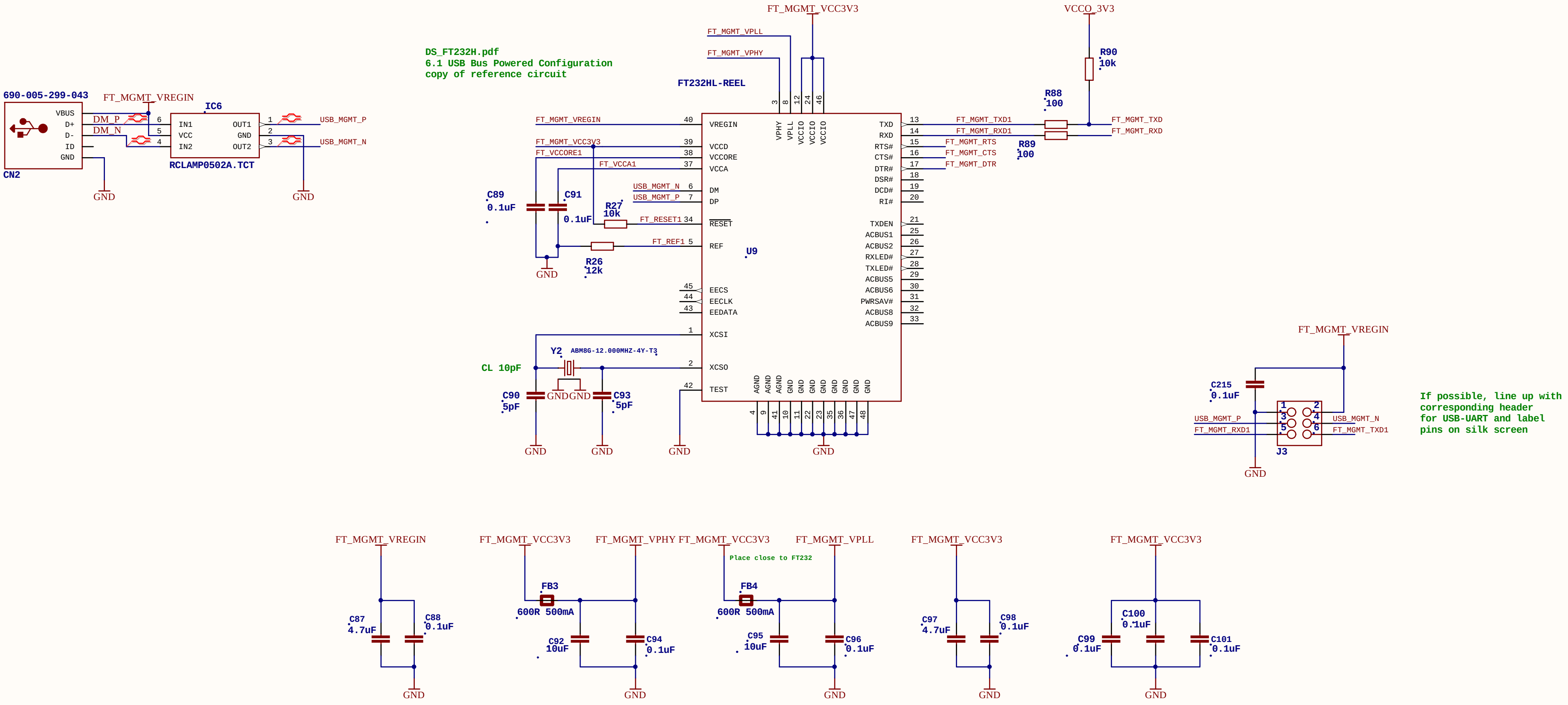
### *) Intermediate Regulator: 18V -> 5V



*) VCC_5V0 = 0.8V x (1 + 6.3/1.21) = 4.965V
*) Current sharing not used
*) SYNC is not used

| Title | Input power | |
|---|---|---|
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_1.SchDoc | | Drawn By: |

# Management access USB UART



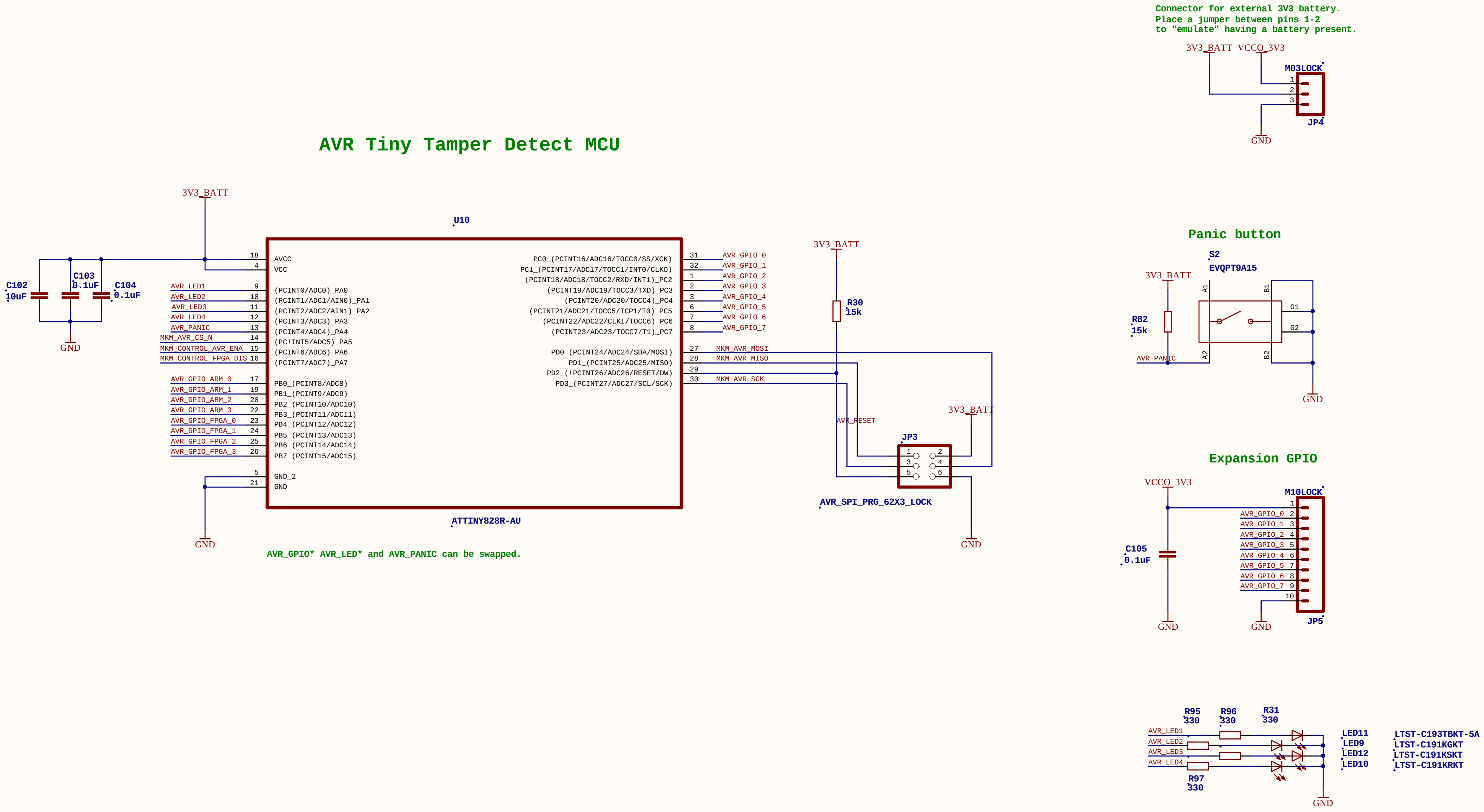
DS_FT232H.pdf
6.1 USB Bus Powered Configuration
copy of reference circuit

Place close to FT232

If possible, line up with corresponding header for USB-UART and label pins on silk screen

| Title | MGMT USB-UART | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_10.SchDoc | Drawn By: | |

# AVR Tiny Tamper Detect MCU



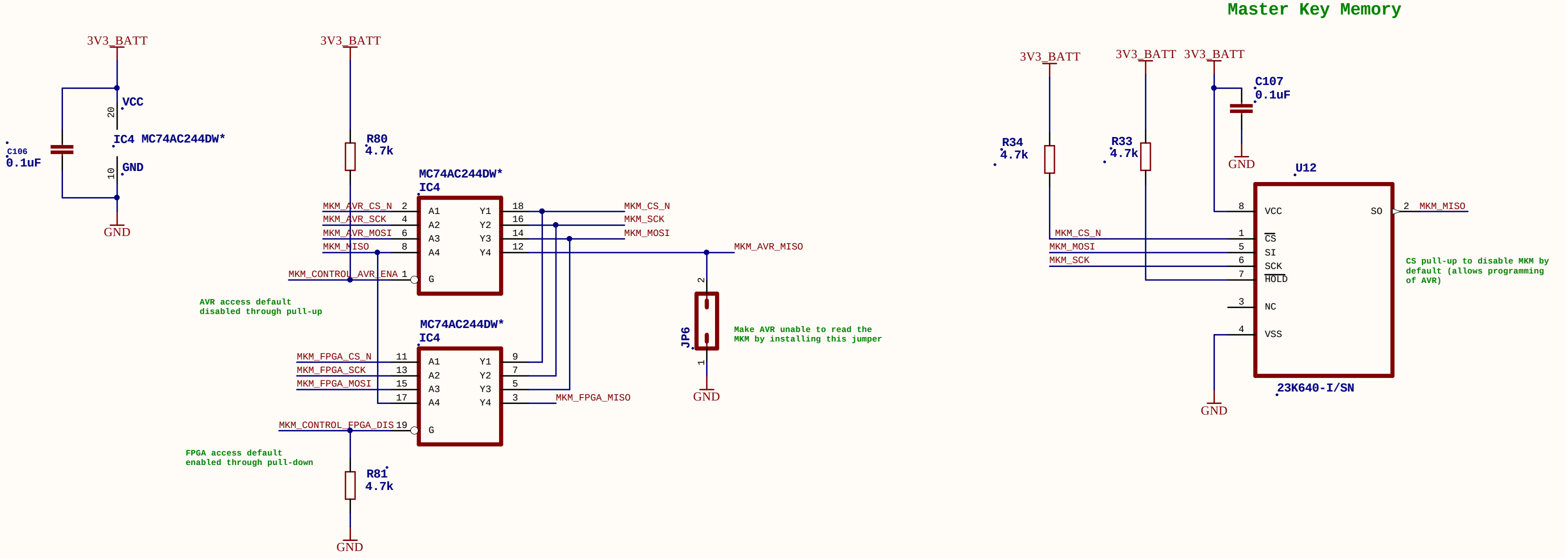
Connector for external 3V3 battery.
Place a jumper between pins 1-2
to "emulate" having a battery present.
3V3_BATT
VCCO_3V3
M03LOCK
JP4
1
2
3
GND
U10
ATTINY828R-AU
3V3_BATT
C102
10uF
C103
0.1uF
C104
0.1uF
GND
18 AVCC
4 VCC
AVR_LED1 9 (PCINT0/ADC0)_PA0
AVR_LED2 10 (PCINT1/ADC1/AIN0)_PA1
AVR_LED3 11 (PCINT2/ADC2/AIN1)_PA2
AVR_LED4 12 (PCINT3/ADC3)_PA3
AVR_PANIC 13 (PCINT4/ADC4)_PA4
MKM_AVR_CS_N 14 (PC!INT5/ADC5)_PA5
MKM_CONTROL_AVR_ENA 15 (PCINT6/ADC6)_PA6
MKM_CONTROL_FPGA_DIS 16 (PCINT7/ADC7)_PA7
AVR_GPIO_ARM_0 17 PB0_(PCINT8/ADC8)
AVR_GPIO_ARM_1 19 PB1_(PCINT9/ADC9)
AVR_GPIO_ARM_2 20 PB2_(PCINT10/ADC10)
AVR_GPIO_ARM_3 22 PB3_(PCINT11/ADC11)
AVR_GPIO_FPGA_0 23 PB4_(PCINT12/ADC12)
AVR_GPIO_FPGA_1 24 PB5_(PCINT13/ADC13)
AVR_GPIO_FPGA_2 25 PB6_(PCINT14/ADC14)
AVR_GPIO_FPGA_3 26 PB7_(PCINT15/ADC15)
5 GND_2
21 GND
GND
PC0_(PCINT16/ADC16/TOCC0/SS/XCK) 31 AVR_GPIO_0
PC1_(PCINT17/ADC17/TOCC1/INT0/CLKO) 32 AVR_GPIO_1
(PCINT18/ADC18/TOCC2/RXD/INT1)_PC2 1 AVR_GPIO_2
(PCINT19/ADC19/TOCC3/TXD)_PC3 2 AVR_GPIO_3
(PCINT20/ADC20/TOCC4)_PC4 3 AVR_GPIO_4
(PCINT21/ADC21/TOCC5/ICP1/T0)_PC5 6 AVR_GPIO_5
(PCINT22/ADC22/CLKI/TOCC6)_PC6 7 AVR_GPIO_6
(PCINT23/ADC23/TOCC7/T1)_PC7 8 AVR_GPIO_7
PD0_(PCINT24/ADC24/SDA/MOSI) 27 MKM_AVR_MOSI
PD1_(PCINT25/ADC25/MISO) 28 MKM_AVR_MISO
PD2_(!PCINT26/ADC26/RESET/DW) 29
PD3_(PCINT27/ADC27/SCL/SCK) 30 MKM_AVR_SCK
AVR_GPIO* AVR_LED* and AVR_PANIC can be swapped.
3V3_BATT
R30
15k
AVR_RESET
3V3_BATT
JP3
1 2
3 4
5 6
AVR_SPI_PRG_62X3_LOCK
GND
Panic button
S2
EVQPT9A15
3V3_BATT
R82
15k
AVR_PANIC
A1
A2
B1
B2
G1
G2
GND
Expansion GPIO
VCCO_3V3
M10LOCK
C105
0.1uF
GND
1
AVR_GPIO_0 2
AVR_GPIO_1 3
AVR_GPIO_2 4
AVR_GPIO_3 5
AVR_GPIO_4 6
AVR_GPIO_5 7
AVR_GPIO_6 8
AVR_GPIO_7 9
10
GND
JP5
R95
330
R96
330
R31
330
R97
330
AVR_LED1
AVR_LED2
AVR_LED3
AVR_LED4
LED11
LED9
LED12
LED10
LTST-C193TBKT-5A
LTST-C191KGKT
LTST-C191KSKT
LTST-C191KRKT
GND

Title

**AVR Tamper circuit**

| | | |
|---|---|---|
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_11.SchDoc | | Drawn By: |

SPI mux controlling access to the MKM.
Normally, the FPGA has R/W access to the MKM but on a
tamper event the tamper detect MCU (AVR) will grab access
to the MKM and erase the contents.



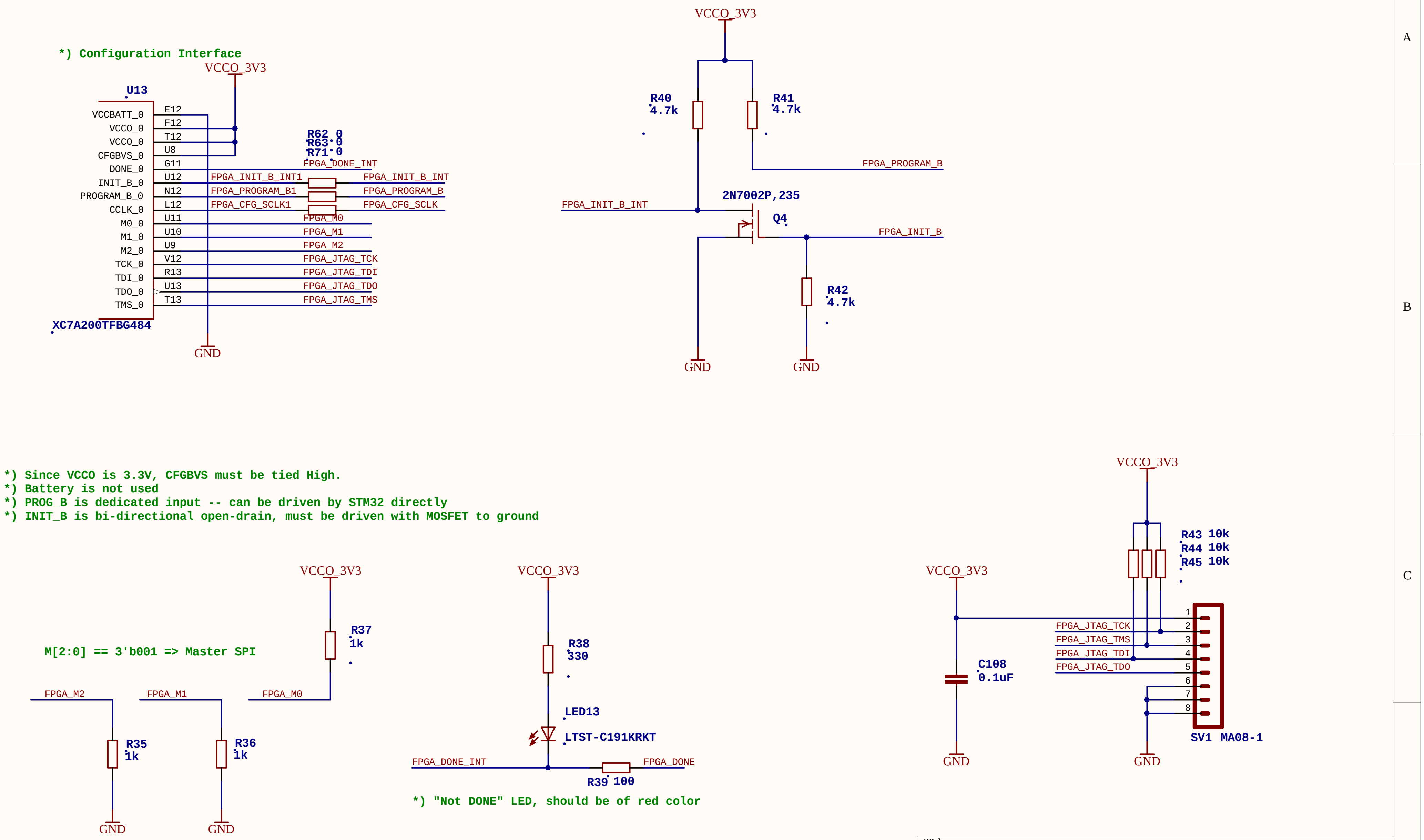
Title
Master Key Memory

Size
A4

Number

Revision

Date: 30.05.2016
File: C:\SHARE\..\rev02_12.SchDoc
Sheet of
Drawn By:



*) Configuration Interface

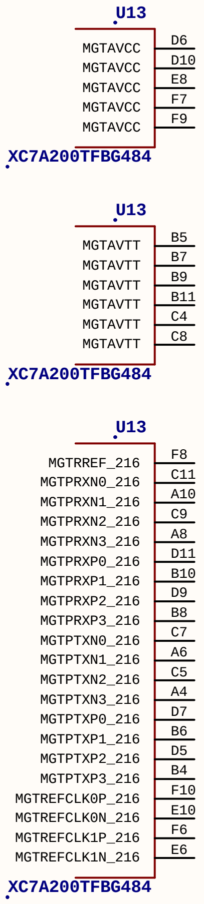
*) Since VCCO is 3.3V, CFGBVS must be tied High.
*) Battery is not used
*) PROG_B is dedicated input -- can be driven by STM32 directly
*) INIT_B is bi-directional open-drain, must be driven with MOSFET to ground

M[2:0] == 3'b001 => Master SPI

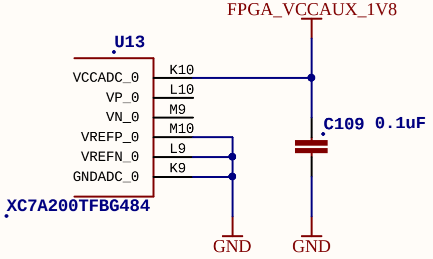
*) "Not DONE" LED, should be of red color

| Title | | |
|---|---|---|
| FPGA configuration interface | | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_13.SchDoc | | Drawn By: |

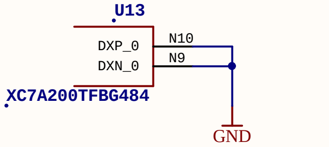
*) Transceivers [NOT USED]



*) XADC [NOT USED]



*) Temperature Sensor [NOT USED]

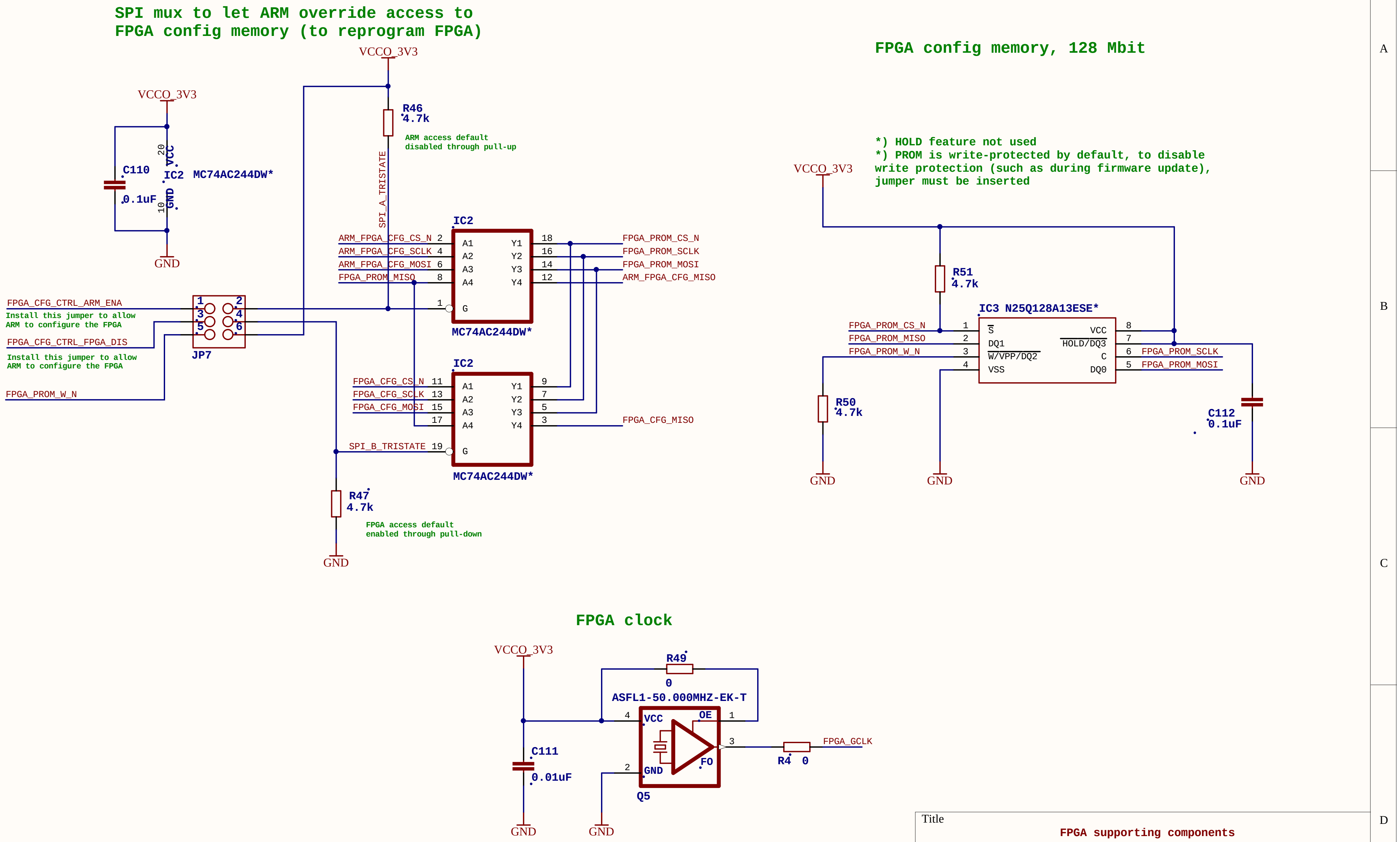


| Title | FPGA unused | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_14.SchDoc | Drawn By: | |

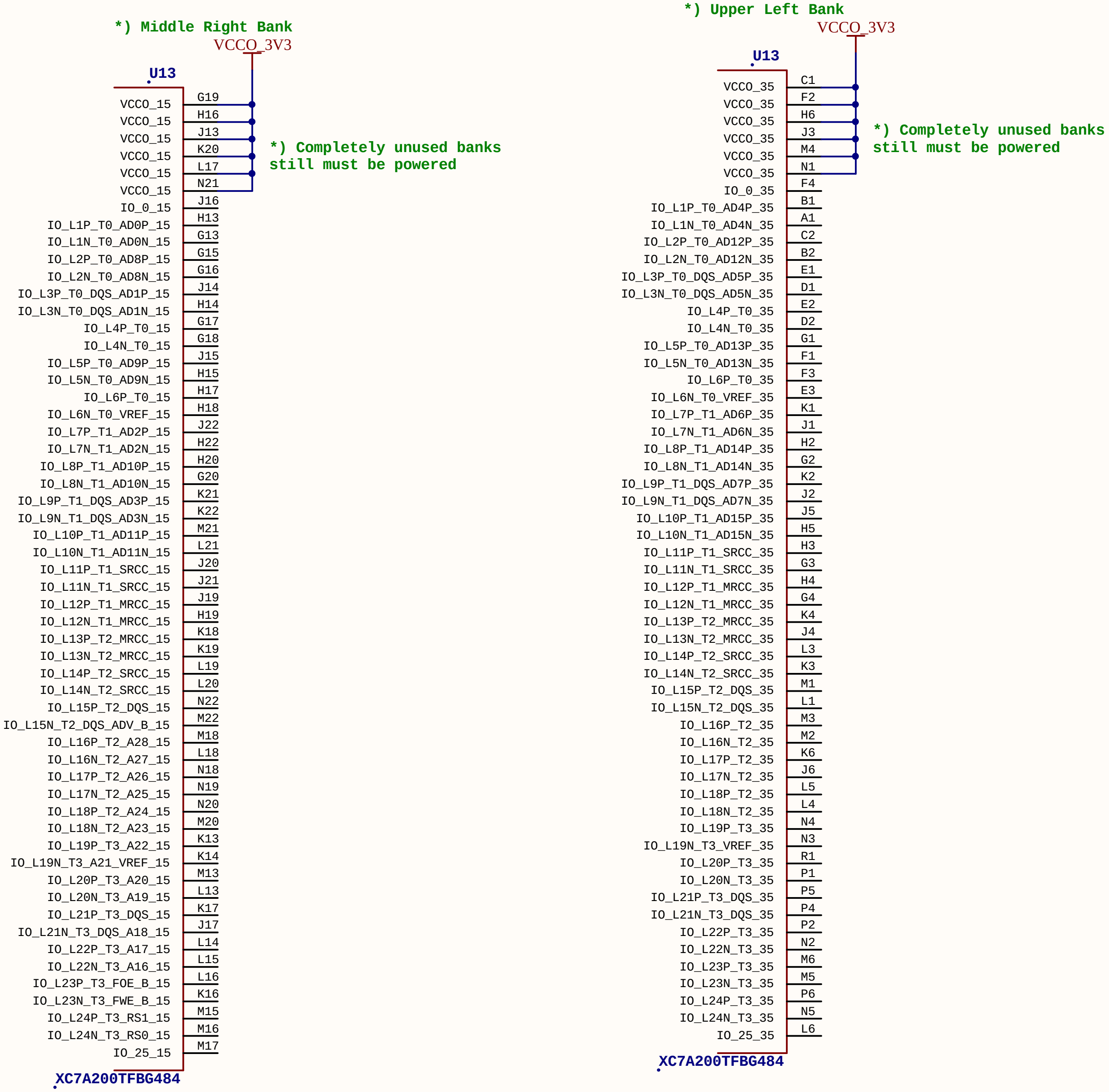
## SPI mux to let ARM override access to FPGA config memory (to reprogram FPGA)

## FPGA config memory, 128 Mbit

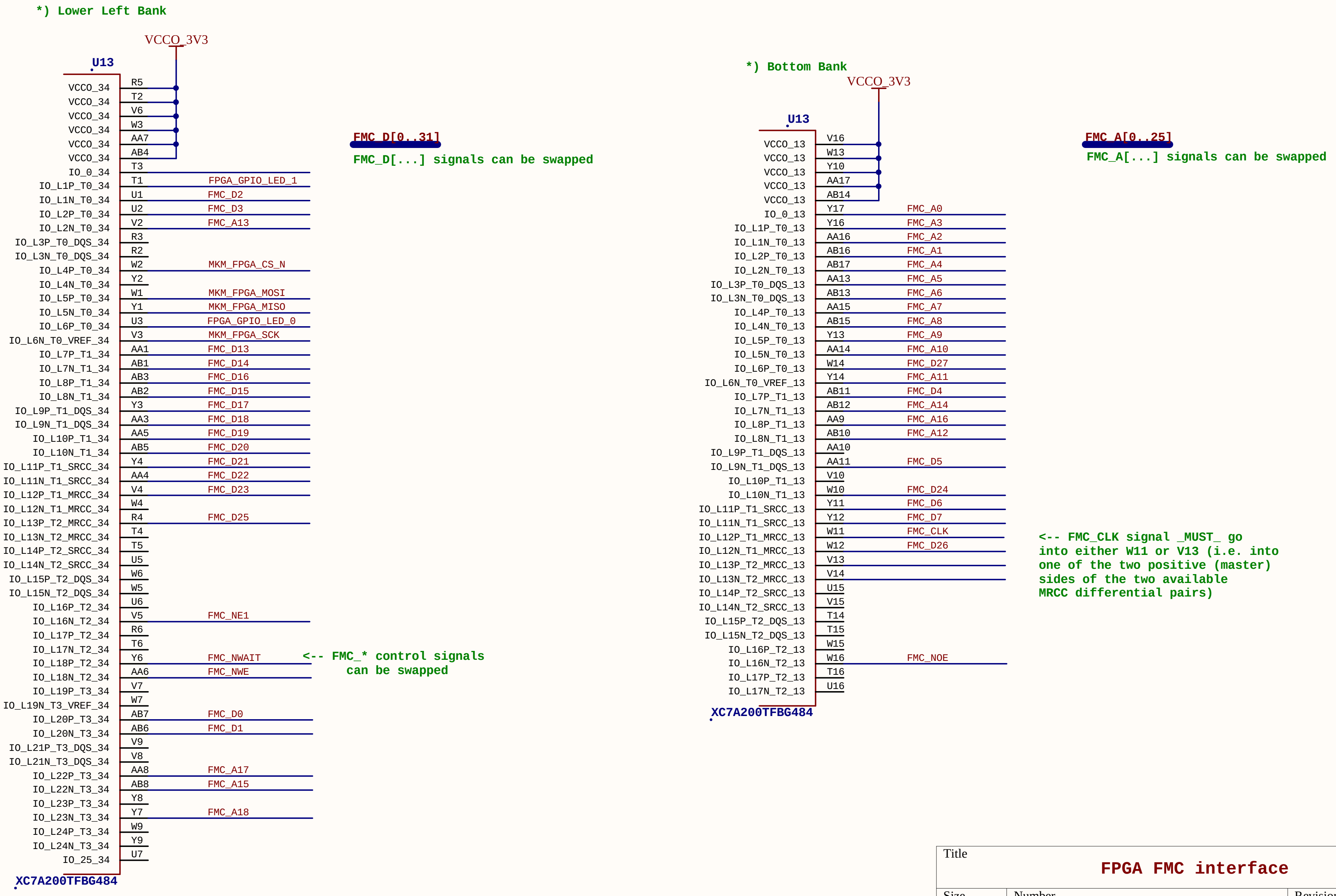
## FPGA clock



| Title | | |
|---|---|---|
| FPGA supporting components | | |
| Size | Number | Revision |
| A4 | | |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_15.SchDoc | | Drawn By: |



| | | | |
|---|---|---|---|
| Title | **FPGA unused banks** | | |
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_16.SchDoc | Drawn By: | |



*) Lower Left Bank

FMC_D[...] signals can be swapped

<-- FMC_* control signals
can be swapped

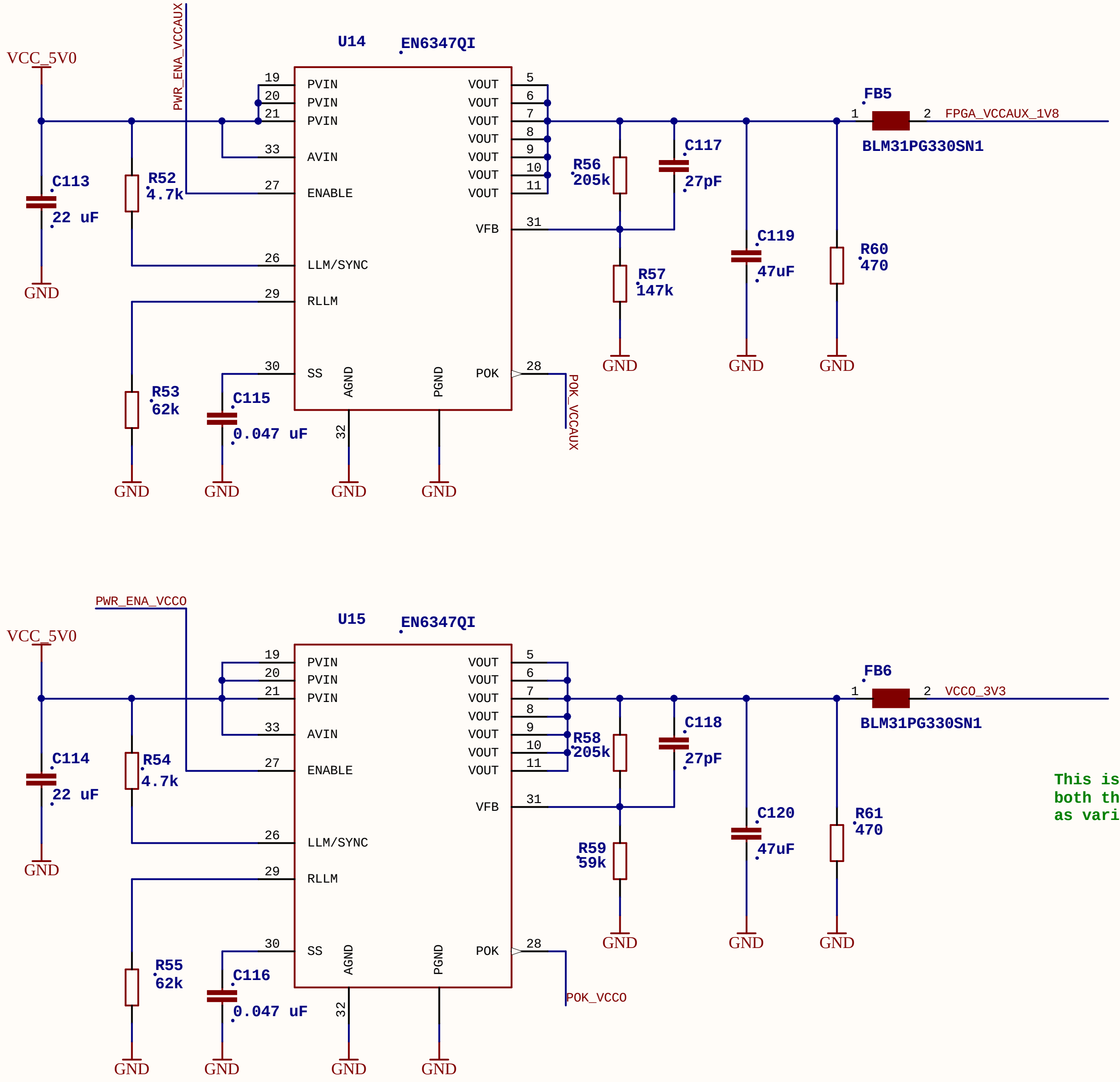
*) Bottom Bank

FMC_A[...] signals can be swapped

<-- FMC_CLK signal _MUST_ go
into either W11 or V13 (i.e. into
one of the two positive (master)
sides of the two available
MRCC differential pairs)

| Title | | |
|---|---|---|
| FPGA FMC interface | | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_17.SchDoc | | Drawn By: |

*) FPGA Power Subsystem -- AUX and I/O

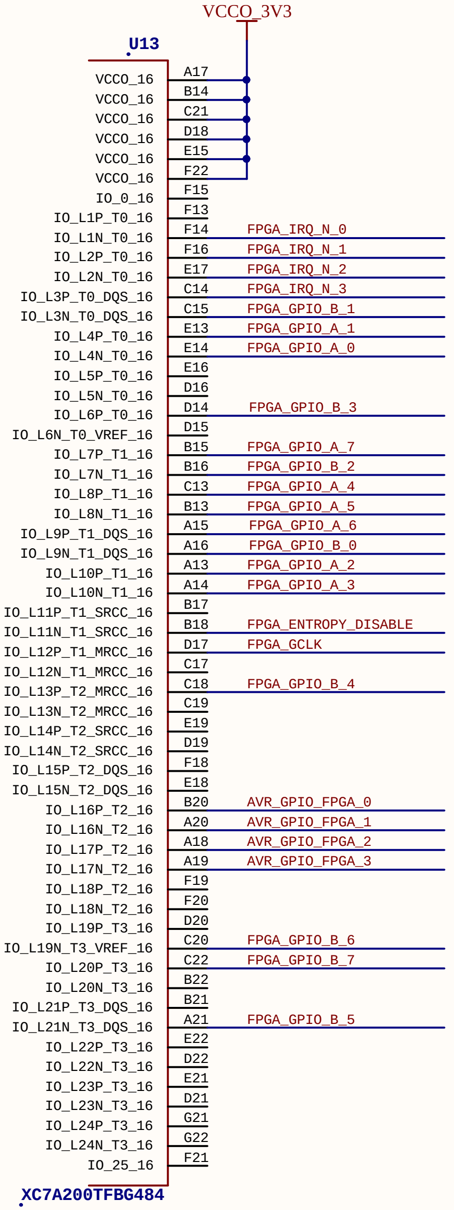


*) VCCAUX = 0.75V x (1 + 205 / 147) = 1.796V
*) VCCO = 0.75V x (1 + 205 / 59) = 3.356
*) Minimal load current is 2 mA:
1.8V / 470 Ohm = ~4mA
3.3V / 470 Ohm = ~7mA
*) Light-load mode is enabled

This is the 3V3 rail that powers
both the FPGA and the ARM as well
as various other components.

| Title | | |
|---|---|---|
| FPGA voltage regulators | | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_18.SchDoc | | Drawn By: |

*) Upper Right Bank

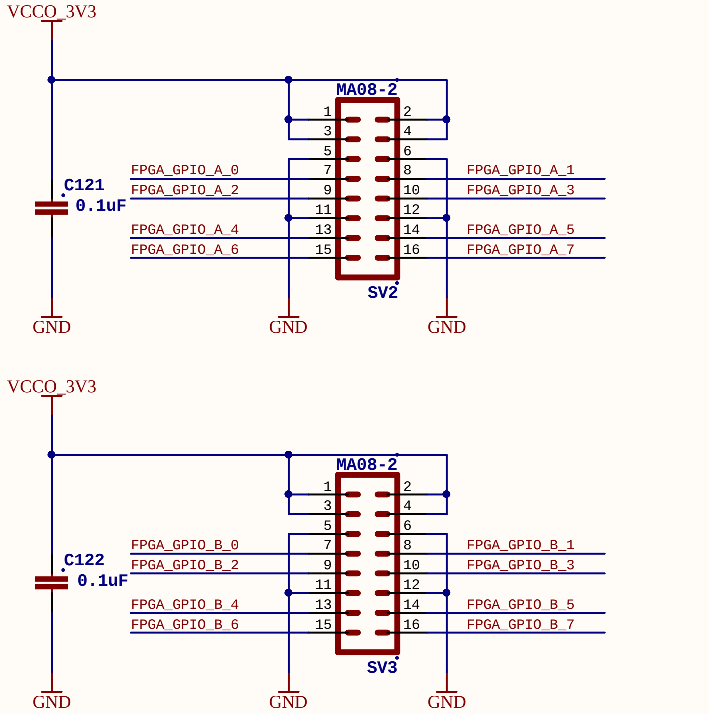

VCCO_3V3
U13
VCCO_16 A17
VCCO_16 B14
VCCO_16 C21
VCCO_16 D18
VCCO_16 E15
VCCO_16 F22
IO_0_16 F15
IO_L1P_T0_16 F13
IO_L1N_T0_16 F14 FPGA_IRQ_N_0
IO_L2P_T0_16 F16 FPGA_IRQ_N_1
IO_L2N_T0_16 E17 FPGA_IRQ_N_2
IO_L3P_T0_DQS_16 C14 FPGA_IRQ_N_3
IO_L3N_T0_DQS_16 C15 FPGA_GPIO_B_1
IO_L4P_T0_16 E13 FPGA_GPIO_A_1
IO_L4N_T0_16 E14 FPGA_GPIO_A_0
IO_L5P_T0_16 E16
IO_L5N_T0_16 D16
IO_L6P_T0_16 D14 FPGA_GPIO_B_3
IO_L6N_T0_VREF_16 D15
IO_L7P_T1_16 B15 FPGA_GPIO_A_7
IO_L7N_T1_16 B16 FPGA_GPIO_B_2
IO_L8P_T1_16 C13 FPGA_GPIO_A_4
IO_L8N_T1_16 B13 FPGA_GPIO_A_5
IO_L9P_T1_DQS_16 A15 FPGA_GPIO_A_6
IO_L9N_T1_DQS_16 A16 FPGA_GPIO_B_0
IO_L10P_T1_16 A13 FPGA_GPIO_A_2
IO_L10N_T1_16 A14 FPGA_GPIO_A_3
IO_L11P_T1_SRCC_16 B17
IO_L11N_T1_SRCC_16 B18 FPGA_ENTROPY_DISABLE
IO_L12P_T1_MRCC_16 D17 FPGA_GCLK
IO_L12N_T1_MRCC_16 C17
IO_L13P_T2_MRCC_16 C18 FPGA_GPIO_B_4
IO_L13N_T2_MRCC_16 C19
IO_L14P_T2_SRCC_16 E19
IO_L14N_T2_SRCC_16 D19
IO_L15P_T2_DQS_16 F18
IO_L15N_T2_DQS_16 E18
IO_L16P_T2_16 B20 AVR_GPIO_FPGA_0
IO_L16N_T2_16 A20 AVR_GPIO_FPGA_1
IO_L17P_T2_16 A18 AVR_GPIO_FPGA_2
IO_L17N_T2_16 A19 AVR_GPIO_FPGA_3
IO_L18P_T2_16 F19
IO_L18N_T2_16 F20
IO_L19P_T3_16 D20
IO_L19N_T3_VREF_16 C20 FPGA_GPIO_B_6
IO_L20P_T3_16 C22 FPGA_GPIO_B_7
IO_L20N_T3_16 B22
IO_L21P_T3_DQS_16 B21
IO_L21N_T3_DQS_16 A21 FPGA_GPIO_B_5
IO_L22P_T3_16 E22
IO_L22N_T3_16 D22
IO_L23P_T3_16 E21
IO_L23N_T3_16 D21
IO_L24P_T3_16 G21
IO_L24N_T3_16 G22
IO_25_16 F21
XC7A200TFBG484

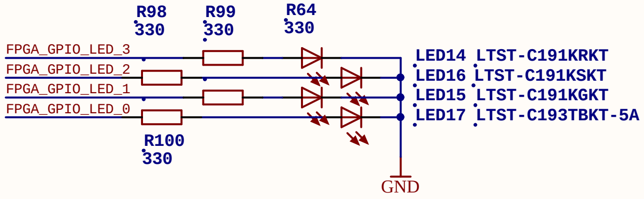
NOTE: One of the FPGA_GPIO_* pins should be connected to one of the MRCC pins.
The non-MRCC GPIO signals should be length matched to within 500 ps of the MRCC signal.

*) FPGA_GCLK signal _MUST_ go into either D17 or C18 (i.e. into one of the two positive (master) sides of the two available MRCC differential pairs)

*) FPGA_GPIO_* and FPGA_IRQ_N_* signals can be swapped

*) Signals, that are allowed to be swapped, can be be swapped with each other and/or moved to different pins within their bank.

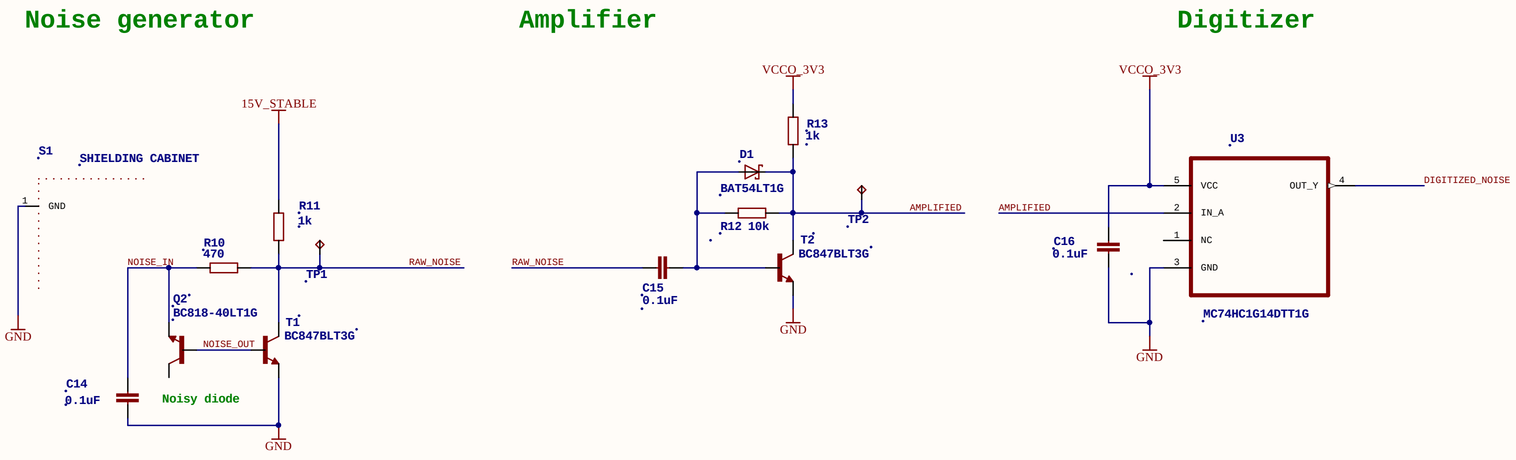

VCCO_3V3
MA08-2
C121
0.1uF
FPGA_GPIO_A_0 7 8 FPGA_GPIO_A_1
FPGA_GPIO_A_2 9 10 FPGA_GPIO_A_3
FPGA_GPIO_A_4 13 14 FPGA_GPIO_A_5
FPGA_GPIO_A_6 15 16 FPGA_GPIO_A_7
1 2 3 4 5 6 11 12
SV2
GND
GND
GND
VCCO_3V3
MA08-2
C122
0.1uF
FPGA_GPIO_B_0 7 8 FPGA_GPIO_B_1
FPGA_GPIO_B_2 9 10 FPGA_GPIO_B_3
FPGA_GPIO_B_4 13 14 FPGA_GPIO_B_5
FPGA_GPIO_B_6 15 16 FPGA_GPIO_B_7
1 2 3 4 5 6 11 12
SV3
GND
GND
GND



Title
**FPGA GPIO**

Size: A4
Number
Revision

Date: 30.05.2016
File: C:\SHARE\..\rev02_19.SchDoc
Sheet of
Drawn By:



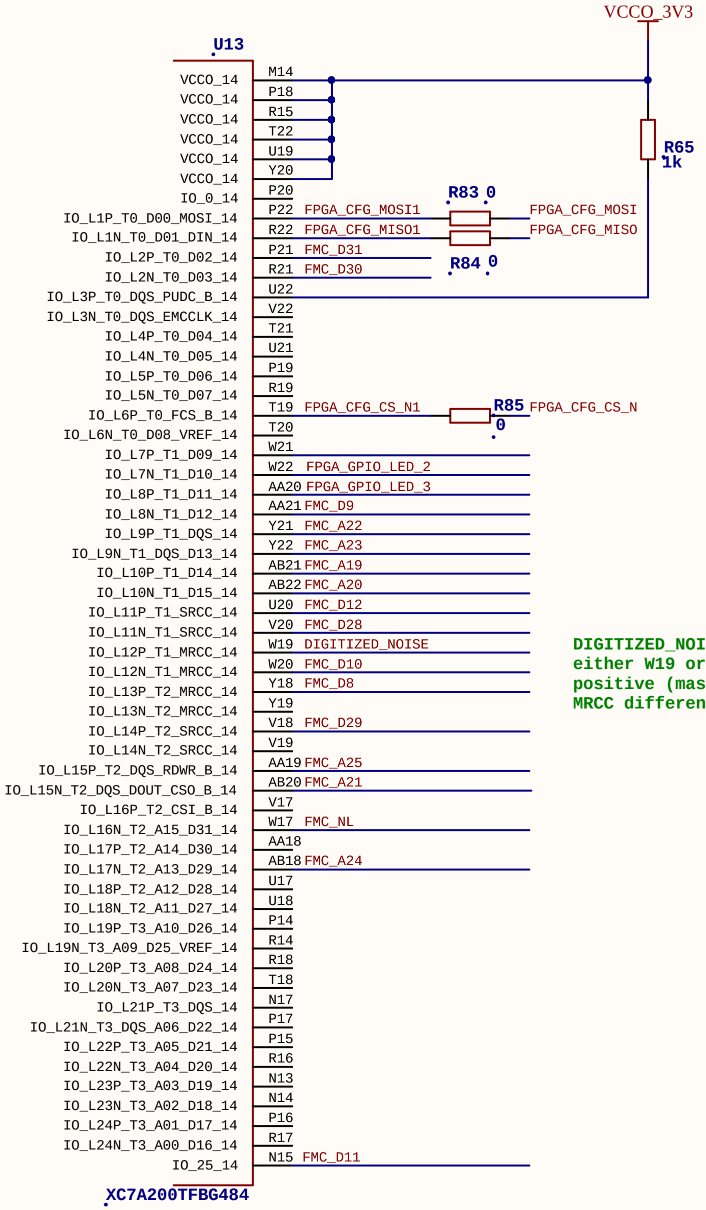
AGND is connected to GND on the board using polygons
(found no other good way) - not visible in schematics.

This whole sheets circuitry should be as shielded as possible.
Solid isolated ground plane and internal planes connected
to the rest of the board at a single point is expected.

| | | | |
|---|---|---|---|
| Title | **Noise source** | | |
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_2.SchDoc | Drawn By: | |

*) Lower Right Bank

*) Signals, that are allowed to be swapped, can be be swapped with each other and/or moved to different pins within their bank.

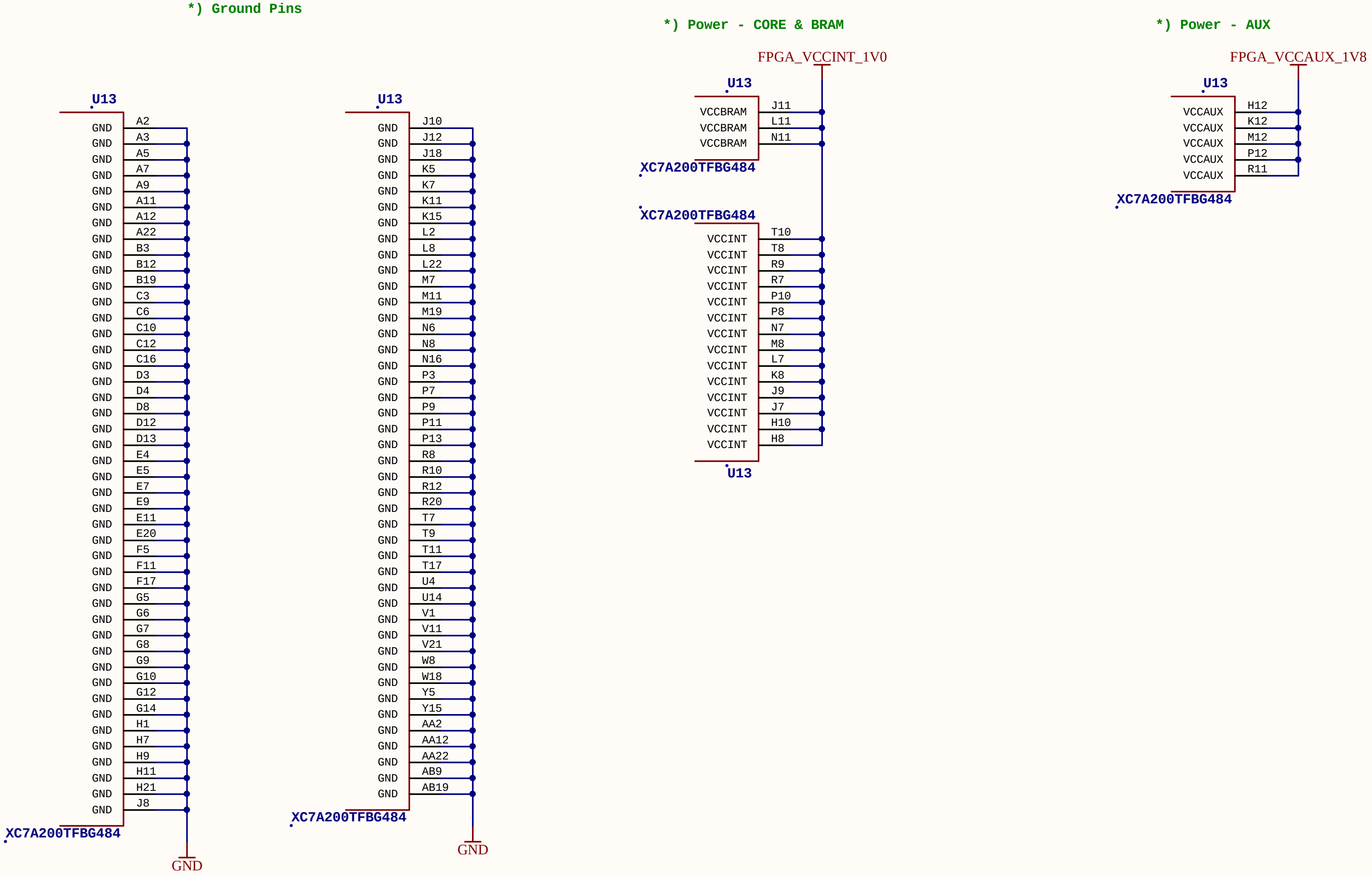

U13
VCCO_3V3
VCCO_14 M14
VCCO_14 P18
VCCO_14 R15
VCCO_14 T22
VCCO_14 U19
VCCO_14 Y20
IO_0_14 P20
IO_L1P_T0_D00_MOSI_14 P22 FPGA_CFG_MOSI1
IO_L1N_T0_D01_DIN_14 R22 FPGA_CFG_MISO1
IO_L2P_T0_D02_14 P21 FMC_D31
IO_L2N_T0_D03_14 R21 FMC_D30
IO_L3P_T0_DQS_PUDC_B_14 U22
IO_L3N_T0_DQS_EMCCLK_14 V22
IO_L4P_T0_D04_14 T21
IO_L4N_T0_D05_14 U21
IO_L5P_T0_D06_14 P19
IO_L5N_T0_D07_14 R19
IO_L6P_T0_FCS_B_14 T19 FPGA_CFG_CS_N1
IO_L6N_T0_D08_VREF_14 T20
IO_L7P_T1_D09_14 W21
IO_L7N_T1_D10_14 W22 FPGA_GPIO_LED_2
IO_L8P_T1_D11_14 AA20 FPGA_GPIO_LED_3
IO_L8N_T1_D12_14 AA21 FMC_D9
IO_L9P_T1_DQS_14 Y21 FMC_A22
IO_L9N_T1_DQS_D13_14 Y22 FMC_A23
IO_L10P_T1_D14_14 AB21 FMC_A19
IO_L10N_T1_D15_14 AB22 FMC_A20
IO_L11P_T1_SRCC_14 U20 FMC_D12
IO_L11N_T1_SRCC_14 V20 FMC_D28
IO_L12P_T1_MRCC_14 W19 DIGITIZED_NOISE
IO_L12N_T1_MRCC_14 W20 FMC_D10
IO_L13P_T2_MRCC_14 Y18 FMC_D8
IO_L13N_T2_MRCC_14 Y19
IO_L14P_T2_SRCC_14 V18 FMC_D29
IO_L14N_T2_SRCC_14 V19
IO_L15P_T2_DQS_RDWR_B_14 AA19 FMC_A25
IO_L15N_T2_DQS_DOUT_CSO_B_14 AB20 FMC_A21
IO_L16P_T2_CSI_B_14 V17
IO_L16N_T2_A15_D31_14 W17 FMC_NL
IO_L17P_T2_A14_D30_14 AA18
IO_L17N_T2_A13_D29_14 AB18 FMC_A24
IO_L18P_T2_A12_D28_14 U17
IO_L18N_T2_A11_D27_14 U18
IO_L19P_T3_A10_D26_14 P14
IO_L19N_T3_A09_D25_VREF_14 R14
IO_L20P_T3_A08_D24_14 R18
IO_L20N_T3_A07_D23_14 T18
IO_L21P_T3_DQS_14 N17
IO_L21N_T3_DQS_A06_D22_14 P17
IO_L22P_T3_A05_D21_14 P15
IO_L22N_T3_A04_D20_14 R16
IO_L23P_T3_A03_D19_14 N13
IO_L23N_T3_A02_D18_14 N14
IO_L24P_T3_A01_D17_14 P16
IO_L24N_T3_A00_D16_14 R17
IO_25_14 N15 FMC_D11
XC7A200TFBG484
R83 0
R84 0
FPGA_CFG_MOSI
FPGA_CFG_MISO
R85 0
FPGA_CFG_CS_N
R65 1k

<-- Disable pull-ups on all pins during configuration

<-- FPGA_GPIO_* and FPGA_IRQ_N_* signals can be swapped

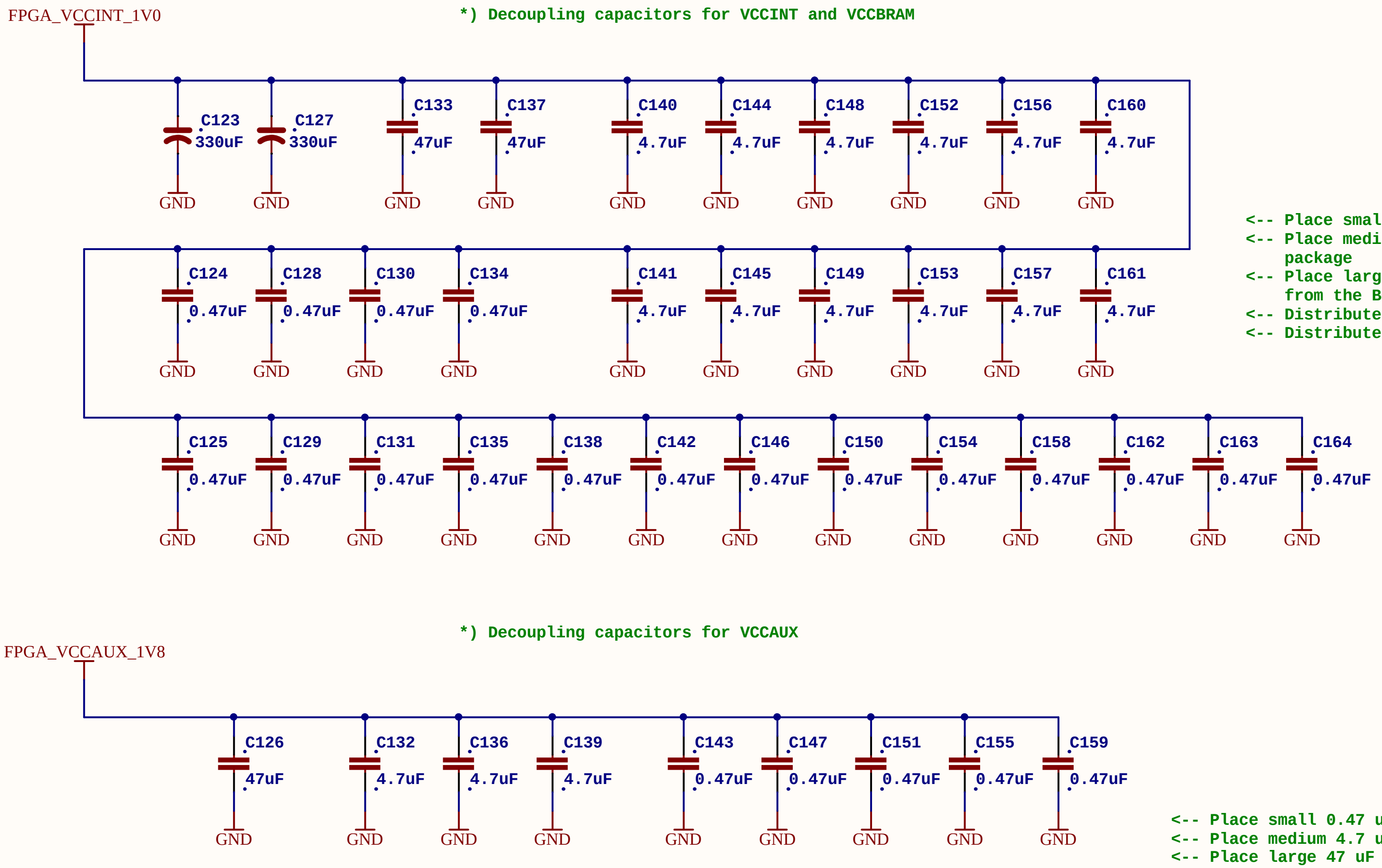
DIGITIZED_NOISE signal should go into
either W19 or Y18 (i.e. into one of the two
positive (master) sides of the two available
MRCC differential pairs)

| | | |
|---|---|---|
| Title | FPGA MKM interface | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_20.SchDoc | | Drawn By: |



| Title | FPGA power and ground | | |
|---|---|---|---|
| Size | Number | | Revision |
| A4 | | | |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_21.SchDoc | Drawn By: | |

*) Decoupling capacitors for VCCINT and VCCBRAM



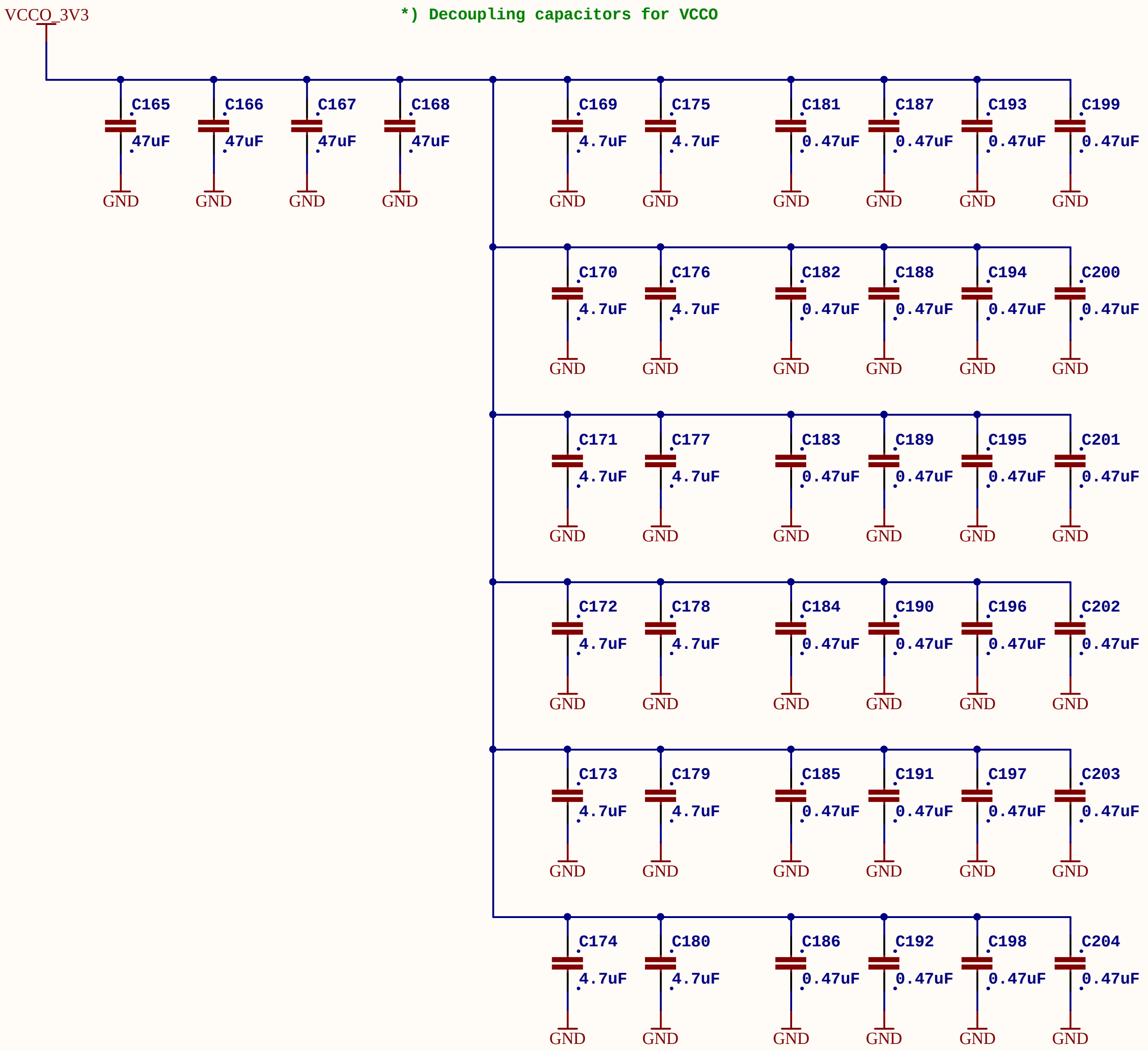
<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF and 330 uF caps not far from the BGA package
<-- Distribute smaller caps evenly under the BGA package
<-- Distribute larger caps evenly around the BGA package

*) Decoupling capacitors for VCCAUX

<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF caps not far from the BGA package
<-- Try to place smaller caps next to FPGA balls

| | | |
|---|---|---|
| Title<br>FPGA CORE and AUX capacitors | | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_22.SchDoc | | Drawn By: |

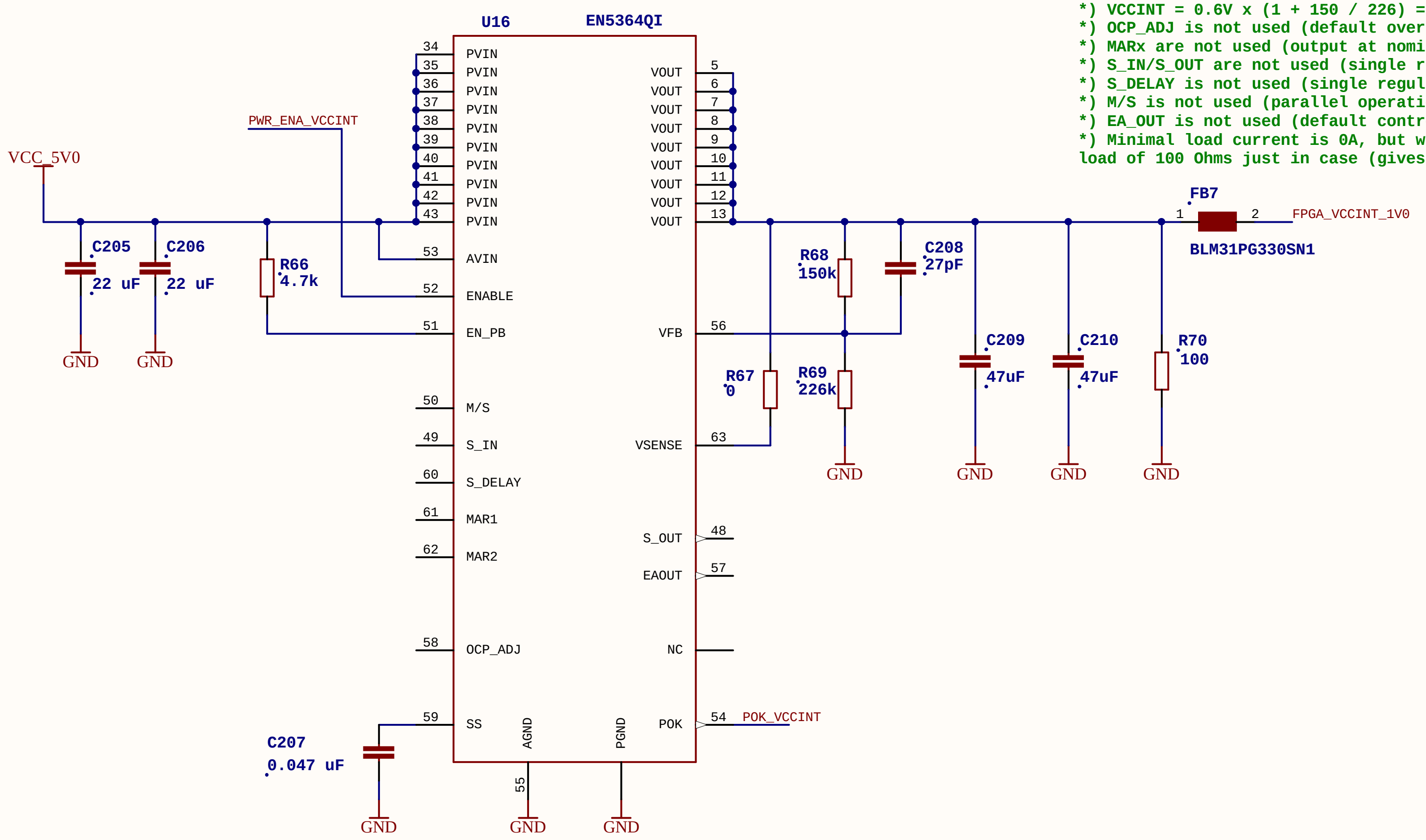
*) Decoupling capacitors for VCCO



<-- Place small 0.47 uF caps right under the BGA package
<-- Place medium 4.7 uF caps very close to the BGA package
<-- Place large 47 uF caps not far from the BGA package
<-- Place one of four 47 uF caps on every side of the BGA p.
<-- Distribute six sets of caps among six FPGA I/O banks

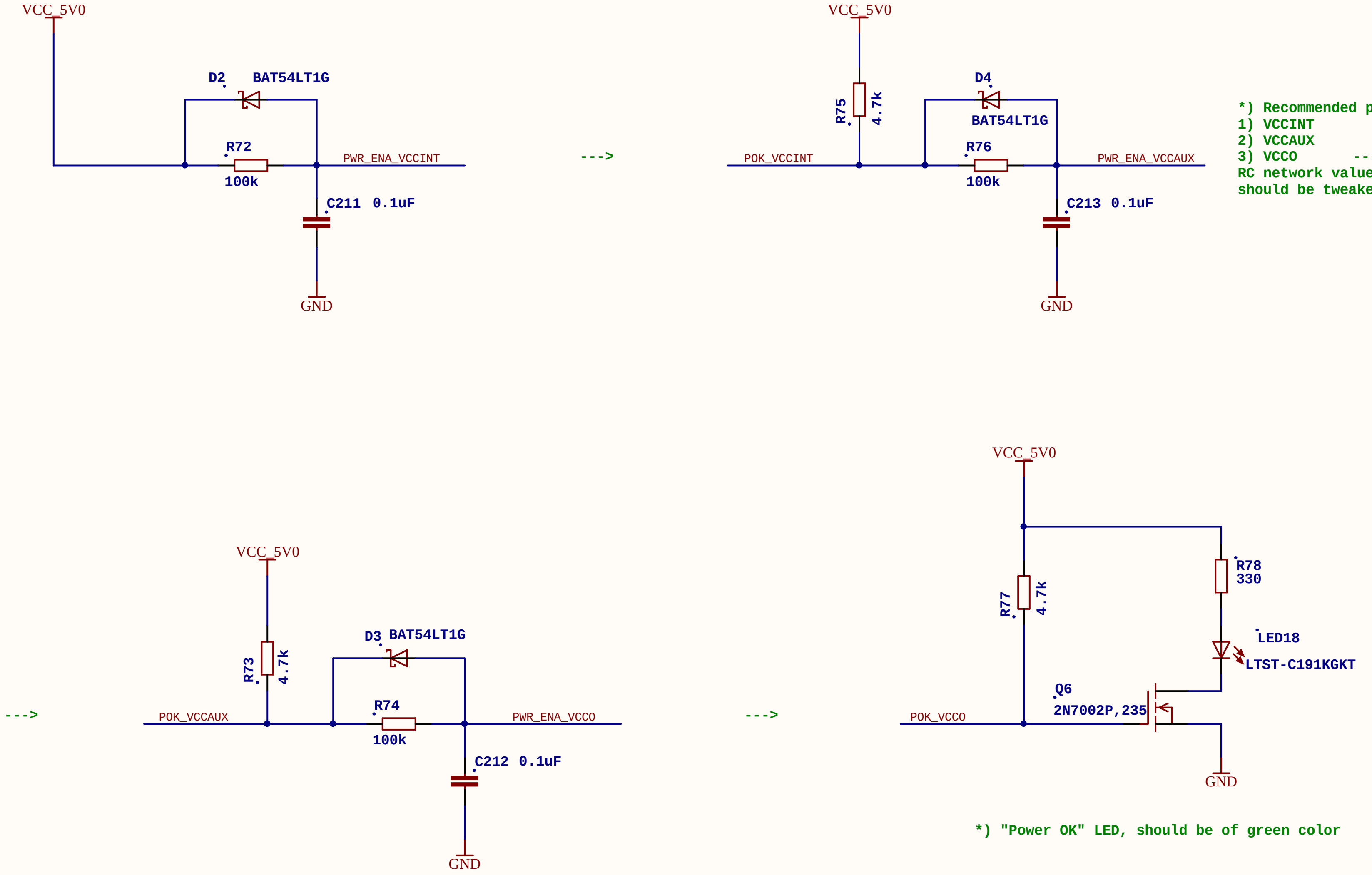
| Title | FPGA VCCO bypass capacitors | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_23.SchDoc | Drawn By: | |

*) FPGA Power Subsystem -- CORE



*) VCCINT = 0.6V x (1 + 150 / 226) = 0.998V
*) OCP_ADJ is not used (default over-current threshold)
*) MARx are not used (output at nominal 100%)
*) S_IN/S_OUT are not used (single regulator mode)
*) S_DELAY is not used (single regulator mode)
*) M/S is not used (parallel operation not needed)
*) EA_OUT is not used (default control loop)
*) Minimal load current is 0A, but we still place
load of 100 Ohms just in case (gives 10 mA)

| | | |
|---|---|---|
| Title<br>FPGA CORE voltage regulators | | |
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_24.SchDoc | | Drawn By: |

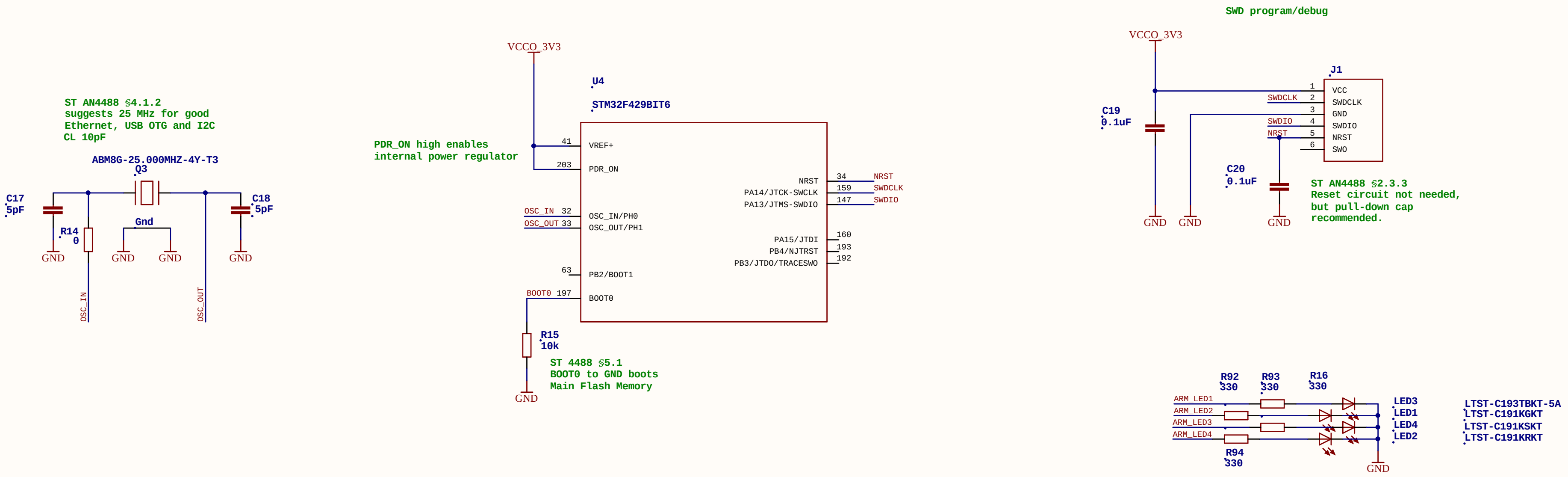


```
*) Recommended power-up sequence:
1) VCCINT
2) VCCAUX
3) VCCO      --->
RC network values are preliminary,
should be tweaked after experiments
```

*) "Power OK" LED, should be of green color

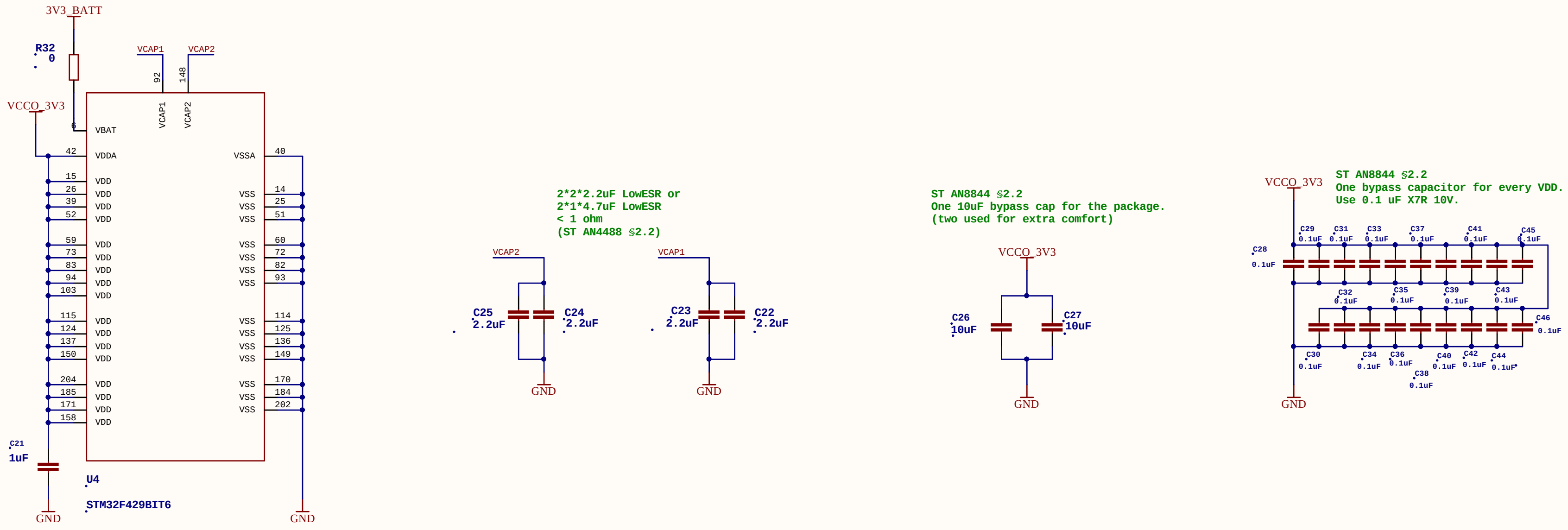
| Title | FPGA power sequencing | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_25.SchDoc | Drawn By: | |

# Basic configuration, STM32



| Title | ARM configuration | |
|---|---|---|
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_3.SchDoc | | Drawn By: |

# Power and bypass capacitors, STM32



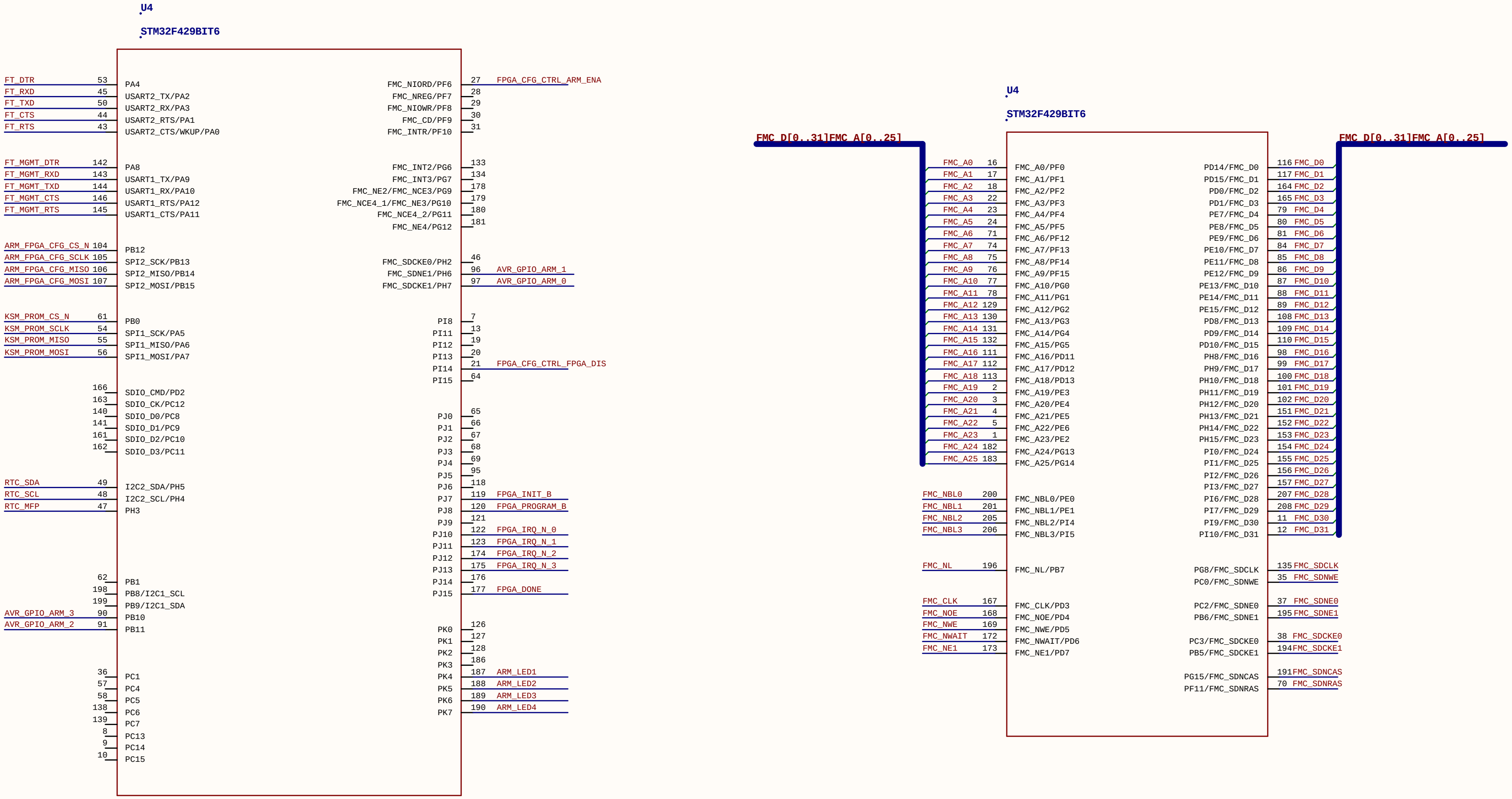
2*2*2.2uF LowESR or
2*1*4.7uF LowESR
< 1 ohm
(ST AN4488 §2.2)

ST AN8844 §2.2
One 10uF bypass cap for the package.
(two used for extra comfort)

ST AN8844 §2.2
One bypass capacitor for every VDD.
Use 0.1 uF X7R 10V.

|  |  |  |  |
|---|---|---|---|
| Title | ARM power |  |  |
| Size<br>A4 | Number |  | Revision |
| Date: | 30.05.2016 | Sheet of |  |
| File: | C:\SHARE\..\rev02_4.SchDoc | Drawn By: |  |

# Input/output, STM32

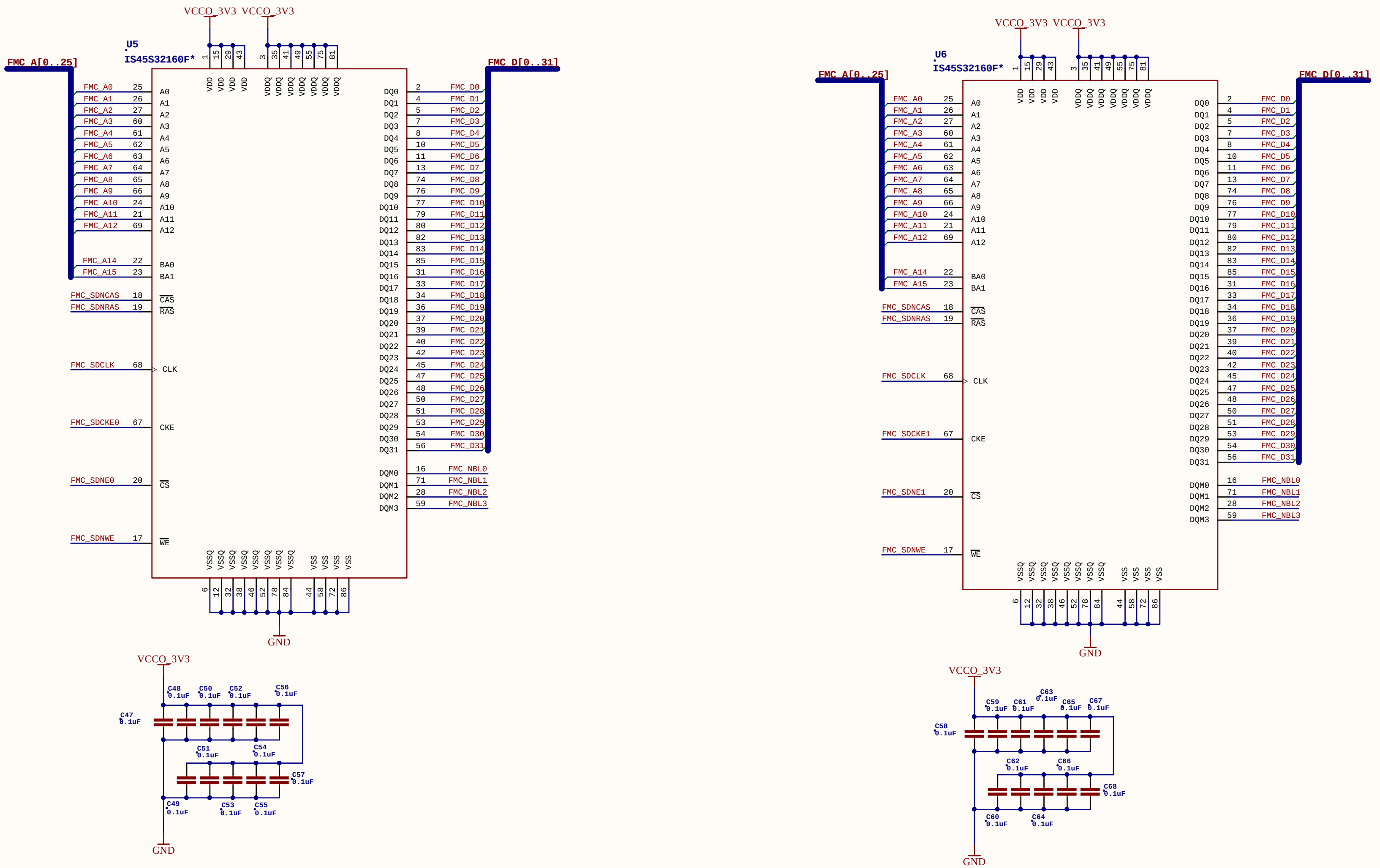


All of these input/outputs can be swapped
with equivalent functionality pins.

| Title | ARM I/O | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_5.SchDoc | Drawn By: | |

# 2x512 Mbit SDRAM memory for the ARM

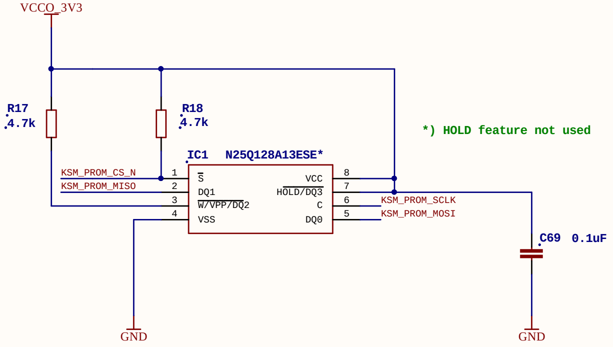
These packages are TSSOP, but if new packages are to be created
for layout, BGA package is preferred.



| Title | SDRAM | | |
|---|---|---|---|
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_6.SchDoc | Drawn By: | |

# Keystore memory, 128 Mbit

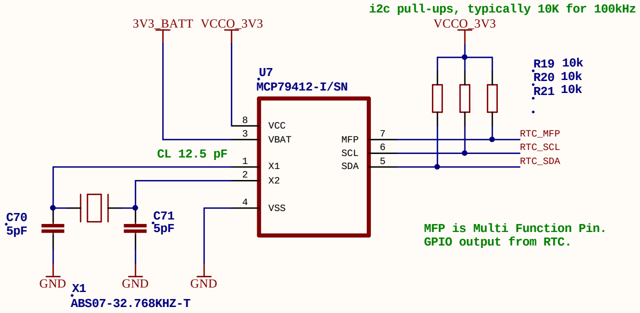
This memory holds cryptographic keys wrapped with the master key.



*) HOLD feature not used

| | | | |
|---|---|---|---|
| Title | **Keystore memory** | | |
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_7.SchDoc | Drawn By: | |

# Real Time Clock

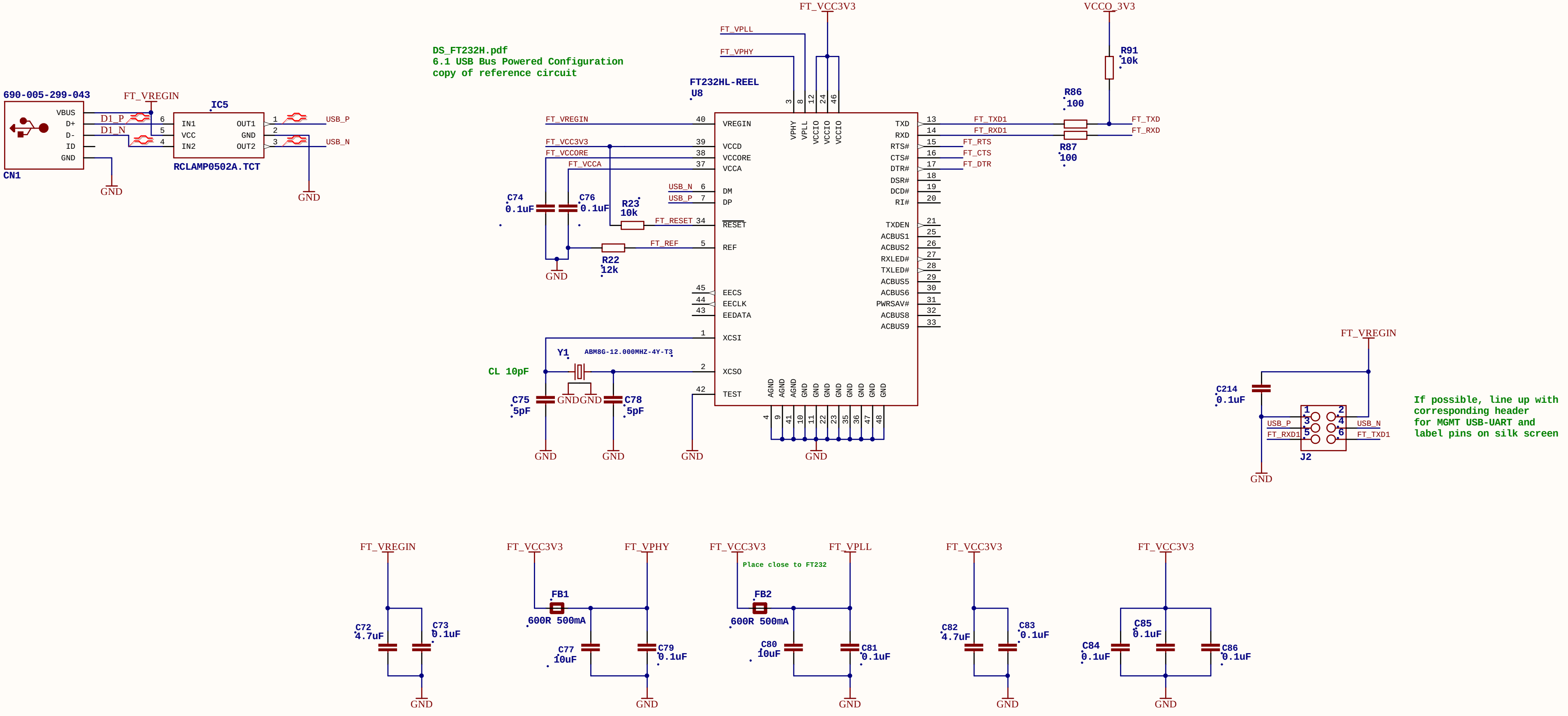


i2c pull-ups, typically 10K for 100kHz

MFP is Multi Function Pin.
GPIO output from RTC.

| | | | |
|---|---|---|---|
| Title | Real Time Clock | | |
| Size<br>A4 | Number | | Revision |
| Date: | 30.05.2016 | Sheet of | |
| File: | C:\SHARE\..\rev02_8.SchDoc | Drawn By: | |

# Application access USB UART



DS_FT232H.pdf
6.1 USB Bus Powered Configuration
copy of reference circuit

CL 10pF

Place close to FT232

If possible, line up with corresponding header for MGMT USB-UART and label pins on silk screen

| Title | USB-UART interface | |
|---|---|---|
| Size<br>A4 | Number | Revision |
| Date: 30.05.2016 | | Sheet of |
| File: C:\SHARE\..\rev02_9.SchDoc | | Drawn By: |