Datasheet Typical Characteristic Simulation in Qspice

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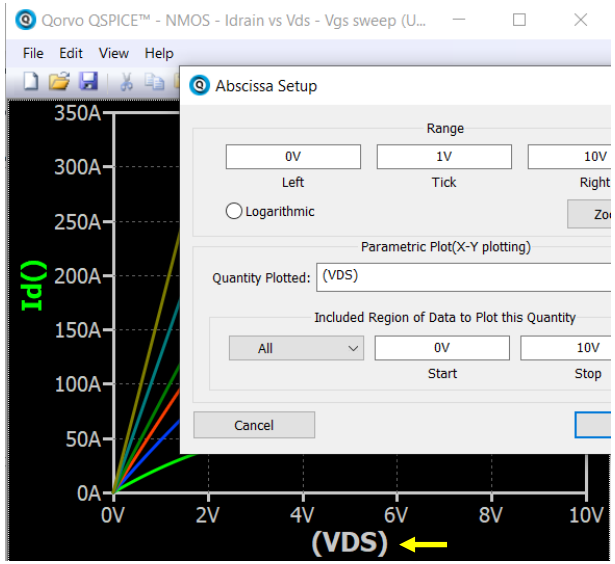
Purpose

- Purpose
  - This presentation provides Qspice simulation test circuit templates for simulating device characteristics as stated in the datasheet

Technique in Waveform Viewer for Datasheet Plot

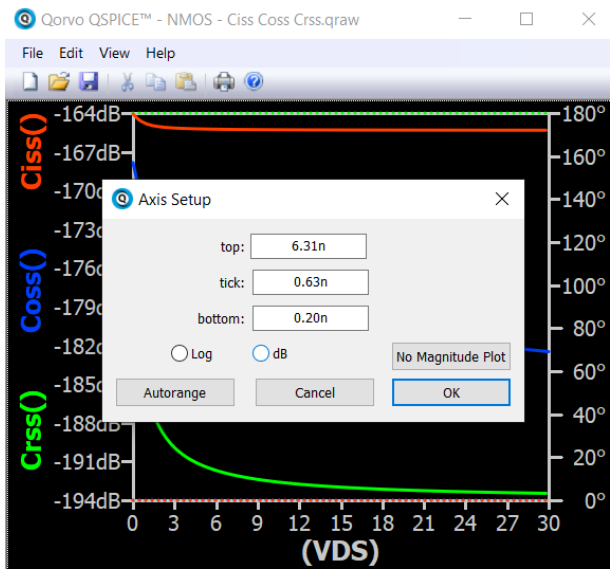
X-Axis Parametric



For X-Axis Label

- Right Click x-axis for Abscissa Setup Window
- In Quantity Plotted, assign to x-axis parameter
- Add bracket () if to display default x-axis parameter

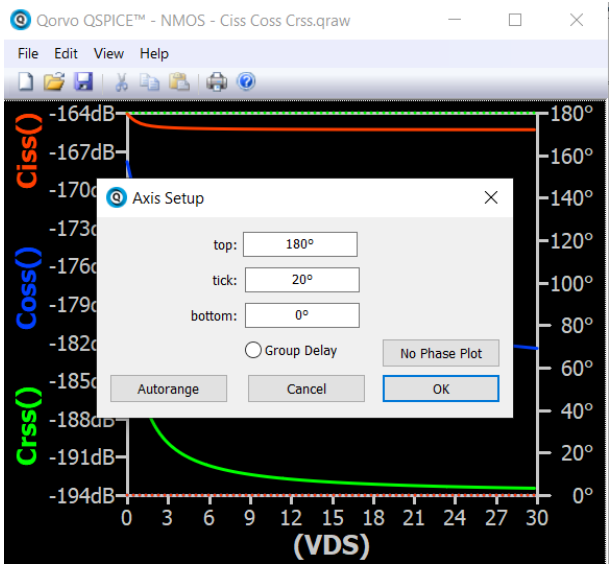
Linear Y-Axis Scale



For Y-Axis Scale

- Right Click y-axis for Axis Setup
- Deselect “Log” and “dB” in .ac can change y-axis to linear scale
- User may adjust top, tick and bottom value

Remove Phase Plot



Remove Phase Plot

- Right Click y-axis (Right side) to open Axis Setup
- Select “No Phase Plot” to disable phase plot

NMOS
N-Channel MOSFET

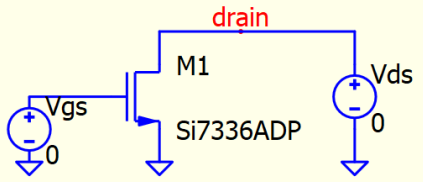
Folder : NMOS

#1 Test Circuit for Drain Current (Id) vs Drain-to-Source Voltage (Vds)

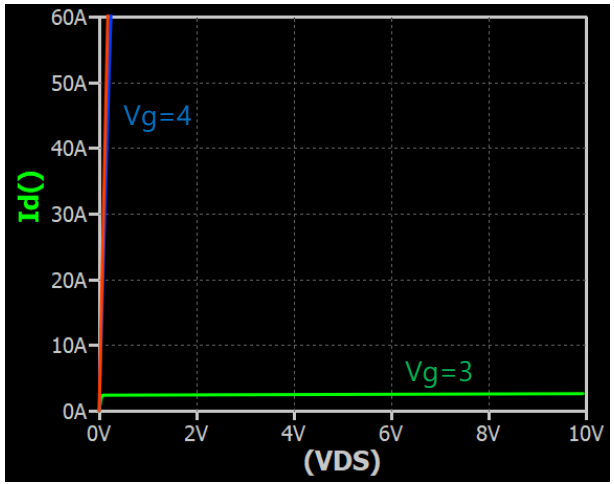
Qspice : NMOS - Idrain vs Vds - Vgs sweep.qsch

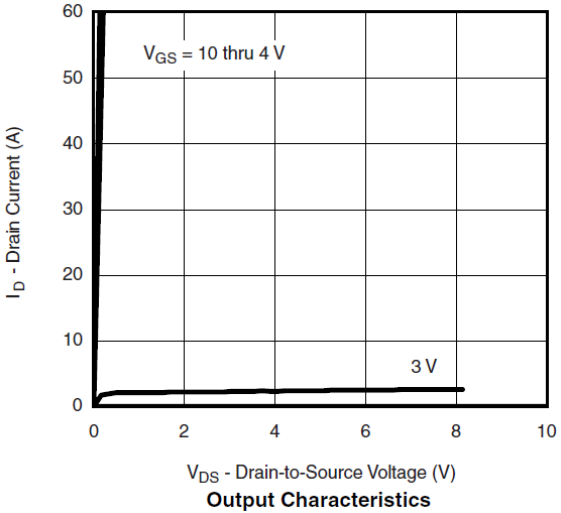
- Test Circuit for Drain Current (Id) vs Drain-to-Source Voltage (Vds)
  - Use .dc directive to sweep Vds and Vg for Drain Current vs Drain-to-Source Voltage characteristic

Test Circuit for Drain Current (Id) vs Drain-to-Source Voltage (Vds)




```
.dc Vds 0 10 0.01 Vgs list 3 4 5
.func Id() -I(Vds)
.plot Id()
.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```



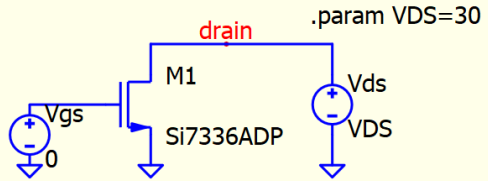


#2 Test Circuit for Drain Current (Id) vs Gate-to-Source Voltage (Vgs)

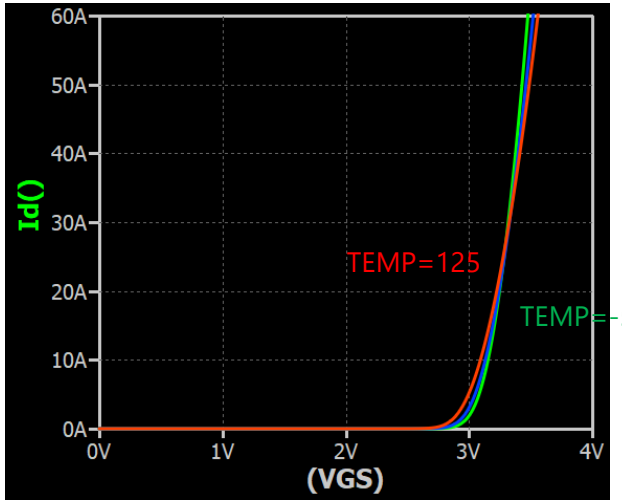
Qspice : NMOS - Idrain vs Vgs - Temp sweep.qsch

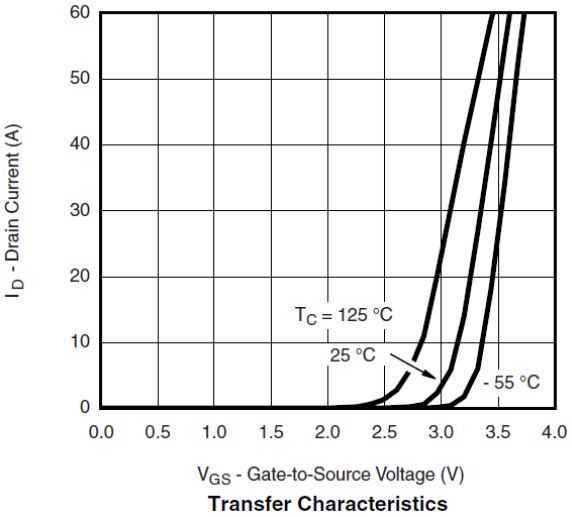
- Test Circuit for Drain Current (Id) vs Gate-to-Source Voltage (Vgs)
  - Use .dc directive to sweep Vgs and .step param TEMP to sweep temperature
  - ** The device model does not match the datasheet well in this condition

Test Circuit for Drain Current (Id) vs Gate-to-Source Voltage (Vgs)




```
.dc Vgs 0 4 0.01
.step param TEMP list -55 25 125
.func Id() -I(Vds)
.plot Id()
.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```





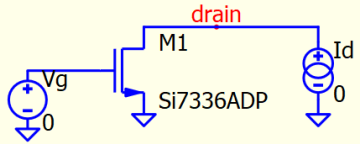
#3 Test Circuit for On-Resistance Rds(on) vs Drain Current Id

Qspice : NMOS - Rdson vs Idrain.qsch

- Test Circuit for On-Resistance Rds(on) vs Drain Current Id
  - A current source Id is used to force drain current to sweep and resistance is calculated by

$$R_{ds,on} = \frac{V_{drain}}{I_{drain}}$$

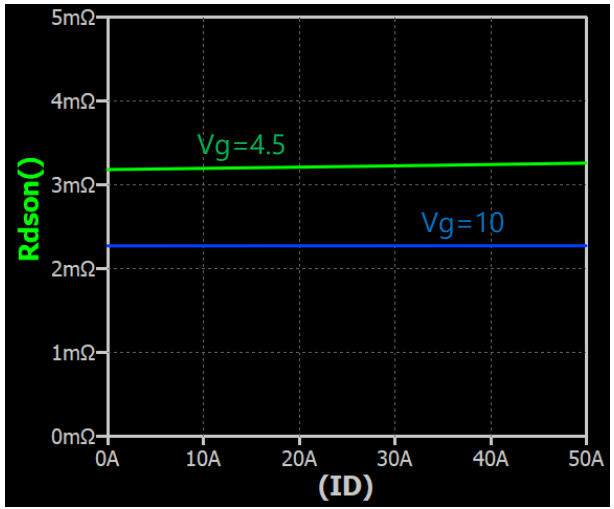
Test Circuit for On-Resistance Rds(on) vs Drain Current Id

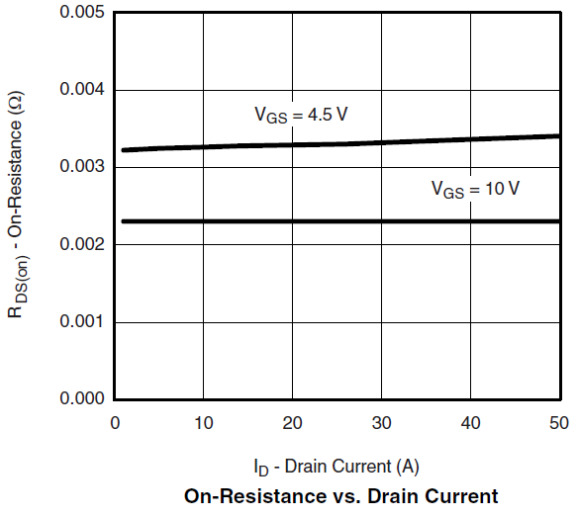



```
.dc Id 1m 50 1 Vg list 4.5 10
.func Rdson() V(drain)/I(Id)
.plot Rdson()
```

(.dc) DC Sweep :
Id from 1mA to 50A
Vg at 4.5V and 10V

```
.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```





On-Resistance vs. Drain Current

#4 Test Circuit for Ciss, Crss and Coss

Qspice : NMOS - Ciss Coss Crss.qsch

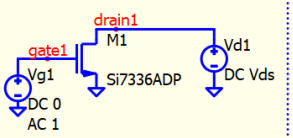
- Test Circuit for Ciss, Crss and Coss
  - Use .ac analysis for capacitance measurement
  - Use .func to get imaginary of impedance with $Z = R + jX = \frac{V}{I}$, where $X = im(Z)$
  - With equation $jX_C = \frac{1}{j2\pi fC} = j\frac{1}{-2\pi fC}$ → Capacitance can be calculated by $C = -\frac{1}{2\pi f X_C}$

Test Circuit for Ciss, Crss and Coss

```
.param f=1Meg
.ac list f
.step param Vds 0 30 0.2
.plot Crss() Coss() Ciss()
```

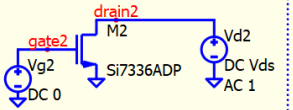
```
.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Qo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```

Measure Ciss vs Vds

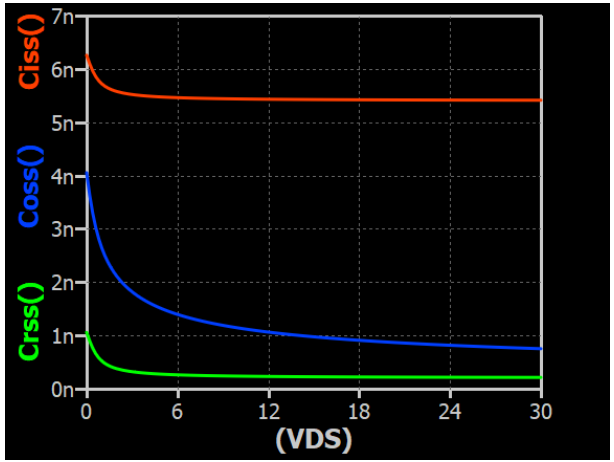


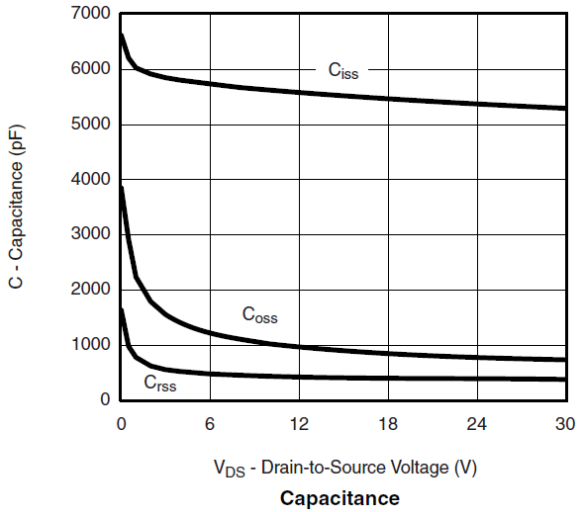

```
// formula to calculate Ciss
.func imZciss() imag(V(gate1)/-I(Vg1))
.func Ciss() -1/2/pi/f/imZciss()
```

Measure Coss, Crss vs Vds




```
// formula to calculate Coss and Crss
.func imZcoss() imag(V(drain2)/-I(Vd2))
.func Coss() -1/2/pi/f/imZcoss()
.func imZcrss() imag(V(drain2)/-I(Vg2))
.func Crss() -1/2/pi/f/imZcrss()
```



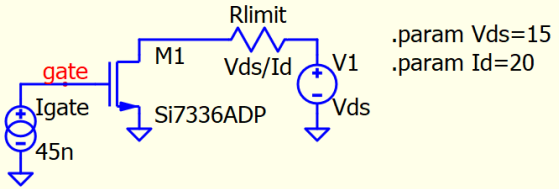


#5 Test Circuit for Gate-to-Source Voltage (Vgs) and Gate Charge (Qg)

Qspice : NMOS - Vgs vs Qg Gate Charge.qsch

- Test Circuit for Gate-to-Source Voltage (Vgs) and Gate Charge (Qg)
  - .tran analysis is required as charge can be calculated by $Q = I \times t$
  - Simulation method is to use a constant current source with 1s transient analysis, by the end, total charge equal current source value as $Q_{total} = I_{value} \times 1s = I_{value}$
  - A resistor R1 is used to limit maximum drain current as datasheet specified Vds and Id, where Rlimit can be defined as $R_{limit} = \frac{V_{ds}}{I_d}$

Measure Gate-to-source Voltage vs Gate Charge (Qg)

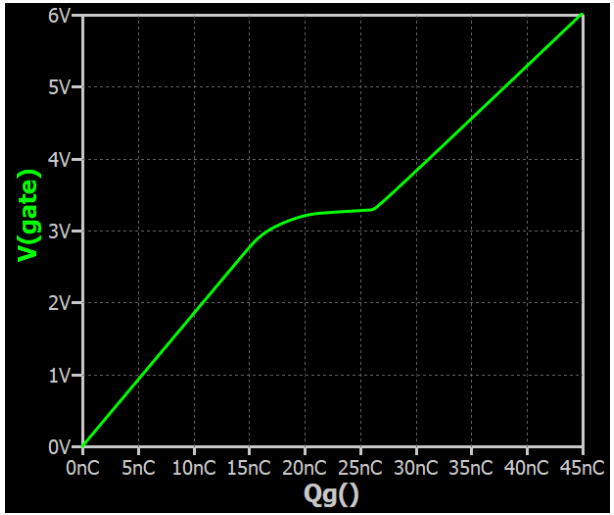


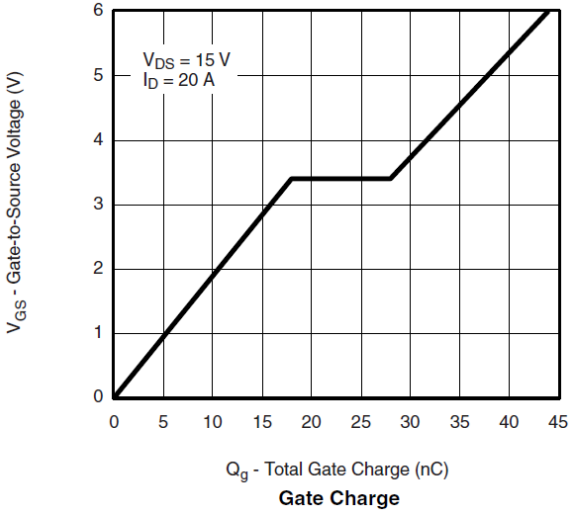
.param Vds=15
.param Id=20

```
.tran 1    .ic V(gate)=0
.func Qg() I(Igate)*time
.plot V(gate)
```

** Change x-axis from time to Qg() in waveform viewer

```
.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```



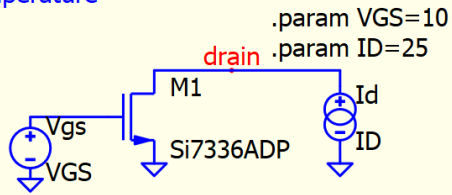


#6 Test Circuit for On-Resistance Rds(on) vs Temperature

Qspice : NMOS - Rdson vs Temp.qsch

- Test Circuit for On-Resistance Rds(on) vs Temperature
  - This circuit is to directly plot Rds,on vs Temperature
  - For normalized plot
    - After simulation, in waveform viewer, measure Rdson @ 25°C, change formula to Rdson()/Rdson@T25
    - Or, add another NMOS and add TEMP=25 attribute to have a device with Rdson@25°C in simulation
  - ** The device model does not match the datasheet well in this condition

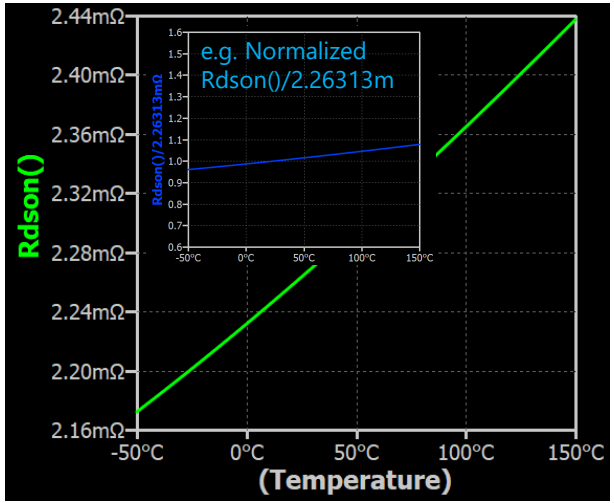
Test Circuit for On-Resistance Rds(on) vs Temperature

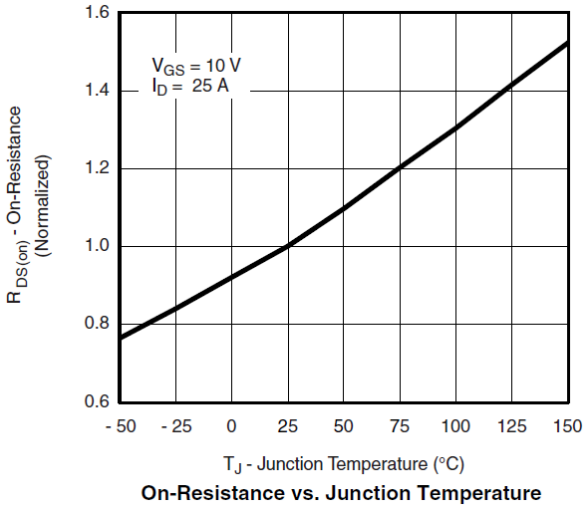



```
.dc TEMP -50 150 1

.func Rdson() V(drain)/I(Id)
.plot Rdson()

.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)
```



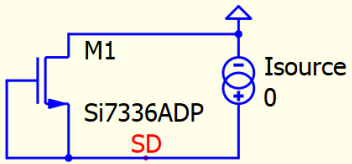


#7 Test Circuit for Source Current vs Source-to-Drain Voltage

Qspice : NMOS - Isource vs Vsd.qsch

- Test Circuit for Source Current (Is) vs Source-to-Drain Voltage (Vsd)
  - This test is to measure body diode forward characteristic, where gate-source is shorted to turn MOSFET off
  - .step param TEMP list 25 150 is to specify temperature step at 25°C and 150°C

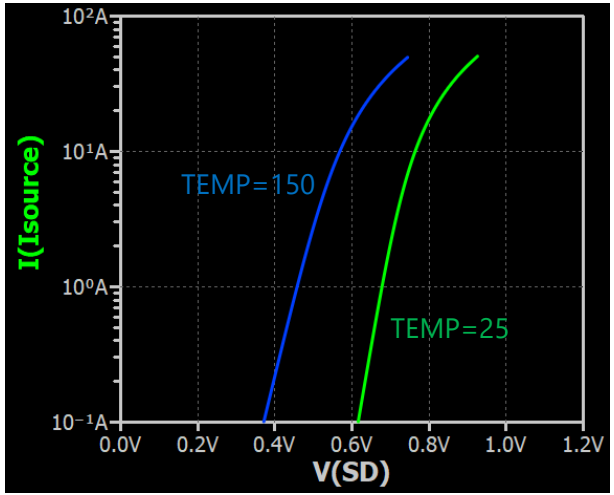
Source Current (Is) vs Source-to-Drain Voltage (VSD)
** to measure body diode forward characteristic

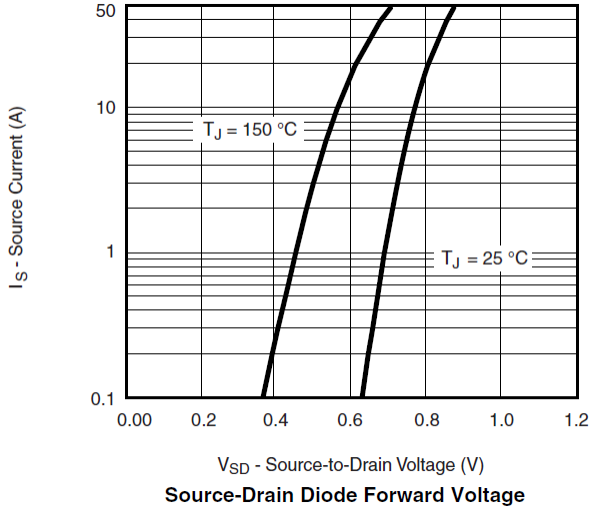


.dc Isource 0.1 50 0.1
.plot I(Isource)
.step param TEMP list 25 150

In waveform viewer, y-axis set to log, x-axis as V(SD)

.model Si7336ADP VDMOS(Rg=3.5 Rd=1.2m Rs=800µ mtriode=1.9
+lambda=0.01 Vto=2.9 Ksubthres=100m Kp=280 Cgdmax=1.6n
+Cgdmin=200p A=1.5 Cgs=5.2n Cjo=3n M=.5 Is=5p Rb=3m
+mfg=Siliconix Vds=30 Ron=2.4m Qg=36n)





Source-Drain Diode Forward Voltage